



2006

INTERNATIONAL SYMPOSIUM ON
VLSI DESIGN, AUTOMATION, AND TEST
(VLSI-DAT)

PROCEEDINGS OF TECHNICAL PAPERS

- April 26-28, 2006
- AMBASSADOR HOTEL
- HSINCHU, TAIWAN
- <http://vlsidat.itri.org.tw>

Copyright and Reprint Permission Statement

FOR PRINT VERSION

Copyright and Reprint Permission: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Operations Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331. All rights reserved. Copyright ©2006 by the Institute of Electrical and Electronics Engineers.

IEEE Catalog Number: 06TH8869

ISBN: 1-4244-0179-8

Library of Congress: 2006920748

Publication Office

STC/ITRI

A000, Bldg. 9, 195-4, Chung Hsin Rd.
Chutung, Hsinchu, Taiwan 31015, R.O.C.
Tel: +886-3-591-9046
Fax: +886-3-582-0233
E-mail: vlsidat@itri.org.tw

IEEE Conference Publications Management Group

445 Hoes Lane
Piscataway, NJ 08854 U.S.A.
Tel: (732)562-3872
Fax: (732)981-1769
E-mail: confpubs@ieee.org

CONTENT

PLENARTY SESSION

Technical Program Chair: Youn-Long Lin (National Tsing Hua University, Taiwan)

K1. New Strategies for System Level Design

Daniel D. Gajski.....	1
-----------------------	---

K2. DFM in Perspective - A Challenge and Opportunity in Nanometer Era -

Katsuhiko Shimohigashi.....	6
-----------------------------	---

K3. VLSI & Mobility

Bruno Thuillier.....	7
----------------------	---

INVITED INDUSTRIAL SESSION

Session Chair: An-Yeu Wu (National Taiwan University, Taiwan)

IS1 A Low-Power and Compact Sigma-Delta Voice-band Codec in a 0.18- μ m CMOS Technology

Daniel Quoc-Dang Ho, Chinchi Chang, Jeetin Rathore, Lewelyn D'Souza, Yuwen Swei, Kuan-Dar Chen, Jyhfong Lin.....	8
---	---

IS2 Chaos In Phase Locked Loop

Ping-Ying Wang.....	12
---------------------	----

IS3 A Low Power Mobile Camera Processor Design with SubLVDS Interface

Charng Lee, Kuang-Ting Hsiao, Min-Chung Chou.....	14
---	----

IS4 Experiences In Deep Sub-Micron Scan-Based At-Speed Delay Testing

Jih-Ning Lee, Ta-Chia Yeh, Chi-Feng Wu, Shih-Arn Hwang, Chao-Cheng Lee.....	18
---	----

IS5 New LCD Display Technology for High Performance with Low Cost-Shared Pixel Rendering Display

Chih-Chung Chien, Adom Wang, Weber Chien.....	22
---	----

Session W2B: RF Front-end (I)

Session Chair: Shen-Juan Liu (National Taiwan University, Taiwan)

W2B1 Circuit and System Design for a Homodyne W-CDMA Front-End Receiver RF IC

D. Y.C. Lie, J. Kennedy, D. Livezey, B. Yang, T. Robinson, N. Sornin, C. Saint, L.E. Larson.....	25
--	----

W2B2 A CMOS Variable Gain Amplifier with DC Offset Calibration Loop for Wireless Communications

Zhih-Siou Cheng, Jenn-Chyou Bor.....	29
--------------------------------------	----

W2B3 A New CMOS VCO Topology With Capacitive Degeneration And Transformer Feedback

Yun-Hsueh Chuang, Shao-Hua Lee, Chien-Feng Lee, Sheng-Lyang Jang, Min-Horng Juang.....	33
--	----

W2B4 Design Trade-offs for Low-power and High Figure-of-merit LNA

Hsien-Ku Chen, J. R. Sha, Da-Chiang Chang, Ying-Zong Juang, Chin-Fong Chiu.....	37
---	----

Session W3A: High Performance Circuit Design

Session Chair: Shyh-Jye Jou (National Chiao Tung University, Taiwan)

W3A1	Alpha and Neutron SER of embedded-SRAM and Novel Estimation Method	
Toshikazu Fukuda, Shigeyuki Hayakawa, Naoyuki Shigyo.....	41	
W3A2	Novel High-Density Data-Retention Power Gating Structure Using a Four -Terminal Double-Gate Device	
Keunwoo Kim, Koushik K. Das, Ching- Te Chuang.....	45	
W3A3	Power-Gating Schemes for Ultra-Thin SOI (UTSOI) Circuits in Hybrid SOI - Epitaxial CMOS Structures	
Shih-Hsien Lo, Koushik K. Das, Ching- Te Chuang, Jeffrey W. Sleight.....	49	
W3A4	Sleep Transistor Design and Implementation – Simple Concepts Yet Challenge To Be Optimum	
Kaijian Shi, David Howard.....	51	

Session W3B: High Performance SoC Architecture

Session Chair: Satoshi Goto (Waseda University, Japan)

W3B1	High Performance On-chip Interconnect System Supporting Fast SoC Generation	
Ori Goren, Yaron Netanel.....	55	
W3B3	Hazard-Aware Performance Prediction for Automatic Instruction-Set Selection	
Peter Hallschmid, Resve Saleh.....	59	
W3B4	61.5mW 2048-bit RSA Cryptographic Co-processor LSI based on N bit-wised Modular Multiplier	
Toru Hisakado, Nobuyuki Kobayashi, Satoshi Goto, Takeshi Ikenaga, Kunihiko Higashi, Ichiro Kitao, Yukiyasu Tsunoo.....	63	

Session T1A: DVB Baseband Techniques

Session Chair: Luca P. Carloni (Columbia University, NY, USA)

T1A1	SoC for COFDM Wireless Communications: Challenges and Opportunities (Invited)	
Chen-Yi Lee, Hsuan- Yu Liu, and Chien-Ching Lin.....	67	
T1A2	A 0.18μm CMOS Prototype of COFDM Demodulator for European DVB-T Standard	
Chua-Chin Wang, Jian-Ming Huang, Yung-Mu Tseng, Chih-Yi Chang.....	71	
T1A3	A Channel Equalizer Design for COFDM System	
Ying-Hao Ma, Lei-Fone Chen, Chen-Yi Lee.....	75	

Session T1B: RF Front-end (II)

Session Chair: Chin-Fong Chiu (National Chip Implementation Center, Taiwan)

T1B1	Monolithic Class E SiGe Power Amplifiers Design with Wideband High-Efficiency and Linearity (Invited)	
Donald Y.C. Lie, Jeremy D. Popp, Patrick Lee, Annie H. Yang, Jason F. Rowland, F. Wang, Don Kimball.....	79	
T1B2	A 2.4-GHz/3.5-GHz/5-GHz Multi-Band LNA with Complementary Switched Capacitor Multi-Tap Inductor in 0.18μm CMOS	
Wei-Chang Li, Chao-Shiun Wang, Chorng-Kuang Wang.....	83	
T1B3	Design and Implementation of a DC-to-17-GHz UWB SiGe LNA with a Peaking Inductor	
Shu-Hui Yen, Yo-Sheng Lin.....	87	

Session T2A: Digital Signal Processing Architecture

Session Chair: Chen-Yi Lee (National Chiao Tung University, Taiwan)

T2A1	VLSI Architecture for Variable Block Size Motion Estimation in H.264/AVC with Low Cost Memory Organization	
	Yang Song, Zhenyu Liu, Takeshi Ikenaga, Satoshi Goto.....	89
T2A2	A Low-Power and High-Quality Cordic Based Loeffler DCT	
	Chi-Chia Sun, Benjamin Heyne, Shanq-Jang Ruan, Juergen Goetze.....	93
T2A3	An Efficient Field-Partition Based Code Compression and Its Pipelined Decompression System	
	Yuan-Long Jeang, Yong-Zong Lin.....	97
T2A4	High-Throughput LDPC Decoder for long code-length	
	Tatsuyuki Ishikawa, Kazunori Shimizu, Takeshi Ikenaga, Satoshi Goto.....	101

Session T2B: Data Converters

Session Chair: Yun Chiu (University of Illinois at Urbana-Champaign, USA)

T2B1	A 75MS/s Low Power Pipeline ADC with scalable Resolution	
	David Muthers, Reinhard Tielert.....	105
T2B2	A 6-b 1.3Gs/s A/D Converter with C-2C Switch-Capacitor Technique	
	Ying-Min Liao, Tai-Cheng Lee.....	109
T2B3	A 250MHz 11BIT 20mW CMOS Low-Hold-Pedestal Fully Differential Track-and-Hold Circuit	
	Tsung-Sum Lee, Chi-Chang Lu, Jian-Ting Zhan.....	113
T2B4	Clock-Jitter Reduction Techniques in Continuous Time Delta-Sigma Modulators	
	Hashem Zare-Hoseini, Izzet Kale.....	117

Session T3A: Low Power Design and Optimization

Session Chair: Ting Ting Huang (National Tsing Hua University)

T3A1	Challenges on Low-Power Platform Design for Real-World Wireless Sensing Applications (Invited)	
	Pai H. Chou.....	119
T3A2	Automatic Low Power Optimizations during ADL-driven ASIP Design	
	Anupam Chattopadhyay, D. Kammler, E. M. Witte, O. Schliebusch, H. Ishebabi, B. Geukes, R. Leupers, G. Ascheid, H. Meyr.....	123
T3A3	A Partition-Based Voltage Scaling Algorithm Using Dual Supply Voltages for Low Power Designs	
	Hung Hsie Lee, Sung Han Tsai, Jun Cheng Chi, Mely Chen Chi.....	127

Session T3B: SoC Design, Verification and Application

Session Chair: Shih-Chieh Chang (National Tsing Hua University, Taiwan)

T3B1	Software Verification for System on a Chip using a C/C++ Simulator and FPGA Emulator (Invited)	
	Yuichi Nakamura.....	131
T3B2	Cycle-accurate Verification of AHB-based RTL IP with Transaction-level System Environment	
	Heejun Shim, Sang-Heon Lee, Yun-Sik Woo, Moo-Kyoung Chung, Jae-Gon Lee, Chong-Min Kyung	135
T3B3	System Redundancy; A Means of Improving Process Variation Yield Degradation in Memory Arrays	
	Ahmed M. Eltawil, Fadi J. Kurdahi.....	139

Session T4A: Physical Design

Session Chair: Shih-Hsu Huang (Chung Yuan Christian University, Taiwan)

T4A1	Floorplanning Multiple Reticles for Multi-project Wafers	
Meng-Chiou Wu, Shr-Cheng Tsai, Rung-Bin Lin.....	143	
T4A2	Design Migration from Peripheral ASIC Design to Area-IO Flip-Chip Design by Chip I/O Planning and Legalization	
Chia-Yi Chang, Hung-Ming Chen.....	147	
T4A3	Thermal-Driven Interconnect Optimization by Simultaneous Gate and Wire Sizing	
Yi-Wei Lin, Yao-Wen Chang.....	151	
T4A4	A VLSI Layout Legalization Technique Based On A Graph Fixing Algorithm	
S. D. Wu, Chun-Chi Tsai, Michael Yang.....	155	

Session T4B: Testing and Diagnostics in the Deep-Submicron Era

Session Chair: Chau-Chin Su (National Chiao Tung University, Taiwan)

T4B1	Modeling and Testing of Intra-Cell Bridging Defects Using Butterfly Structure	
Lu-Yen Ko, Shi-Yu Huang, Jia-Liang Chiou, Han-Chia Cheng.....	159	
T4B2	An Infrastructure IP for Repairing Multiple RAMs in SOCs	
Chao-Da Huang, Tsu-Wei Tseng, Jin-Fu Li.....	163	
T4B3	A Supply-Gating Scheme for Both Data-Retention and Spike-Reduction in Power Management and Test Scheduling	
Tsung-Chu Huang, Jing-Chi Tzeng, Yuan-Wei Chao, Ji-Jan Chen, Wei-Ting Liu, Kuen-Jong Lee.....	167	
T4B4	A New Robust Paradigm for Diagnosing Hold-Time Faults in Scan Chains	
Jui-Jung Hsu, Shi-Yu Huang, Chao-Wen Tzeng.....	171	

Session F1A: Design Flow, Optimization and Modeling

Session Chair: Juinn-Dar Huang (National Chiao Tung University, Taiwan)

F1A2	Improving Single-Pass Redundancy Addition and Removal with Inconsistent Assignments	
Wing-Hang Lo, Yu-Liang Wu.....	175	
F1A3	Gain-based Cell Delay Modeling	
Shahin Nazarian, Massoud Pedram	179	

Session F1B: High-Speed Analog Circuits

Session Chair: David Chang (STC/ITRI, Taiwan)

F1B1	The HOY Tester- Can IC Testing Go Wireless? (Invited)	
Cheng-Wen Wu, Chih-Tsun Huang, Shi-Yu Huang, Po-Chiun Huang, Tsin-Yuan Chang, Yu-Tsao Hsing.....	183	
F1B2	Gb/s CMOS 1-4th-rate CDR with Frequency Detector and Skew Calibration	
Sitt Tontisirin, Reinhard Tielert.....	187	
F1B3	A Fully Integrated Spread Spectrum Clock Generator	
Chao-Chyun Chen, Sheng-Chou Lee, Shen-Iuan Liu.....	191	

Session F2A: Digital Timing Module

Session Chair: Jinn-Shyan Wang (National Chung Cheng University, Taiwan)

F2A1	An All-Digital Duty Cycle Corrector	Bo-Jiun Chen, Shao-Ku Kao, Shen-Iuan Liu.....	195
F2A2	An All-Digital Delay-Locked Loop for DDR SDRAM Controller Applications	Ching-Che Chung, Pao-Lung, Chen-Yi Lee.....	199
F2A3	Adaptive Quadrature Clock Generator	Juin-Hau Huang, Chih-Hsien Lin, Shyh-Jye Jou.....	203
F2A4	An All-Digital Phase-Locked Loop with High-Resolution for SoC Applications	Duo Sheng, Ching-Che Chung, Chen-Yi Lee.....	207

Session F2B: Regulators and Equalizers

Session Chair: Gin-Kou Ma (STC/ITRI, Taiwan)

F2B1	A Capacitor-free CMOS Low Dropout Regulator with Slew Rate Enhancement	Wei-Jen Huang, Sao-Hung Lu, Shen-Iuan Liu.....	211
F2B2	A Power Efficient and Fast Transient Response Low Drop-Out Regulator in Standard CMOS Process	Chung-Wei Lin, Yen-Jen Liu.....	215
F2B3	An Adaptive 3.125Gbps Coaxial Cable Equalizer	Jian-Hao Lu, Chi-Lun Luo, Shen-Iuan Liu.....	219
F2B4	Blind Adaptive Mixed-Signal DFE for Gb/s, Multi-Drop, Buses	Henrik Fredriksson, Christer Svensson	223

Poster Session I: Digital, SoC, EDA and DFT

Session Chair: Ching-Te Chuang (IBM T. J. Watson Research Center, USA)

PI1	Improving the Reliability of JFFS2	Chin-Hsing Chen, Wen-Tzeng Huang, Chun-Ta Chen, Rong-Shue Hsiao.....	227
PI2	Efficient Hardware/Software Partitioning Approach for Embedded Multiprocessor Systems	Tzong-Yen Lin, Yu-Ting Hung, Rong-Guey Chang.....	231
PI3	Multilevel Large-Scale Modules Placement with Refined Neighborhood Exchange	Kuan-Chung Wang, Hung-Ming Chen.....	235
PI4	A Multi-Code Compression Technique for Reducing System-On-Chip Test Time	Hong-Ming Shieh, Chun-Shien Wu, Jin-Fu Li.....	239
PI5	On Feasibility of HOY- A Wireless Test Methodology for VLSI Chips and Wafers	Po-Kai Chen, Yu-Tsao Hsing, Cheng-Wen Wu.....	243
PI6	Memory-Hierarchy-Based Power Reduction for H.264/AVC Video Decoder	Tsu-Ming Liu, Chen-Yi Lee	247
PI7	A High-Speed Baseband Receiver for MIMO OFDM Based WLAN	Tsung-Hsueh Lee, Jing-Siang Jhuang, Tzi-Dar Chiueh	251
PI8	A Lower-Power Viterbi Decoder Design Methodology Based on Dynamic Survivor Path Decision	Yun-Nan Chang, Yu-Chung Ding.....	255

PI9	Power-On Current Control In Sleep Transistor Implementations	259
	David Howard, Kajjian Shi.....	

Poster Session II: Analog, Mixed-Signal & RF Design

Session Chair: Li-Ren Huang (STC/ITRI, Taiwan)

PII1	A Self-Biased Current Source Based Power-on Reset Circuit for On-Chip Applications	263
	Amit Katyal, Nitin Bansal.....	
PII2	A Fully Integrated Ultra-Low-Power High-Voltage Driver for Bistable LCDs	267
	J. Doutreloigne.....	
PII3	Impact of Interstitial Carbon on Base Current Ideality in SiGe:C Heterojunction Bipolar Transistors	271
	J.P. Liu, P.R. Verma, S.F. Chu, S.Q. Zhang, W.B. Loh, K.C. Leong, H.L. Siew, D.K. Sohn, L.C. Hsia.....	
PII4	The Column Driver Circuit Design for Passive Organic Electroluminescence Display	273
	Wen-Yaw Chung, Yu-Chien Tseng, Yu-Wen Chen, Chih-Jen Yen.....	
PII5	A Highly Integrated SiGe BiCMOS Class F Power Amplifier for Bluetooth Application	277
	Jia-Liang Chen, Tang-Jung Chiu, Christina F. Jou.....	
PII6	A Merged LNA-Mixer Design with On-Chip Balun	279
	Hsien-Ku Chen, J. R. Sha, Da-Chiang Chang, Ying-Zong Juang, Chin-Fong Chiu.....	
PII7	A 4.8GHz Low-Phase Noise Quadrature Colpitts VCO	281
	Sheng-Lyang Jang, Yun-Hsueh Chuang, Chien-Feng Lee, Shao-Hua Lee.....	
PII8	Modeling of Hi-Q Embedded Inductors for RF-SOP Applications	285
	Y.S. Tsai, T.S. Horng.....	
PII9	V-Band CMOS Differential-type Injection Locked Frequency Dividers	289
	Fan-Hsiu Huang, Yi-Jen Chan.....	
PII10	A 1.5V Current-Mode Operational Amplifier Using Level Shifter Technique	291
	Socheat Heng, Cong-Kha Pham	
PII11	A Low Power, Transverse Analog FIR Filter as Feed Forward Equalizer in Gigabit Ethernet	295
	M.B. Vahidfar, O. Shoaei, M.Fardis.....	
PII12	Design and Implementation of a 1-V Dual-Transformer-Feedback LNA and a 5-GHz-Band Transformer-Feedback VCO	299
	Yo-Sheng Lin, Si-Chang Chen, and Shu-Bin Chang.....	
PII13	A New Low Voltage CMOS Micromixer for 2.45GHz Applications	301
	Chin-Hsien Yen, Win-Ming Chang, Kuo-Hua Cheng, Christina F. Jou.....	