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Session 5 – Measurement Techniques for High Speed Signals
Cedar Ballroom, Monday Morning, September 11
Chair: Jeanne Trinko-Mechler Co-Chair: Robert Aitken

On-chip signal digitization and capture at 70-GHz is presented in the first paper. Next is offered a jitter and link characterization tutorial which addresses standards such as PCI Express, Fibre Channel, and Giga Bit Ethernet. A novel bus probing technique based on electromagnetic couplers is presented in the third paper. The session closes with an innovative circuit design which allows a two order improvement in characterization accuracy of the frequency response of on-chip continuous-time filters.

Session 6 – Power Optimized RF and Wireline SoCs
Oak Ballroom, Monday Afternoon, September 11
Chair: Aurangzeb Khan Co-Chair: Rakesh Patel

The first four papers present software-assisted GSM radio RF processing, 802.11 WLAN integration, multiprocessing and integrated power management for wireless products. The next four papers present SoCs with 6.375 Gb/s SerDes I/Os, 22.5 Gb/s cross-current and a 10 Gb/s framer. A human-body network processor with less than 30uW power, and a 15 dB SNR substrate noise reduction for wireline networks.

Session 7 – Wireless Transmitter Building Blocks
Fir Ballroom, Monday Afternoon, September 11
Chair: Cicero Vaucher Co-Chair: Payam Heydari

The session starts with an invited paper on low-power design challenges, followed by advances in wireless transmitter building blocks, including direct modulators, a wide-band VCO, and high-efficiency PA techniques.

Session 10 – Advanced Memories
Oak Ballroom, Tuesday Morning, September 12
Chair: Phil Diodato Co-Chair: Jean-Christophe Vial

Next generation DRAM technology and FIN-FET SRAMs are presented. Exhaustive SER analysis and low cost test methods are described. CAM design techniques are highlighted.

8:00 am Introduction

Session 11 – Emerging Technologies: Materials and Structures
Fir Ballroom, Tuesday Morning, September 12
Chair: Dawn Fitzgerald Co-Chair: Mourad El-Gamal

This session focuses on emerging materials and structures including microfluid platforms for DNA detection, antennas used for communications on chip, carbon nanotubes forming an innovative memory and MEMS structures integrated for leakage control.

Session 12 – Nyquist Analog-to-Digital Converters
Pine Ballroom, Tuesday Morning, September 12
Chair: David Nairn Co-Chair: Takahiro Miki

Nyquist analog-to-digital converters continue to push the accuracy, speed and low-power boundaries by exploiting circuit techniques and newer processing technologies.

Session 13 – Signal and Data Processing
Cedar Ballroom, Tuesday Morning, September 12
Chair: Bryan Ackland Co-Chair: Ravi Kolagotla

Mobile computing and communications are primary market drivers for today's integrated circuit technology. Papers describe novel techniques for providing improved communications and application signal processing capability while maintaining low power consumption.

Session 14 – Design for Test and Reliability
Fir Ballroom, Tuesday Morning, September 12
Chair: Hamid Mahmoodi Co-Chair: Kenichi Osada

Architecting reliability is the focus of the first two invited papers, followed by a paper on capturing supply noise, another on at-speed structural test, concluding with a paper on improving EM-robustness in inductors.

Session 15 – SoC/SiP 3-D Power/Signal Transport And MEMS/Sensors Management
Oak Ballroom, Tuesday Afternoon, September 12
Chair: Paul Billig Co-Chair: Ric Williams

Novel techniques for SoC/SiP are presented which include wireless power transmission and high density through die vias for SiP, a photo diode interface for automotive, and a high voltage generator for MEMS.

Session 16 – Eye-Opening Circuits
Fir Ballroom, Tuesday Afternoon, September 12
Chair: Tony Chan Carusone Co-Chair: Jafar Savoj

This session focuses on CMOS wireline transceiver building blocks. A tutorial on transmit equalization and two novel clock and data recovery architectures are described.

2:00 pm **Introduction**

2:05 pm **16.1** **Wireline Equalization Using Pulse-Width Modulation (INVITED PAPER),** *J. Schrader, E. Klumperink, J. Visschers* and B. Nauta, University of Twente, Enschede, The Netherlands, *NIKHEF, Amsterdam, The Netherlands* **591**

2:55 pm **16.2** **A 10Gbps Burst-Mode CDR Circuit in 0.18µm CMOS,** *C-F. Liang, S-C. Hwu and S-I. Liu, National Taiwan University, Taipei, Taiwan, ROC* **599**

3:20 pm **16.3** **A 1.6Gbps Digital Clock and Data Recovery Circuit,** *P. Hanumolu, M. Kim, G-Y. Wei* and U-K. Moon, Oregon State University, Corvallis, OR, *Harvard University, Cambridge, MA* **603**

3:45 pm **BREAK**

Session 17 – Analog Techniques
Pine Ballroom, Tuesday Afternoon, September 12
Chair: Don Thelen Co-Chair: Kathleen Philips

Speed isn't everything! This session covers circuits with challenges in other dimensions including voltage references, voltage regulators and high voltage circuits.

2:00 pm **Introduction**

2:05 pm **17.1** **A Sub-1V Low-Noise Bandgap Voltage Reference,** *K. Sanborn, D. Ma and V. Ivanov*, University of Arizona, Tucson, AZ, *Texas Instruments, Inc., Tucson, AZ* **607**

2:30 pm **17.2** **A Compact Programmable CMOS Reference With 40µV Accuracy,** *V. Srinivasan, G. Serrano, C. Twigg and P. Hasler, Georgia Institute of Technology, Atlanta, GA* **611**

2:55 pm **17.3** **A Transient-Enhanced 20µA-Quiescent 200mA-Load Low-Dropout Regulator With Buffer Impedance Attenuation,** *M. Al-Shyoukh, R. Perez and H. Lee*, Texas Instruments Inc., Dallas, TX, *University of Texas at Dallas, Richardson, TX* **615**

3:20 pm **17.4** **Compact Outside-Rail Circuit Structure By Single-Cascode Two-Transistor Topology,** *A. Tamtrakarn, H. Ishikuro*, K. Ishida** and T. Sakurai, University of Tokyo, Tokyo, Japan, Keio University, Yokohama, Japan, Tokyo Institute of Technology, Yokohama, Japan* **619**

3:45 pm **BREAK**

Session 18 – Productivity Enhancement and Design Optimization
Cedar Ballroom, Tuesday Afternoon, September 12
Chair: Gennady Gildenblat Co-Chair: Rob Jones

This session presents the most important advances in compact models, simulation algorithms, and web-based design methodologies for productivity improvement and design optimization.

2:00 pm **Introduction**

2:05 pm **18.1** **Enhancing Productivity by Continuously Improving Standard Compact Models (INVITED PAPER),** *J. Watts, IBM Mocroelectronics, Essex Junction, VT* **623**

2:55 pm **18.2** **A Web Tool for Interactive Exploration of Analog Design Tradeoffs,** *C. Recker, B. Braswell, P. Drennan and C. McAndrew, Freescale Semiconductor, Tempe, AZ* **631**

3:20 pm **18.3** **Circuit Optimization Using Scale Based Sensitivities,** *B. Agrawal, F. Liu* and S. Nassif*, IBM EDA, Fishkill, NY, *IBM Austin Research Lab., Austin, TX* **635**

3:45 pm **BREAK**

Session 19 – Afternoon Panel Discussion
Oak Ballroom, Tuesday Afternoon, September 12

4:00 pm – 5:30 pm
Can the Analog/RF Designer/Enterpreneur Make Money in a Fabless Startup?

Session 20 – Afternoon Panel Discussion
Fir Ballroom, Tuesday Afternoon, September 12

4:00 pm – 5:30 pm
Fabless to Designless – How Do We Manage Globalization Challenges?

Session 21 – Custom Circuits
Oak Ballroom, Wednesday Morning, September 13
Chair: Ken Szajda Co-Chair: Jacqueline Snyder

The session covers a number of applications ranging from current and voltage effective generation to custom circuits used in optical sensor systems, MEMS and implantable biomedical micro-systems.

8:00 am **Introduction**

8:05 am **21.1** **A 4-Channel High-Precision Constant Current Control ASIC for Automotive Transmission Applications,** *W. Horn, M. Graefling, G. Gross, M. Steiner, J. Treiber, R. Dickman, and K. Reis, Infineon Technologies Austria AG, Austria* **639**

8:30 am **21.2** **Dithering Skip Modulator with a Width Controller for Ultra-wide-load High-Efficiency DC-DC Converters,** *H-W. Huang, H-H. Ho*, C-C. Chien*, K-H. Chen*, G-K. Ma** and S-Y. Kuo, National Taiwan University, Taipei, Taiwan, *National Chiao Tung University, Hsinchu, Taiwan, **ITRI, Hsinchu, Taiwan* **643**

Session 28 – High Speed Analog
Pine Ballroom, Wednesday Afternoon, September 13
Chair: Yusuf Haque Co-Chair: David Rich

This session presents advances in on chip noise suppression, improvements on filter tuning and linearity, temperature sensing techniques, dc and ac amplifier performance and low noise oscillator.

Session 29 – Modeling and EDA Challenges in Nano-CMOS
Cedar Ballroom, Wednesday Afternoon, September 13
Chair: Yuhua Cheng Co-Chair: Hidetoshi Onodera

This session discusses and reviews modeling and EPA challenges in nano-scale CMOS technologies. The impact of variabilities on device and circuit performances will also be covered.