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Henry Chang, General Chair

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Dr. Sanjay K. Jha, Executive Vice President of QUALCOMM Incorporated and President of QUALCOMM CDMA Technologies

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Oak Ballroom, Monday Morning, September 11

Chair: Steve Wilton Co-Chair: Arif Rahman

Programmable devices provide a low-cost, low-risk path to complex analog, digital, and mixed-signal implementations. This session highlights circuit and architectural techniques that make these devices possible.

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Chair: John Rogers Co-Chair: Ali Niknejad

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Cedar Ballroom, Monday Morning, September 11

Chair: Jeanne Trinko-Mechler Co-Chair: Robert Aitken

On-chip signal digitization and capture at 70-GHz is presented in the first paper. Next is offered a jitter and link characterization tutorial which addresses standards such as PCI Express, Fibre Channel, and Giga Bit Ethernet. A novel bus probing technique based on electromagnetic couplers is presented in the third paper. The session closes with an innovative circuit design which allows a two order improvement in characterization accuracy of the frequency response of on-chip continuous-time filters.

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Chair: Aurangzeb Khan

Co-Chair: Rakesh Patel

The first four papers present software-assisted GSM radio RF processing, 802.11 WLAN integration, multiprocessing and integrated power management for wireless products. The next four papers present SoCs with 6.375 Gb/s SerDes I/Os, 22.5 Gb/s cross-current and a 10 Gb/s framer. A human-body network processor with less than 30uW power, and a 15 dB SNR substrate noise reduction for wireline networks.

1:30 pm Introduction

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Session 7 – Wireless Transmitter Building Blocks

Fir Ballroom, Monday Afternoon, September 11

Chair: Cicero Vaucher

Co-Chair: Payam Heydari

The session starts with an invited paper on low-power design challenges, followed by advances in wireless transmitter building blocks, including direct modulators, a wide-band VCO, and high-efficiency PA techniques.

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Session 10 – Advanced Memories

Oak Ballroom, Tuesday Morning, September 12

Chair: Phil Diodato

Co-Chair: Jean-Christophe Vial

Next generation DRAM technology and FIN-FET SRAMs are presented. Exhaustive SER analysis and low cost test methods are described. CAM design techniques are highlighted.

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10:00 am 10.4	Spreading Diversity in Multi-Cell Neutron-Induced Upsets with Device Scaling (INVITED PAPER) , E. Ibe, S. Chung*, S. Wen*, H. Yamaguchi, Y. Yahagi, H. Kameyama**, S. Yamamoto***, and T. Akioka**, Hitachi, Ltd., Kanagawa, Japan, *Cisco Systems, Inc., San Jose, CA, **Renesas Technology Corp., Tokyo, Japan, ***Renesas Technology Corp., Hyogo, Japan	437		Nyquist analog-to-digital converters continue to push the accuracy, speed and low-power boundaries by exploiting circuit techniques and newer processing technologies.	
10:50 am 10.5	Low Cost Test of High Bandwidth Embedded Memories (INVITED PAPER) , K. Gorman, D. Anand, G. Pomichter and W. Corbin, IBM Systems and Technology Group, Essex Junction, VT	445	8:00 am	Introduction	
11:15 am 10.6	High-Temperature, High Reliability EEPROM Design For Automotive Applications , J. Walsh and G. Scott, AMI Semiconductor, Pocatello, ID	449	8:05 am 12.1	Frequency-Based Measurement of Mismatches Between Small Capacitors , A. Verma and B. Razavi, University of California, Los Angeles, CA	481
11:40 am 10.7	Self-Referenced Sense Amplifier for Across-Chip-Variation Immune Sensing in High-Performance Content Addressable Memories , I. Arsovski and R. Wistort, IBM Silicon Solutions, Essex Junction, VT	453	8:30 am 12.2	A Calibration-Free 14b 70MS/s 3.3mm² 235mW 0.13µm CMOS Pipeline ADC with High-Matching 3-D Symmetric Capacitors , Y-J. Cho, K-H. Lee, H-C. Choi, S-H. Lee, K-H. Moon* and J-W. Kim*, Sogang University, Seoul, Korea, *Samsung Electronics Co., Ltd., Gyeonggi-Do, Korea	485
	Session 11 – Emerging Technologies: Materials and Structures Fir Ballroom, Tuesday Morning, September 12 Chair: Dawn Fitzgerald Co-Chair: Mourad El-Gamal		8:55 am 12.3	A 3.5 GS/s 5-b Flash ADC in 90 nm CMOS , S. Park, Y. Palaskas*, A. Ravi*, R. Bishop* and M. Flynn, University of Michigan, Ann Arbor, MI, *Intel Corporatio, Hillsboro, OR	489
	This session focuses on emerging materials and structures including microfluid platforms for DNA detection, antennas used for communications on chip, carbon nanotubes forming an innovative memory and MEMS structures integrated for leakage control.		9:20 am 12.4	A 30-GS/sec Track and Hold Amplifier in 0.13-µm CMOS Technology , S. Shahramian, S. Voinigescu and A. Chan Carusone, University of Toronto, Toronto, Canada	493
8:00 am	Introduction		9:45 am	BREAK	
8:05 am 11.1	Integrated MEMS Switches for Leakage Control of Battery Operated Systems , A. Raychowdhury, J. Kim, D. Peroullis and K. Roy, Purdue University, West Lafayette, IN	457	10:00 am 12.5	A 10b 25MS/s 4.8mW 0.13µm CMOS ADC for Digital Multimedia Broadcasting Applications , Y-J. Cho, D-H. Sa, Y-W. Kim, K-H. Lee, H-C. Choi, S-H. Lee, Y-D. Jeon*, S-C. Lee* and J-K. Kwon*, Sogang University, Seoul, Korea, *ETRI, Daejeon, Korea	497
8:30 am 11.2	CNT Based Mechanical Devices for ULSI Memory (INVITED PAPER) , J. Jang, S. Cha, Y. Choi, D. Kang*, T. Butler, D. Hasko, J. Kim** and G. Amaratunga, University of Cambridge, Cambridge, UK, *Sungkyunkwan University, Suwon, Korea, *Samsung Advanced Institute of Technology, Yongin, Korea	461	10:25 am 12.6	A 1.2 V, 24 mW/ch, 10 bit, 80 MSample/s Pipelined A/D Converters , T. Ueno, T. Ito, D. Kurose, T. Yamaji and T. Itakura, Toshiba Corporation, Kawasaki, Japan	501
			10:50 am 12.7	Low-Power Design of Pipeline A/D Converters (INVITED PAPER) , S. Kawahito, Shizuoka University, Hamamatsu, Japan	505
			11:40 am 12.8	A 1.8-V 22-mW 10-bit 30-MS/s Subsampling Pipelined CMOS ADC , J. Li, X. Zeng, L. Xie, J. Chen, J. Zhang and Y. Guo*, Fudan University, Shanghai, China, *Shanghai MicroScience Integrated Circuits Co., Ltd., Shanghai, China	513

Session 13 – Signal and Data Processing

Cedar Ballroom, Tuesday Morning, September 12

Chair: Bryan Ackland Co-Chair: Ravi Kolagotla

Mobile computing and communications are primary market drivers for today's integrated circuit technology. Papers describe novel techniques for providing improved communications and application signal processing capability while maintaining low power consumption.

8:00 am	Introduction	
8:05 am 13.1	Digital Signal Processing for RF at 45-nm CMOS and Beyond (INVITED PAPER), B. Staszewski, K. Muhammad and D. Leipold, Texas Instruments, Dallas, TX	517
8:55 am 13.2	Delta-Sigma Modulation in Direct Digital Frequency Synthesis, D. Yang, W. Ni*, F. Dai, Y. Shi* and R. Jaeger, Auburn University, Auburn, AL, *Chinese Academy of Sciences, China	523
9:20 am 13.3	OFDM Modulator With Digital IF and On-Chip D/A-Converter, J. Lindeberg, O. Väänänen, J. Pirkkalanemi, M. Kosunen and K. Halonen, Helsinki University of Technology, Espoo, Finland	527
9:45 am	BREAK	
10:00 am 13.4	Neuromorphic Vision Systems for Mobile Applications (INVITED PAPER), R. Etienne-Cummings, S. Mehta, R. Philipp and V. Gruev*, Johns Hopkins University, Baltimore, MD, *University of Pennsylvania, Philadelphia, PA	531
10:25 am 13.5	A Low-Power Unified Arithmetic Unit for Programmable Handheld 3-D Graphics Systems, B-G. Nam, H Kim and H-J. Yoo, KAIST, Daejeon, Korea	535
10:50 am 13.6	A Scalable 7.2 Mb/s 3GPP HSDPA Co-processor with Advanced NLMS Receiver and Receive Diversity for Mobile Terminals, C. Thomas, M. Cooke, O. Ridler, K. Van Den Beld, D. Yip, U. Sontowski, A. Kind, G. Zhou, Y-C. Li, L. Ung, R. Banna, B. Widdup, T. Prokop, M. Bickerstaff, G. Woodward, R. Srikantiah*, K. Gupta*, R. Reddy*, S. Arvapalli*, R. Bidnur*, P. Avss*, R. Lang, C. Nicol, Agere Systems, North Ryde, Australia, *Agere Systems, Bangalore, India	539
11:15am 13.7	A GFLOPS Vector-DSP for Broadband Wireless Applications, E. Matus, H. Seidel, T. Limberg, P. Robelly and G. Fettweis, Dresden University of Technology, Dresden, Germany	543

Session 14 – Design for Test and Reliability

Fir Ballroom, Tuesday Morning, September 12

Chair: Hamid Mahmoodi Co-Chair: Kenichi Osada

Architecting reliability is the focus of the first two invited papers, followed by a paper on capturing supply noise, another on at-speed structural test, concluding with a paper on improving EM-robustness in inductors.

9:55 am	Introduction	
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10:00 am 14.1	SRAMs in Scaled Technologies Under Process Variations: Failure Mechanisms, Test and Variation Tolerant Design (INVITED PAPER), S. Mukho-padhyay, A. Agarwal, Q. Chen and K. Roy, Purdue University, West Lafayette, IN	547
10:25 am 14.2	The UltraSPARC T1 Processor: CMT Reliability (INVITED PAPER), A. Leon, B. Langley and J. Shin, Sun Microsystems Inc., Sunnyvale, CA	555
10:50 am 14.3	A Time-Slicing Ring Oscillator for Capturing Instantaneous Delay Degradation and Power Supply Voltage Drop, T. Sato, Y. Matsumoto, K. Hirakimoto, M. Komoda and J. Mano, Renesas Technology Corporation, Tokyo, Japan	563
11:15 am 14.4	Design For At-Speed Structural Test And Performance Verification Of High-Performance ASICs, V. Iyengar, M. Johnson, T. Anemikos, G. Grise, M. Taylor, R. Farmer, F. Woytowich and B. Bassett, IBM Microelectronics, Essex Junction, VT	567
11:40 am 14.5	Robust Inductor Design for RF Circuits, Y-L. Lu, Y-H. Lee, W. McMahon and T-C. Fung, Intel Corporation, Santa Clara, CA	571

Session 15 – SoC/SiP 3-D Power/Signal Transport And MEMS/Sensors Management

Oak Ballroom, Tuesday Afternoon, September 12

Chair: Paul Billig Co-Chair: Ric Williams

Novel techniques for SoC/SiP are presented which include wireless power transmission and high density through die vias for SiP, a photo diode interface for automotive, and a high voltage generator for MEMS.

2:00 pm	Introduction	
2:05 pm 15.1	Chip-to-Chip Inductive Wireless Power Transmission System for SiP Applications, K. Onizuka, H. Kawaguchi*, M. Takamiya, T. Kuroda** and T. Sakurai, University of Tokyo, Tokyo, Japan, *Kobe Univ., Kobe, Japan, **Keio Univ., Yokohama, Japan	575
2:30 pm 15.2	Balanced Low Noise High Dynamic Photodiode Interface for Automotive, I. Koudar, AMIS Mixed Signal Design Center, Brno, Czech Republic	579
2:55 pm 15.3	On-chip Digitally Tunable High Voltage Generator for Electrostatic Control of Micromechanical Devices, L. Aaltonen, M. Saukoski and K. Halonen, Helsinki University of Technology, Finland	583
3:20 pm 15.4	Die Stacking Technology for Terabit Chip-to-Chip Communications, A. Rahman, J. Trezza*, B. New, and S. Trimberger, Xilinx Research Lab, San Jose, CA, *Cubic Wafer, Inc., Merrimack, NH	587
3:45 pm	BREAK	

Session 16 – Eye-Opening Circuits

Fir Ballroom, Tuesday Afternoon, September 12

Chair: Tony Chan Carusone

Co-Chair: Jafar Savoj

This session focuses on CMOS wireline transceiver building blocks. A tutorial on transmit equalization and two novel clock and data recovery architectures are described.

2:00 pm	Introduction	
2:05 pm 16.1	Wireline Equalization Using Pulse-Width Modulation (INVITED PAPER), J. Schrader, E. Klumperink, J. Visschers* and B. Nauta, University of Twente, Enschede, The Netherlands, *NIKHEF, Amsterdam, The Netherlands	591
2:55 pm 16.2	A 10Gbps Burst-Mode CDR Circuit in 0.18μm CMOS, C-F. Liang, S-C. Hwu and S-I. Liu, National Taiwan University, Taipei, Taiwan, ROC	599
3:20 pm 16.3	A 1.6Gbps Digital Clock and Data Recovery Circuit, P. Hanumolu, M. Kim, G-Y. Wei* and U-K. Moon, Oregon State University, Corvallis, OR, *Harvard University, Cambridge, MA	603
3:45 pm	BREAK	

Session 17 – Analog Techniques

Pine Ballroom, Tuesday Afternoon, September 12

Chair: Don Thelen

Co-Chair: Kathleen Philips

Speed isn't everything! This session covers circuits with challenges in other dimensions including voltage references, voltage regulators and high voltage circuits.

2:00 pm	Introduction	
2:05 pm 17.1	A Sub-1V Low-Noise Bandgap Voltage Reference, K. Sanborn, D. Ma and V. Ivanov*, University of Arizona, Tucson, AZ, *Texas Instruments, Inc., Tucson, AZ	607
2:30 pm 17.2	A Compact Programmable CMOS Reference With 40μV Accuracy, V. Srinivasan, G. Serrano, C. Twigg and P. Hasler, Georgia Institute of Technology, Atlanta, GA	611
2:55 pm 17.3	A Transient-Enhanced 20μA-Quiescent 200mA-Load Low-Dropout Regulator With Buffer Impedance Attenuation, M. Al-Shyoukh, R. Perez and H. Lee*, Texas Instruments Inc., Dallas, TX, *University of Texas at Dallas, Richardson, TX	615
3:20 pm 17.4	Compact Outside-Rail Circuit Structure By Single-Cascode Two-Transistor Topology, A. Tamtrakam, H. Ishikuro*, K. Ishida** and T. Sakurai, University of Tokyo, Tokyo, Japan, Keio University, Yokohama, Japan, Tokyo Institute of Technology, Yokohama, Japan	619
3:45 pm	BREAK	

Session 18 – Productivity Enhancement and Design Optimization

Cedar Ballroom, Tuesday Afternoon, September 12

Chair: Gennady Gildenblat

Co-Chair: Rob Jones

This session presents the most important advances in compact models, simulation algorithms, and web-based design methodologies for productivity improvement and design optimization.

2:00 pm	Introduction	
2:05 pm 18.1	Enhancing Productivity by Continuously Improving Standard Compact Models (INVITED PAPER), J. Watts, IBM Microelectronics, Essex Junction, VT	623
2:55 pm 18.2	A Web Tool for Interactive Exploration of Analog Design Tradeoffs, C. Recker, B. Braswell, P. Drennan and C. McAndrew, Freescale Semiconductor, Tempe, AZ	631
3:20 pm 18.3	Circuit Optimization Using Scale Based Sensitivities, B. Agrawal, F. Liu* and S. Nassif*, IBM EDA, Fishkill, NY, *IBM Austin Research Lab., Austin, TX	635
3:45 pm	BREAK	

Session 19 – Afternoon Panel Discussion

Oak Ballroom, Tuesday Afternoon, September 12

4:00 pm – 5:30 pm

Can the Analog/RF Designer/Entrepreneur Make Money in a Fabless Startup?

Session 20 – Afternoon Panel Discussion

Fir Ballroom, Tuesday Afternoon, September 12

4:00 pm – 5:30 pm

Fabless to Designless – How Do We Manage Globalization Challenges?

Session 21 – Custom Circuits

Oak Ballroom, Wednesday Morning, September 13

Chair: Ken Szajda

Co-Chair: Jacqueline Snyder

The session covers a number of applications ranging from current and voltage effective generation to custom circuits used in optical sensor systems, MEMS and implantable biomedical micro-systems.

8:00 am	Introduction	
8:05 am 21.1	A 4-Channel High-Precision Constant Current Control ASIC for Automotive Transmission Applications, W. Horn, M. Graeffling, G. Gross, M. Steiner, J. Treiber, R. Dickman, and K. Reis, Infineon Technologies Austria AG, Austria	639
8:30 am 21.2	Dithering Skip Modulator with a Width Controller for Ultra-wide-load High-Efficiency DC-DC Converters, H-W. Huang, H-H. Ho*, C-C. Chien*, K-H. Chen*, G-K. Ma** and S-Y. Kuo, National Taiwan University, Taipei, Taiwan, *National Chiao Tung University, Hsinchu, Taiwan, **ITRI, Hsinchu, Taiwan	643

8:55 am 21.3	Per-Pixel Floating-Point ADCs with Electronic Shutters for a High Dynamic Range, High Frame Rate Infrared Focal Plane Array , S-M. Lee, H. Park and B. Wooley, Stanford University, Stanford, CA	647	8:55 am 23.2	Recent Advances in III-V Electronics (INVITED PAPER) , Y-K. Chen, Y. Baeyens, N. Weimann, J. Lee, J. Weiner, V. Houtsma and Y. Yang, Lucent Technologies, Murray Hill, NJ	687
9:20 am 21.4	Smart CMOS Charge Transfer Readout Circuit for Time Delay and Integration Arrays , C.B. Kim, B-H. Kim, Y.S. Lee, H. Jung and H.C. Lee, KAIST, Daejeon, Korea	651	9:45 am	BREAK	
9:45 am	BREAK		10:00 am 23.3	Electrical Characteristic Fluctuations in Sub-45nm CMOS Devices (INVITED PAPER) , F-L. Yang, J-R. Hwang and Y. Li*, TSMC, Taiwan, ROC, *National Chiao Tung University, Taiwan, ROC	691
10:00 am 21.5	A 104dB SNDR Transimpedance-based CMOS ASIC for Tuning Fork Microgyroscopes , A. Sharma, F. Zaman and F. Ayazi, Georgia Institute of Technology, Atlanta, GA	655	10:25 am 23.4	SiGe BiCMOS Trends - Today and Tomorrow (INVITED PAPER) , J. Dunn, D. Harame, A. Joseph, S. St. Onge, N. Feilchenfeld, L. Lanzerotti, B. Ormer, E. Gebreselasie, J. Johnson, D. Coolbaugh*, R. Rassel and M. Khater**, IBM, Essex Junction, VT, *Hopewell Junction, NY, **Yorktown Heights, NY	695
10:25 am 21.6	Fully-Integrated CMOS Power Regulator for Telemetry-Powered Implantable Biomedical Microsystems , A. Sodagar, K. Wise, K. Najafi and M. Ghovanloo, University of Michigan, Ann Arbor, MI	659	11:15 am 23.5	Advances and Challenges in Flip-Chip Packaging (INVITED PAPER) , R. Mahajan, D. Mallik, R. Sankman, K. Radhakrishnan, C. Chiu and J. He, Intel Corporation, Chandler, AZ	703

Session 22 – Oscillators

Fir Ballroom, Wednesday Morning, September 13

Chair: Amjad Obeidat Co-Chair: Cormac O'Connell

This session presents advances in high-speed, widely-tunable voltage-controlled oscillators and analysis of mutual pulling between oscillators.

8:00 am	Introduction	
8:05 am 22.1	A Varactor-Less 10GHz CMOS LC-VCO for Optical Communications Transceiver SOCs Using Caged Inductors (INVITED PAPER) , A. Maxim, Maxim Inc., Austin, TX	663
8:55 am 22.2	An Ultra Compact Differentially Tuned 6GHz CMOS LC VCO with Dynamic Common-Mode Feedback. , B. Soltanian, H. Ainspan*, W. Rhee*, D. Friedman* and P. Kinget, Columbia University, New York, NY, *IBM T.J. Watson Research Center, Yorktown Heights, NY	671
9:20 am 22.3	Mutual Injection Pulling Between Oscillators , B. Razavi, University of California, Los Angeles, CA	675

9:45 am **BREAK**

Session 23 – Advanced Technology Developments and Fabrication Challenges

Pine Ballroom, Wednesday Morning, September 13

Chair: Alvin Loke Co-Chair: David Sunderland

This session of Invited papers covers CMOS scaling, advanced structures and packaging for high-performance digital and RF applications, as well as competing technologies that overcome present-day limitations of conventional CMOS.

8:00 am	Introduction	
8:05 am 23.1	Technologies for (sub-) 45nm Analog/RF CMOS - Circuit Design Opportunities and Challenges (INVITED PAPER) , S. Decoutere, P. Wambacq, V. Subramanian, J. Borremans and A. Mercha, IMEC, Leuven, Belgium	679

Session 24 – Modeling for RF

Cedar Ballroom, Wednesday Morning, September 13

Chair: Colin McAndrew Co-Chair: Yuhua Cheng

This session presents developments in modeling of noise, inductors and gate resistance in advanced RF processes, and new research in injection-locked oscillators.

8:00 am	Introduction	
8:05 am 24.1	Compact modeling of noise in CMOS (INVITED PAPER) , A. Scholten, R. van Langevelde, L. Tiemeijer and D. Klaassen, Philips Research Europe, Eindhoven, The Netherlands	711
8:55 am 24.2	A Scalable Model Methodology for Octagonal Differential and Single-Ended Inductors , V. Blaschke and J. Victory, Jazz Semiconductor, Newport Beach CA	717
9:20 am 24.3	Measurement of Inductive Coupling Effect on Timing in 90nm Global Interconnects , Y. Ogasahara, M. Hashimoto and T. Onoye, Osaka University, Suita, Japan	721
9:45 am	BREAK	
10:00 am 24.4	A Novel Monitoring Method of RF Characteristics Variations for Sub-0.1µm MOSFETs with Precise Gate-resistance Model , A. Tanabe, K. Hijioaka and Y. Hayashi, NEC Corporation, Kanagawa, Japan	725
10:25 am 24.5	Sizing Ground Taps to Minimize Substrate Noise Coupling in RF LNAs , A. Sundaresan, T. Fiez and K. Mayaram, Oregon State University, Corvallis, OR	729
10:50 am 24.6	First-Harmonic Injection-Locked Ring Oscillators , B. Mesgarzadeh and A. Alvandpour, Linkoping University, Linkoping, Sweden	733

11:15 am 24.7	Analysis of Oscillators Locked by Large Injection Signals: Generalized Adler's Equation and Geometrical Interpretation , A. Mirzaei, M. Heidari and A. Abidi, University of California, Los Angeles, CA	737	2:25 pm 26.3	A 36Gb/s ACCI Multi-Channel Bus using a Fully Differential Pulse Receiver , L. Luo*, J. Wilson, S. Mick, J. Xu, L. Zhang, E. Erickson and P. Franzon, North Carolina State University, Raleigh, NC, *Rambus, Inc., Chapel Hill, NC	773
11:40 am 24.8	Rigorous Analytical/Graphical Injection Locking Analysis of Two-Port Negative Resistance Oscillators , T. Mei and J. Roychowdhury, University Minnesota, Twin Cities, MN	741	2:50 pm 26.4	900MHz to 1.2GHz Two-Phase Resonant Clock Network with Programmable Driver and Loading , J-Y. Chueh, V. Sathe and M. Papaefthymiou, University of Michigan, Ann Arbor, MI	777
Session 25 – PLLs and DLLs Fir Ballroom, Wednesday Morning, September 13 Chair: Eric Naviasky Co-Chair: Shahriar Mirabbasi			3:15 pm	BREAK	
This session covers advances in the design of low noise/spurious PLLs and DLLs for frequency generation and clock recovery.			3:35 pm 26.5	Clock Generation and Distribution Using Traveling-Wave Oscillators with Reflection and Regeneration , R. Wang, C-K. Koh, B. Jung and W. Chappell, Purdue University, West Lafayette, IN	781
9:55 am	Introduction		4:00 pm 26.6	Injection-Locked Clocking: A New GHz Clock Distribution Scheme , L. Zhang, B. Ciftcioglu, M. Huang and H. Wu, University of Rochester, Rochester, NY	785
10:00 am 25.1	A Digital PLL with 5-Phase Digital PFD for Low Long-Term Jitter Clock Recovery , T.Y. Oh, S-H. Yi, S-H Yang, B-C. Lim and K-T. Hong, LG Electronics, Seoul, Korea	745	Session 27 – Wireless Receivers Fir Ballroom, Wednesday Afternoon, September 13 Chair: Stefan Drude Co-Chair: Ranjit Gharpurey		
10:25 am 25.2	Adaptive-Bandwidth Mixing PLL/DLL Based Multi-Phase Clock Generator for Optimal Jitter Performance , A. Tan and G-Y. Wei, Harvard University, Cambridge, MA	749	In this session implementations for advanced radio receivers that address the challenges of modern communication systems will be presented.		
10:50 am 25.3	A Low Jitter Multi-Phase PLL with Capacitive Coupling , J.Y. Park and M. Flynn, University of Michigan, Ann Arbor, MI	753	1:30 pm	Introduction	
11:15 am 25.4	A 150MHz-400MHz DLL-Based Programmable Clock Multiplier with -70dBc Reference Spur in 0.18µm CMOS , P. Maulik and D. Mercer, Analog Devices, Wilmington, MA	757	1:35 pm 27.1	Digital RF Processor Techniques for Single-Chip Radios (INVITED PAPER) , B. Staszewski, K. Muhammad and D. Leipold, Texas Instruments, Dallas, TX	789
11:40 am 25.5	An Anti-Harmonic Locking, DLL Frequency Multiplier with Low Phase Noise and Reduced Spur , Q. Du, J. Zhuang and T. Kwasniewski, Carleton University, Ottawa, Canada	761	2:25 pm 27.2	A 1.5V 0.7-2.5GHz CMOS Quadrature Demodulator for Multi-Band Direct-Conversion Receivers , N. Poobuapheun, W-H. Chen, Z. Boos* and A. Niknejad, University of California, Berkeley, CA, *Infineon Technologies, Munich, Germany	797
Session 26 – Clocking and Data Recovery Oak Ballroom, Wednesday Afternoon, September 13 Chair: Makoto Takamiya Co-Chair: Jackie Snyder			2:50 pm 27.3	A 1.5-V CMOS Receiver Front-End for 9-Band MB-OFDM UWB System , S. Lou, H. Zheng and H. Luong, The Hong Kong University of Science and Technology, Hong Kong	801
This session presents novel GHz clock distribution techniques, low power oscillators, and AC coupled interconnects.			3:15 pm	BREAK	
1:30 pm	Introduction		3:35 pm 27.4	A Distributed RF Front-End for UWB Receivers , A. Safarian, L. Zhou and P. Heydari, University of California, Irvine, CA	805
1:35 pm 26.1	Integrated VCO Design for MICS Transceivers , A. Tekin, M. Yuce* and W. Liu, University of California at Santa Cruz, Santa Cruz, CA, *The University of Newcastle, Callaghan, Australia	765	4:00 pm 27.5	A Fully-Integrated 0.11µm CMOS Digital Low-IF DVB-S2 Satellite TV Dual Tuner SOC , A. Maxim, R. Poorfard, R. Johnson, P. Crawley, J. Kao, Z. Dong, M. Chennam, T. Nutt and D. Trager, Silicon Inc., Nashua, NH	809
2:00 pm 26.2	A 0.8V 1.52MHz MSVC Relaxation Oscillator with Inverted Mirror Feedback Reference for UHF RFID , R. Barnett and J. Liu*, Texas Instruments, Dallas, TX, *University of Texas at Dallas, Richardson, TX	769			

Session 28 – High Speed Analog

Pine Ballroom, Wednesday Afternoon, September 13

Chair: Yusuf Haque Co-Chair: David Rich

This session presents advances in on chip noise suppression, improvements on filter tuning and linearity, temperature sensing techniques, dc and ac amplifier performance and low noise oscillator.

1:30 pm	Introduction	
1:35 pm 28.1	Active On-Die Suppression of Power Supply Noise , G. Keskin, X. Li and L. Pileggi, Carnegie Mellon University, Pittsburgh, PA	813
2:00 pm 28.2	A Fully Integrated DC/DC Converter for Tunable RF filters , M. Bouhamame, J. Turret, L. Lococo, S. Toutain* and O. Pasquier*, Philips Semiconductors, Caen, France, *Institut de Recherche en Electronique et Electrotechnique de Nantes Atlantique	817
2:25 pm 28.3	A Time Domain Mixed-Mode Temperature Sensor with Digital Set-Point Programming , P. Chen, C-C. Chen, T-K. Chen and S-W. Chen, National Taiwan University of Science and Technology, Taipei, Taiwan	821
2:50 pm 28.4	A Unity-Gain Buffer with Reduced Offset and Gain Error , G. Xing, S. Lewis* and T. Viswanathan**, Marvell Semiconductor, *University of California, Davis, CA, **University of Texas, Dallas, TX	825
3:15 pm	BREAK	
3:35 pm 28.5	A 19-GHz Broadband Amplifier Using a gm-Boosted Cascode in 0.18-um CMOS , M. Hossain and A. Chan Carusone, University of Toronto, Ottawa, Canada	829
4:00 pm 28.6	A 0.6V Highly Linear Switched-R-MOSFET-C Filter , P. Kurahashi, P. Hanumolu, G. Temes and U-K. Moon, Oregon State, Corvallis, OR	833
4:25 pm 28.7	Fast Automatic Tuning of Channel Selection Filters Based on Phase Delay Calibration , K. Kagoshima, S. Kawama, S. Toyoyama and K. Iizuka, Sharp Corporation, Nara, Japan	837
4:50 pm 28.8	A Low Phase Noise 100MHz Silicon BAW Reference Oscillator , K. Sundaresan, G. Ho, S. Pourkamali and F. Ayazi, Georgia Institute of Technology, Atlanta, GA	841

Session 29 – Modeling and EDA Challenges in Nano-CMOS

Cedar Ballroom, Wednesday Afternoon, September 13

Chair: Yuhua Cheng Co-Chair: Hidetoshi Onodera

This session discusses and reviews modeling and EPA challenges in nano-scale CMOS technologies. The impact of variabilities on device and circuit performances will also be covered.

1:30 pm	Introduction	
1:35 pm 29.1	EDA Challenges in Nano-scale Technology (INVITED PAPER) , J. Kawa, C. Chiang and R. Camposano, Synopsys, Inc., Mountain View, CA	845
2:25 pm 29.2	Statistical and Corner Modeling of Interconnect Resistance and Capacitance , N. Lu, IBM Semiconductor Research and Development Center, Essex Junction, VT	853
2:50 pm 29.3	Experimental Verification of Simulation Based Yield Optimization for Power-On Reset Cells , G. Rappitsch, O. Eisenberger, B. Obermeier*, A. Ripp* and M. Pronath*, austriamicrosystems AG, Unterpremstatten, Austria, *MunEDA GmbH, Munich, Germany	857
3:15 pm	BREAK	
3:35 pm 29.4	Measurement Results of Delay Degradation Due To Power Supply Noise Well Correlated With Full-Chip Simulation , Y. Ogasahara, T. Enami, M. Hashimoto, T. Sato* and T. Onoye, Osaka University, Suita, Japan, *Tokyo Institute of Technology, Yokohama, Japan	861
4:00 pm 29.5	Delay Variation Analysis in Consideration of Dynamic Power Supply Noise Waveform , M. Fukazawa and M. Nagata, Kobe University, Kobe, Japan	865
4:25 pm 29.6	Crosstalk Reduction with Nonlinear Transmission Lines for High-Speed VLSI System , J. Kim, W. Ni and E. Kan, Cornell University, Ithaca, NY	869