

**2006 International Conference
On Design & Test
Integrated Systems in
Nanoscale Technology**

**La Marsa, Tunisia
5-7 September 2006**



**IEEE Catalog Number:
ISBN:**

**06EX1441
0-7803-9726-6**

**Copyright © 2006 by The Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republications permission, write to IEEE Copyrights Manager, IEEE Operations Center, 445 Hoes Lane, Piscataway, New Jersey USA 08854. All rights reserved.

IEEE Catalog Number: 06EX1441
ISBN: 0-7803-9726-6
Library of Congress: 2006927935

Additional Copies of This Publication Are Available from:

IEEE Service Center
445 Hoes Lane
Piscataway, NJ 08854
IEEE Service Center
445 Hoes Lane
Piscataway, NJ 08854
Phone: (800) 678-IEEE
 (732) 981-1393
Fax: (732) 981-9667
E-mail: customer-service@ieee.org

Table of Contents

Design and Implementation of An 11-bit Non-linear Interpolation DAC.....	1
<i>S. M. Eisa, K. A. Shehata, H. F. Ragai</i>	
Reliability of Active RF Filters in Nanoscale Region.....	5
<i>Enjun Xiao</i>	
TRANSACTION LEVEL MODELING OF AN OSI-LIKE LAYERED NOC	9
<i>Salaheddine Hamza Sfar, Imed E. Bennour, Rached Tourki</i>	
Hybrid fault simulation with compiled and event-driven methods.....	14
<i>Kenjiro Taniguchi, Hideo Fujii, Seiji Kajihara, Xiaoqing Wen</i>	
Two dimensional model for lateral photodiode.....	18
<i>A. Alexandre, F. Dadouche, P. Garda</i>	
Synthesis of Symmetric Functions Using Quantum Cellular Automata.....	23
<i>Hafizur Rahaman, Biplab K Sikdar, Debesh K. Das</i>	
High Frequency CCII Based Oscillators and Multifunction Filters	29
<i>S. Ben Salem, D. Sellami Masmoudi, M. Fakhfakh, M. Loulou, N. Masmoudi</i>	
Folded Cascode OTA Design for Wide Band Applications.....	33
<i>Houda Daoud, Samir Ben Salem, Sonia Zouari, Mourad Loulou</i>	
Dual Band CMOS LNA Design With Current Reuse Topology.....	37
<i>Meriam Ben Amor, Ahmed Fakhfakh, Hassene Mnif, Mourad Loulou</i>	
Design of enhanced performances CMOS RF mixers suitable for multi-standards receiver	42
<i>Skandar Douss, Mourad Loulou</i>	
Trends in Tests and Failure Mechanisms in Deep Sub-Micron Technologies.....	46
<i>Said Hamdioui, Zaid Al-Ars, Lotfi Mhamdi, Georgi Gaydadjiev, Stamatias Vassiliadis</i>	
A Distributed BIST Architecture Enabling Extended Sharing and Debug Capabilities.....	52
<i>Laurent Vachez, Lotfi Ben Ammar</i>	
Average Modeling of DC-DC and DC-AC converters including Semiconductor Device Non-linearities	57
<i>Slim Abid, Anis Ammous</i>	
SRAM Dedicated PCMs For Leakage Characterization in Nanometer CMOS Technologies	63
<i>Sylvain Léomant, Arnaud Turier, Lotfi Ben Ammar, Amara Amara</i>	
Design of Power-controlled Class1 Bluetooth CMOS Power Amplifier	69
<i>Aida A. El-sabban, Hani F. Ragai</i>	
A 863-870-Mhz Spread-Spectrum Direct Conversion Receiver Design for Wireless Sensor.....	73
<i>H. Trabelsi, Gh. Bouzid, Y. Jaballi, L. Bouzid, F. Derbel, Mohamed Masmoudi</i>	
TESTING SYSTEM-IN-PACKAGE WIRELESSLY	77
<i>Serge Bernard, David Andreu, Marie-Lise Flottes, Philippe Cauvet, Hervé Fleury, Fabrice Verjus</i>	
Universal Low/Medium Speed I2C-Slave Transceiver: a Detailed VLSI Implementation	82
<i>A.K. Oudjida, A. Liacha, D. Benamrouche, M. Goudjil, R. Tiar, A. Ouchabane</i>	
Physical Verification of Microelectronics fiMask Patternsfl with Calibre SVRF Rule Files.....	89
<i>Salager Laurent</i>	
FPGA Implementation of Programmable Pulse Mode Neural Network with on Chip Learning	92
<i>Alima Damak, Mohamed Krid, Dorra Sellami Masmoudi, Nabil Derbel</i>	
Implementation of Scalable Embedded FPGA for SOC	98
<i>Hayder Mrabet, Zied Marrakchi, Habib Mehrez, Andre Tissot</i>	
Theoretical and Numerical modeling of a CMOS micromachined acoustic sensor.....	102
<i>B. Mezghani, K. Haboura, F. Tounsi, S. Smaoui, S. El-Borgi, S. Choura, M. Masmoudi</i>	
Method for Embedded Application Prototyping based on SoC Platform and Architecture Model	106
<i>Y. Aoudni, G. Gogniat, Kais Loukil, J.L. Philippe, M. Abid</i>	

Table of Contents

HARDWARE/SOFTWARE APPROACHE FOR THE FPGA IMPLEMENTATION OF A FUZZY LOGIC CONTROLLER.....	112
<i>Mohamed Slim Masmoudi, Insop Song, Fakhreddine Karray, Mohamed Masmoudi, Nabil Derbel</i>	
Analyzing the Memory Effect of Resistive Open in CMOS Random Logic	117
<i>M. Renovell, M. Comte, I. Polian, P. Engelke, B. Becker</i>	
Automated Design of Microfluidics-Based Biochips: Connecting Biochemistry to Electronics CAD.....	123
<i>Krishnendu Chakrabarty</i>	
SiP Technologies: Perspectives and Challenges	124
<i>P. Cauvet</i>	
Injection Locked Oscillator Based RF Transmitters.....	125
<i>Thomas Finateu, Jean-Baptiste Bégueret, Yann Deval, Franck Badets</i>	
Low Power FPGA-Based Implementation Of Decimating Filters For Multistandard Receiver.....	129
<i>Nadia Khouja, Khaled Grati, Adel Ghazel</i>	
Non-Uniform Sampling Schemes for IF Sampling Radio Receiver.....	134
<i>Manel Ben-Romdhane, Chiheb Rebai, Adel Ghazel, Patricia Desgeys, Patrick Loumeau</i>	
A Dual-Mode Dual-Standard LNA for DCS1800/W-CDMA Applications	140
<i>C. P. Moreira, E. Kerherve, P. Jarry, D. Belot</i>	
CNTFET Basics and Simulation.....	146
<i>T. Dang, L. Anghel, R. Leveugle</i>	
Design-oriented Compact Models for CNTFETs.....	152
<i>Fabien Pregaldiny, Christophe Lallement, Jean-Baptiste Kammerer</i>	
Analysis of CNTFET physical compact model.....	158
<i>C. Maneux, J. Goguet, S. Frégonèse, T. Zimmer, H. Cazin d'Honincthun, S. Galdin-Retailleau</i>	
CNTFET-based logic circuit design	164
<i>I. O'Connor, J. Liu, F. Gaffiot</i>	
Transcutaneous Power And High Data Rate Transmission For Biomedical Implants	170
<i>Ghazi Ben Hmida, Mohamed Dhieb, Hamadi Ghariani, Mounir Samet</i>	
A high-level timing model for variability characterization of interconnect circuits.....	175
<i>Miguel Miranda, Antonis Papanikolaou, Hua Wang, Marios Kaspiris, Patrick David, Francky Catthoor</i>	
Supply voltage glitches effects on CMOS circuits.....	181
<i>Anissa Djellid-Ouar, Guy Cathebra, Frédéric Bancel</i>	
Dependability Analysis: Performance Evaluation of Environment Configurations.....	186
<i>P. Vanhauwaert, R. Leveugle, P. Roche</i>	
MODELING OF PIXEL SENSORS FOR IMAGE SYSTEMS WITH VHDL-AMS	192
<i>F. Dadouche, A. Pinna, P. Garda, A. Alexandre</i>	
An On-Line Software-Based Self-Test Framework for Microprocessor Cores	197
<i>Alfredo Benso, Alberto Bosio, Paolo Prinetto, Alessandro Savino.</i>	
A Low-Power Oscillation Based LNA BIST Scheme.....	203
<i>J. Machado da Silva</i>	
Design of secure digital communication systems using DCSK chaotic modulation	208
<i>M. A. Ben Farah, A. Kachouri, M. Samet</i>	
An Application Specific NoC Mapping for Optimized Delay	213
<i>Wenbiao Zhou, Yan Zhang, Zhigang Mao</i>	
CMOS Leakage Power at Cell Level.....	218
<i>Mendoza R., Ferré A., Balado L., Figueras J.</i>	

Table of Contents

Performance of adaptive filter used in CDMA system for Multiple Access Interference Suppressing.....	224
<i>H. Marouane, A. Benabdennabi, A. Kachouri, L. Kamoun</i>	
Two-Pattern Generation Based On Accumulators with 1's Complement Adders.....	227
<i>I. Voyiatzis, C. Efstathiou</i>	
Accumulator - based compression in Symmetric Transparent RAM BIST	232
<i>Ioannis Voyiatzis</i>	
Design and Optimisation of RF Filters for Multistandard RF Sub-sampling Receiver	238
<i>Rim Barrak, Adel Ghazel, Fadhel Ghannouchi</i>	
Implementation of a Neural Network Module for Fourth Generation Mobile Equipments.....	243
<i>Damergi Emir, Ben Rabaa Abdellatif, Bouallegue Ammar</i>	
Comparison of addition structures synthesis over commercial FPGAs.....	249
<i>Miguel A. Sacristán, Victoria Rodellar, Antonio Díaz</i>	
Hardware Design and Implementation of Digital Controller for Parallel Active Filters	254
<i>Ben Othman Slim, Braham Ahmed, Ben Saoud Slim</i>	
Implementation of a fuzzy logic tracking path algorithm on a Field Programmable Gate Array	258
<i>H. Abdelkrim, S. Ben Saoud</i>	
AUTOMATED BIST-BASED DIAGNOSTIC SOLUTION FOR SOPC.....	262
<i>Alireza Sarvi, Jenny Fan</i>	
Minimizing Peak Power Consumption during Scan Testing: Test Pattern Modification with X Filling Heuristics.....	267
<i>Nabil Badereddine, Patrick Girard, Serge Pravossoudovitch, Christian Landrault Arnaud Virazel</i>	
A Low-Power Design Methodology for Single-Stage Operational Amplifiers	273
<i>Hamed Aminzadeh, Mohammad Danaie, Reza Lotfi</i>	
Speeding up simulation time in EEPROM memory designs.....	279
<i>H. Aziza, B. Delsuc, J.M. Portal, D.Nee</i>	
Dynamic Routing Algorithm for Avoiding Hot Spots in On-chip Networks.....	283
<i>A. Sobhani, M. Daneshalab, M. H. Neishaburi, M. D. Mottaghi, Ali Afzali-Kusha, O. Fatemi, Z. Navabi</i>	
Defect and Fault Tolerant Cell Architecture for Feasible nanoelectronic designs.....	288
<i>Ferran Martorell, Antonio Rubio</i>	
A New Synchronization Policy between PSL Checkers and SystemC designs at Transaction Level.....	294
<i>Younes Lahbib, Mohamed-Arafet Ghrab, Maher Hechkel, Frank Ghenassia, Rached Tourki</i>	
Verification Flow Optimization using an Automatic Coverage Driven Testing Policy	300
<i>Younes Lahbib, Oualid Missaoui, Maher Hechkel, Dhafer Lahbib, Badreddine Mohamed-Yosri3, Rached Tourki</i>	
Application of Neural Network to the Synthesis of Linear Antenna Array's Radiance Diagram.....	306
<i>Ghayoula Ridha, Hajlaoui Elamjed, Glaoui Mohamed, Gharsallah Ali, Korkobi Talel</i>	
Additivity of Capacitive and Inductive Coupling in Submicronic Interconnects	310
<i>J.E. Lorival, D. Deschacht, Y. Quere, T. Le Gouguec, F. Huret</i>	
A non-volatile Flip-Flop in Magnetic FPGA chip.....	315
<i>W.Zhao, E. Belhaire, V. Javerliac, C. Chappert, B. Dieny</i>	
Accelerating the Rijndael Algorithm using Custom Instructions Capability of Nios II in ODYSSEY	319
<i>R. Iraj, S. Hessabi, E. K. Moghadam</i>	
Mixed-Signal Simulation & Test Generation	324
<i>Martine Dufils, Jean-Louis Carbonero, Philippe Planelle, Philippe Raynaud</i>	
ANALYSIS OF MULTILAYER MICROSTRIP FILTER BY WAVE CONCEPT ITERATIVE PROCESS.....	330
<i>Hajlaoui El Amjed, Glaoui Mohamed, Trabelshi Hichem</i>	

Table of Contents

Estimation of test metrics for multiple analogue parametric deviations	334
<i>Ahcene Bounceur, Salvador Mir, Emmanuel Simeu, Luis Rolindez</i>	
Magnetic Domain Wall Logic Requires New Synthesis Methodologies	340
<i>Jacques-Olivier Klein, Eric Belhaire, Claude Chappert, Russell Cowburn, Dan Read, Dorothée Petit</i>	
Analysis of Timing Jitter in Inverters Induced by Power-Supply Noise.....	344
<i>Adam Strak, Hannu Tenhunen</i>	
A SystemC AMS Model of an I2C Bus Controller.....	348
<i>M. Alassir, J. Denoulet, O. Romain, P. Garda</i>	
MDCT IP Core Generator.....	353
<i>Marcel Balaz, Peter Malik, Tomas Pikula, Martin Simlastik</i>	
Performances evaluation and enhancement of MPEG4 transmission over IEEE 802.11 WLAN.....	357
<i>Neila Moussa, Adel Soudani, Rached Tourki</i>	
Performances comparison between Multilevel hierarchical and Mesh FPGA interconnects.....	361
<i>Zied Marrakchi, Hayder Mrabet, Habib Mehrez</i>	
Low Power Digital design using modified GDI method	367
<i>Padmanabhan Balasubramanian, Johince John</i>	
Simultaneous Delay optimization and Depth reduction in Logic trees with minimum resources.....	371
<i>Padmanabhan Balasubramanian, Prathibha.P</i>	
EDP optimized Synthesis scheme for Boolean Read-Once functions.....	375
<i>Padmanabhan Balasubramanian, Theja. S</i>	
Power Aware minimization of Complementary Logic functions based on maximal HD.....	379
<i>Padmanabhan Balasubramanian, Sirisha. Y</i>	
An FPGA Hardware implementation of the Rijndael block cipher.....	384
<i>Chorfi Dhoha, Slim Ben Othman, Slim Ben Saoud</i>	
A NOVEL SCALABLE SPIKING PIXEL ARCHITECTURE FOR DEEP SUBMICRON CMOS TECHNOLOGIES.....	388
<i>Farid Boussaid, Chen Shoushun, Amine Bermak</i>	
Behavioral Synthesis Technique for Flexible IP's Communications.....	393
<i>Smiri Kamel, Imed Bennour, Adel Baganne, Rached Tourki, Abderrazek Jemai</i>	
High Q-VCO with Low phase noise for Communications applications.....	397
<i>Nabil Boughghanmi, Dalenda Ben Issa, Abdennaceur Kachouri, Mounir Samet</i>	
Embedded Flash Testing: Overview and Perspectives.....	401
<i>O. Ginez, J.-M. Daga, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel</i>	
New Generic GALS NoC Architectures With Multiple QoS.....	407
<i>Mounir Zid, Abdelkrim Zitouni, Adel Baganne, Rached Tourki</i>	
Modulation/Demodulation Techniques With FPGA's Architecture to improve OFDM Wireless Underwater Communication Transceiver	412
<i>Nejah Nasri, Helmi Ben Hnia, Abdennaceur Kachouri, Mahmoud Abdellaoui, Mounir Samet</i>	
Ground Bounce Modelling for Digital Gigascale Integrated Circuits.....	416
<i>M. Pons, F. Martorell, X. Aragoes, F. Moll, A. Rubio</i>	