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**Betting the Ranch on
Compound Semiconductors**

**TECHNICAL
DIGEST
2006**

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2006 IEEE Compound Semiconductor Integrated Circuit Symposium

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Reconfigurable and Tunable Networks

Moderators: Peter Zampardi, *Skyworks Solutions, Inc.*
Charles Campbell, *TriQuint Semiconductor*

Tunable or reconfigurable circuits are becoming a critical element in many modern electronics applications. For example, future generation wireless handsets are expected to operate multimode and multiband anywhere in the world. To address this need in a reasonable form factor, reconfiguration of matching networks and filters are highly desirable. Another increasing requirement for portable electronics is that they adapt to the environment they are in to protect the circuit and/or allow operation at reduced power consumption. Finally, these tunable circuits may enable tunable filters, phase shifters, and other circuits or architectures that enable new applications in sensing, defense and communications.

This panel session will discuss the status and state-of-the-art of several proposed technologies for achieving reconfigurable/tunable electrical networks.

Key Points to Discuss:

1. Integration potential with current electronics (on MMIC or package)
2. Reliability and packaging status/concern
3. Technology performance (Tuning range, on/off impedance, operating frequencies, quality factors, required operating voltages)

Panel Members:

Robert York *UCSB/Agile Technologies*
Keith Manssen *Paratek Technologies*
Rik Jos *Philips Semiconductor*
Brandon Pillans *Raytheon*

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Compound Semiconductor MOSFETs: Fact or Fiction? And who cares?

Moderators: Mike Golio, *HVVi Semiconductor*
Sorin Voinigescu, *University of Toronto*

This panel session will examine the recent resurgence of interest in oxide on compound semiconductor devices. Panelists will be asked to address a number of critical questions for this technology. Can reliable, manufacturable oxides be grown on compound semiconductors? Will performance advantages be sufficient to make these technologies commercially viable? What applications might benefit from compound semiconductor oxide devices and what is the competition?

Panel Members:
Matthias Passlack *Freescale Semiconductor*
David Braddock *OSEMI, Inc.*
Patrick Fay *University of Notre Dame*

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Can we trust parasitic extractors at high frequencies?
Moderators: Douglas S. McPherson, *ITT A/CD*
Jaesik Lee, *Lucent Technologies*

Parasitic extraction tools are indispensable for the design of robust integrated circuits. Developed primarily for verifying the correct operation of digital circuits where the inputs and outputs are discrete on or off signals, the same tools have proven equally successful at

predicting the behavior of AMS and RFIC circuits as well. However, the emergence of ultra-high-speed communications and sensor applications presents a new and much more demanding challenge that cannot be solved by mere RC extraction. This is because the frequencies of interest now extend into the millimeter-wave range and the technologies exhibit minimum features of 90 nm or less. In recognition of this fact, tool developers have enhanced their parasitic extraction products to include full RLC extraction, as well as cross-coupling and substrate effects. Although these enhancements are a welcome addition to the high-speed designer's tool kit, how accurate is the parasitic extractor for predicting circuit performance at data rates of 40+ Gb/s or frequencies of 60+ GHz? Can users be confident that the tools have been validated against foundry silicon at comparable speeds? Can parasitic extractors replace the 3D electromagnetic-field simulator or will it simply be incorporated? The panelists will provide their own perspectives and articulate how parasitic extraction tools will or should evolve to meet the new challenges. The issues of speed, complexity, reliability, and cost will form the basis of the ensuing discussion.

Panel Members:

Baribrata Biswas *Synopsys, Inc.*
 Matt D'Amore *Northrop Grumman Corporation*
 Mehran Mokhtari *Vitesse Semiconductor Corporation*
 Jean-Olivier Plouchart *IBM*
 Carey Robertson *Mentor Graphics Corp.*
 Rachid Salik *Cadence Design Systems, Inc.*

SESSION M

Wednesday, November 15th, 2006, 1:00 p.m. – 2:20 p.m.

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PA Technology for WiMAX - Can challengers take on LDMOS at 3.5GHz and beyond ?

Moderators: Rik Jos, *Philips Semiconductors*
 Walter Wohlmuth, *RFMD*

A number of technologies and products are competing for insertion within WiMAX systems currently under development. The high-power performance characteristics, power amplifier linearity and associated linearization techniques, and improved reliability in the field of GaN FETs and high-voltage GaAs FETs

have opened up the field of potential technologies to be used in these systems. LDMOS, however, is a well-entrenched technology for high-power applications that continues to march forward in regards to performance.

These panelists will discuss and debate the merits and demerits of the competing technologies and their product performance characteristics. Systems requirements and technology drivers from WiMAX vendors will be presented and discussed. Development trends towards higher functionality, increased PAE at back-off power levels, commercial aspects such as time to market and cost per Watt, and roadmaps for further products as well as cost reduction will be debated.

Panel Members:

Pierre Piel, *Motorola (LDMOS and High-voltage GaAs FETs)*
 Korne Vennema, *Philips (LDMOS)*
 Bill Pribble, *Cree (GaN on SiC HEMTs)*
 Matthew Poulton, *RFMD (GaN on SiC HEMTs)*
 Toshi Kikkawa, *Fujitsu (GaN on SiC HEMTs)*
 Chris Rauh, *Nitronex (GaN on Silicon HEMTs)*
 TBD, *WiMAX forum representative*

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SYMPOSIUM AT A GLANCE

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REGISTRATION (Short Course & Primer Course Only)

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LDMOS at 3.5GHz and beyond ?

SESSION N: Wide Bandgap Technology

Close of Symposium

Visit us on the World-Wide Web at: <http://www.csics.org/>

Saturday, November 11th, 2006

6:00 p.m. – 8:00 p.m.

Tower View Foyer

Sunday, November 12th, 2006

7:00 a.m. – 8:00 a.m.

Tower View Foyer

7:00 a.m. – 8:00 a.m.

Tower View Foyer

8:30 a.m. – 3:45 p.m.

Room 217 C

8:30 a.m. – 3:45 p.m.

Room 217 D

8:00 a.m. – 5:00 p.m.

Room 213

12:00 p.m. – 1:30 p.m.

Room 217 A

12:00 p.m. – 1:30 p.m.

Room 217 B

3:00 p.m. – 8:00 p.m.

Tower View Foyer

4:00 p.m. – 7:00 p.m.

Room 217 C

6:00 p.m. – 8:00 p.m.

The Grotto

Monday, November 13th, 2006

7:00 a.m. – 5:00 p.m.

Tower View Foyer

7:00 a.m. – 8:00 a.m.

Tower View Foyer

8:00 a.m. – 8:30 a.m.

Room 217 A & B

8:30 a.m. – 11:30 a.m.

Room 217 A & B

1:00 p.m. – 2:20 p.m.

Room 217 A

1:00 p.m. – 3:00 p.m.

Room 217 D

3:10 p.m. – 4:30 p.m.

Room 217 A

3:10 p.m. – 4:40 p.m.

Room 217 D

5:00 p.m. – 7:00 p.m.

Ballroom C1-C2

Tuesday, November 14th, 2006

7:00 a.m. – 5:00 p.m.

Tower View Foyer

7:00 a.m. – 4:00 p.m.

Ballroom C1-C2

7:00 a.m. – 8:00 a.m.

Ballroom C1-C2

8:00 a.m. – 9:50 a.m.

Room 217 A

8:00 a.m. – 9:30 a.m.

Room 217 D

10:10 a.m. – 11:40 a.m.

Room 217 A

10:10 a.m. – 11:20 a.m.

Room 217 D

11:10 a.m. – 1:30 p.m.

Ballroom C1-C2

2:00 p.m. – 3:30 p.m.

Room 217 A

2:00 p.m. – 3:40 p.m.

Room 217 D

7:00 p.m. – 10:00 p.m.

Rio Cibolo Ranch

Wednesday, November 15th, 2006

7:00 a.m. – 12:00 p.m.

Tower View Foyer

7:00 a.m. – 8:00 a.m.

Tower View Foyer

8:00 a.m. – 9:50 a.m.

Room 217 A

8:00 a.m. – 9:00 a.m.

Room 217 D

10:10 a.m. – 11:30 a.m.

Room 217 A

10:10 a.m. – 11:40 a.m.

Room 217 D

1:00 p.m. – 2:20 p.m.

Room 217 A

1:00 p.m. – 2:30 p.m.

Room 217 D

3:00 p.m. – 5:00 p.m.

Room 217 A

5:00 p.m.