

2006 International SiGe Technology and Device Meeting

———— ISTDM 2006 ————



Conference Digest of the Third International
Silicon Germanium Technology and Device
Meeting (ISTDM 2006)

Princeton University, Princeton, NJ USA
May 15th – May 17th, 2006



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Technical Program ISTDM 2006

Monday, May 15th

Session 1: Plenary Session – Friend 101

Session Chair: Eugene Fitzgerald

9:00 –9:15 Welcome and Introduction

9:15 –9:55 1.1 **Discontinuous Innovation: Strained Silicon Technology**, Gary L. Patton; IBM Systems and Technology Group, 2070 Route 52, Hopewell Junction, NY, 12533 USA 1

9:55 – 10:35 1.2 **Silicon Microphotonics: Hardware for the Information Age**, Lionel C Kimerling; Massachusetts Institute of Technology, 77 Massachusetts Ave, Cambridge, MA, 02139 USA 3

Break

10:35 AM – 10:55 AM, Friend 113

[Parallel Session]

Session 2A: Strained Si FET/CMOS and Technology

10:55 AM – 11:55 AM, Friend 101

Session Chair: Minjoo Lee

10:55: 2A.1 **Performance Boosting of Peripheral Transistor for High Density 4Gb DRAM Technologies by SiGe Selective Epitaxial Growth Technique**, I. S. Jung¹; S.-G. Lee¹; D.-H. Lee¹; E.-C. Lee²; W. Kim³; P.K. Kang¹, Y.-H. Son¹; S.-K. Kang¹; J.-B. Kim¹; Y.-P. Kim¹; K.-H. Lee¹; M.-G. Kang¹; H. Kim¹; J.-W. Lee¹; Y.G. Shin¹; U.-I. Chung¹ and J.T. Moon¹; ¹ Process Development Team, Memory Division, Semiconductor Business, Samsung Electronics Co., Ltd. 449-711 San#24 Nongseo-Dong, Giheung-Gu, Yongin-City, Gyeonggi-Do, Korea; ² Technology Development Team, Memory Division, Semiconductor Business, Samsung Electronics Co., Ltd. Korea; ³ Device Research Team, Memory Division, Samsung Electronics Co., Ltd. Korea 4

11:10: 2A.2 **Thick-Strained-Si/SiGe CMOS Technology with Selective-Epitaxial-Si Shallow-Trench Isolation (SES-STI)**, M. Miyamoto¹; N. Sugii²; Y. Yoshida¹, Y. Hoshino³; Y. Kimura², M. Kondo³ and K. Ohnishi³; ¹ Micro Device Division, Hitachi, Ltd., 16-3, Shinmachi 6-chrome, Ome-shi, Tokyo 198-8512 Japan; ² Central Research Laboratory, Hitachi, Ltd.; ³ Renesas Technology Corp. Japan 6

11:25: 2A.3 **p-n Junction Leakage Current in Strained-Si/SGOI Diodes**, A. Tanabe¹; T. Numata¹; T. Tezuka¹; N. Hirashita¹; S. Takagi²; ¹ MIRAI, Association of Super-Advanced Electronics Technology (ASET), 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 212-8582, Japan; ² MIRAI, Advanced Semiconductor Research Center (ASRC), National Institute of Advanced Industrial Science and Technology (AIST) Japan 8

11:40: 2A.4 **Impact of Etching Depth on the Leakage Current of Recessed SiGe Junctions**, M. Bargallo Gonzalez¹; G. Eneman^{1,2,3}; P. Verheyen¹; C. Claeys^{1,2}; A. Benedetti¹; H. Bender¹; K. De Meyer^{1,2}; E. Simoen¹; R. Schreutelkamp⁴; L. Washington⁴; F. Nouri⁴; ¹IMEC, Kapeldreef 75, B-3001, Leuven, Belgium; ² ESAT-INSYS, K.U. Leuven, Kasteelpark Arenberg 10, 3001 Heverlee, Belgium ³Research Assistant of The Fund for Scientific Research – Flanders, Belgium, ⁴Applied Materials, Sunnyvale, CA, USA 10

[Parallel Session]

Session 2B: Germanium Device Technology

10:55 AM – 11:55 AM, CS 104

Session Chair: Roger Loo

10:55: 2B.1 **Germanide phase formation and texture**, Simon Gaudet¹; Christian Lavoie^{1,3}; Christophe Detavernier²; Patrick Desjardins¹; ¹Departement de Génie physique, Ecole Polytechnique de Montreal, P.O. Box 6079, Station Centre-Ville, Montreal, Quebec, H3C 3A7, Canada; ²Department of Solid State Physics, Ghent University, Ghent, Belgium; ³IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, USA **12**

11:10: 2B.2 **Accurate Modeling of Average Phosphorus Diffusivities in Germanium after Long Thermal Anneals**, Malcolm Carroll; R. Koudelka; Sandia National Labs, P. O. Box 5800, M. S. 1077, Albuquerque, NM, 87185, USA **14**

11:25: 2B.3 **Strained Pt Schottky Diodes on n-type Si and Ge**, M. H. Liao¹; S. T Chang²; P. S Kuo¹; H.-T Wu¹; C.-Y Peng¹; C. W Liu¹; ¹Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan R.O.C.; ²Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan R.O.C. **16**

11:40: 2B.4 **Negative Differential Resistance in Ultra-Thin Ge-On-Insulator FETs**, D. Kazazis¹; A. Zaslavsky¹; E. Tutuc²; N.A. Bojarczuk²; S. Guha²; ¹Division of Engineering, Brown University, 182 Hope St., Providence, RI, 02912, USA; ² IBM T. J. Watson Research Center, P.O Box 218, Yorktown Heights, NY, 10598, USA **18**

Lunch

12:00 PM – 1:30 PM, Friend 113

Session 3: Invited: Optoelectronics and Ge FET's

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Session Chairs: Cliff King and Detlev Grützmacher

1:30: 3.1 **Ge/SiGe Quantum Confined Stark Effect Modulators on Silicon**, James S Harris; Yu-Hsuan Kuo; David A.B. Miller; Stanford University, Solid State and Photonics Lab, CISX 328, Stanford, CA, 94305, USA **20**

2:00: 3.2 **Performance and Reliability of SiGe Photodetectors**, Mike Morse¹; Femi Dosunmu²; Yoel Ghetrit³; Gadi Sarid³; ¹ Intel Corporation, 2200 Mission College Blvd, Santa Clara, CA, 95053, USA; ² Intel Corporation, 2200 Mission College Blvd, Santa Clara, CA, 95053, USA; ³ Intel Corporation, S.B. I Park Har Hotzvin, Jerusalem, 91031, Israel **22**

2:30: 3.3 **Ge deep sub-micron HiK/MG pFET with superior Drive compared to Si HiK/MG state-of-the-art reference**, B. De Jaeger¹; B. Kaczer¹; P. Zimmerman²; K. Opsomer³; G. Winderickx³; J. Van Steenberghe³; E. Van Moorhem³; R. Bonzom³; F. Leys³; C. Arena⁴; M. Bauer⁴; C. Werkhoven⁴; M. Meuris⁵; Marc Heyns⁵; ¹IMEC, Kapeldreef 75, B-3001 Leuven, Belgium; ² Intel; ³ IMEC; ⁴ ASM America, 3440 E. University Drive, Phoenix, Ar, 85034; ⁵ IMEC, Belgium **24**

3:00: 3.4 **III-V/Si Device Integration Via Metamorphic SiGe Substrates**, Steven A Ringel¹; Ojin Kwon²; Matthew Lueck¹; John Boeckl³; Eugene Fitzgerald⁴; ¹ Dept. of Electrical and Computer Engineering, The Ohio State University, 2015 Neil Ave, Columbus, OH, 43210, USA; ² Lumileds, Inc., San Jose, CA, 95136, USA; ³ Air Force Research Laboratory, Wright Patterson AFB, Dayton, OH 45433 USA; ⁴ Dept. of Materials and Science and Eng., Massachusetts Institute of Technology, Cambridge, MA 02139, USA **26**

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Session 4A: Optoelectronics

3:50 PM – 4:50 PM, Friend 101

Session Chair: Michael Morse

3:50: 4A.1 **Fast Ge p-i-n photodetectors on Si**, E. Kasper¹; M. Oehme¹; J. Werner¹; M. Jutzi²; M. Berroth²; ¹Institut für Halbleitertechnik, University of Stuttgart, Pfaffenwaldring 47, 70569, Stuttgart, Germany, ²Institut für Elektrische und Optische Nachrichtentechnik, University of Stuttgart, Germany **28**

4:05: 4A.2 **Ge/Si (100) Heterojunction Photodiodes Grown by Low-Energy Plasma-Enhanced CVD**, Giovanni Isella^{1,2}; Johann Osmond¹; Matthias Kummer²; Rolf Kaufmann³; Hans von Kaenel^{1,2}; ¹L-NESS Politecnico di Milano – Polo di Como Via Anzani 52, 22100 Como Italy; ²Epispeed AG Technoparkstrasse 1, 8005 Zurich Switzerland, ³Centre Suisse d'Electronique et de Microtechnique SA Badenerstrasse 569, 8048 Zurich, Switzerland **30**

4:20: 4A.3 **MBE growth and characterization of three-terminal Ge(dot)/SiGe(well) near-infrared photodetectors**, A. Elfving; A. Karim; M. Zhao; G. V. Hansson; W.-X. Ni; Department of Physics, Chemistry and Biology, Linköping University, 581 83 Linköping, Sweden **32**

4:35: 4A.4 **Fabrication of Silicon on Lattice-Engineered Substrate (SOLES) as a Platform for Monolithic Integration of CMOS and Optoelectronic Devices**, Carl L Dohrman; Kamesh Chilukuri; David M Isaacson; Minjoo L Lee; Eugene A Fitzgerald; Department of Materials Science and Engineering, Massachusetts Institute of Technology (MIT), 77 Massachusetts Ave, Rm 13-4154, Cambridge, MA, 02139, USA **34**

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4:05: 4B.2 **Effects of Ambient Conditions in Thermal Treatment for Ge(001) Surfaces on Ge MIS Interface Properties**, Noriyuki Taoka¹; Keiji Ikeda²; Yoshimi Yamashita²; Naoharu Sugiyama²; Shin-ichi Takagi^{1,3}; ¹MIRAI-ASRC, AIST Tsukuba West 7, 16-1, Onogawa, Tsukuba 305-8569, Japan; ²MIRAI-ASET, AIST Tsukuba West 7, 16-1, Onogawa, Tsukuba, 305-8569 Japan; ³The University of Tokyo, 7-3-1 Hongo, Bunkyo- **38**

Ku, Tokyo, 113-8656, Japan

4:20: 4B.3 **Ge nanocrystals metal-oxide-semiconductor capacitors with Ge nanocrystals formed by oxidation of poly-Si_{0.88}Ge_{0.12}**, J. H. Wu; P.W. Li; Dept of Electrical Engineering, National Central University, ChungLi, 32001 Taiwan ROC **40**

4:35: 4B.4 **Thin Germanium-Carbon Layers on Silicon for Metal-Oxide-Semiconductor Devices**, David Q Kelly¹; Isaac Wiedmann¹; Domingo I Garcia Gutierrez²; Miguel Jose Yacaman²; Sanjay K Banerjee¹; ¹ Microelectronics Research Center, UT-Austin, 10100 Burnet Road, Bldg. 160, Austin, TX, 78758, USA, ²Dept. of Chemical Engineering, UT-Austin; 1 University Station MS C0400, Austin, TX 78712 USA **42**

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5P.2 **Proton Radiation Tolerance of SiGe Power HBTs**, Ningyue Jiang¹; Zhenqiang Ma¹; Pingxi Ma²; Marco Racanelli²; ¹ Dept. of Electrical and Computer Engineering, University of Wisconsin-Madison, WI 53706 USA; ² Jazz Semiconductor, Inc. USA **46**

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- 5P.39 **Current Gain of SiGe HBTs Under High Base Doping Concentrations**, Ningyue Jiang; Zhenqiang Ma; Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI, 53706, USA **118**
- 5P.40 **Low-temperature Pre-treatments in Vertical Epitaxial Reactor with Improved Vacuum Load-Lock Chamber**, Jie Wang; Yasuhiro Inokuchi; Yasuo Kunii; Hitachi Kokusai Electric Inc., 2-1 Yasuuchi, Yatsuo-machi, Toyama, 939-2393, Japan **120**
- 5P.41 **Growth of Ultra-uniform B-doped Si/SiGe Multiple Quantum Wells by RTCVD for Mid-IR Applications**, W. Zheng¹; J. C. Sturm¹; C. Gmachl¹; T. Buyuklimanli²; J. Marino²; M. S. Denker²; J. T. Mayer²; ¹ Princeton Institute for the Science and Technology of Materials, Dept. of Electrical Engineering, Princeton University, Princeton, NJ, 08544, USA; ² Evans Analytical Group, 104 Windsor Center, Suite 101, East Windsor, NJ, 08520, USA **122**
- 5P.42 **Bound-to-Continuum Quantum Cascade Emitters for Terahertz Emission**, Douglas J Paul¹; Paul Townsend¹; Stephen A Lynch¹; Ming Zhao²; Wei-Xin Ni²; Jing Zhang³; ¹ University of Cambridge, Cavendish Laboratory, Madingley Road, Cambridge, CB3 0HE, U.K.; ² University of Linköping, Department of Physics and Measurement Technology, Linköping, S-58183, Sweden; ³ Imperial College London, Department of Physics, Blacket Laboratory, London, SW7 2BW, U.K. **124**
- 5P.43 **Integration of selective SiGe epitaxy for source/drain application in MOSFETs**, Henry H Radamson; Julius Hällstedt; Mikael Östling; School of Information and Communication, Royal Institute of Technology (KTH), Isafjordsg. 22-26, Electrum 229, 16640, Kista, Sweden **126**
- 5P.44 **Xenon Difluoride dry etching of Si, SiGe alloy and Ge**, Guangchi Xuan¹; Thomas N Adam^{1*}; John Suehle²; Eugene Fitzgerald³; Pengcheng Lv¹; Nathan Sustersic¹; Matthew Coppinger¹; James Kolodzey¹; ¹ University of Delaware, 140 Evans Hall (ECE Dept.), Newark, DE, 19716, USA; ² National Institute of Standards and technology, Gaithersburg, Maryland 20899; ³ Materials Science and Engineering Dept., MIT, Cambridge, MA, USA; ^{1*} now with IBM Corp., 1101 Kitchawan Road, Route 134/P.O. Box 218, Yorktown, NY 10598 USA **128**
- 5P.45 **Effective Mass Measurement: Influence of Hole Band Nonparabolicity in SiGe/Ge Quantum Wells**, Benjamin Rössner¹; Hans von Känel^{1,2}; Daniel Chrastina²; Giovanni Isella²; Betram Batlogg¹; ¹ Laboratory for Solid State Physics, ETH Zürich, CH-8093 Zürich, Switzerland; ² :L-NESS Dipartimento di Fisica, Polo Regionale di Como del Politecnico di Milano, I-22100 Como, Italy **130**
- 5P.46 **Influence of Collector Design on the SiGe HBT's Quasi-Saturation Characteristics**, Will Cai; Jie Zheng; Ed Preisler; Paul Hurwitz; Marco Racanelli; Jazz Semiconductor, 4321 Jamboree Rd., Newport Beach, CA, 92660, USA **132**
- 5P.47 **Highly tensile strained Silicon Carbon Phosphorus alloys epitaxially grown into recessed source drain areas of NMOS devices**, Matthias Bauer¹; Vladimir Machkauostan²; Chantal Arena¹; ¹ ASM America, 3440 East University Drive, Phoenix, AZ 85034, USA; ² ASM Belgium, Kapeldreef 75, B-3001 Leuven, Belgium **134**
- 5P.48 **Systemic study of thick strained silicon NMOSFETs for digital applications**, J.G. Fiorenza¹; P. Kohli³; S.J. Kang⁴; M. Erdtmann¹; M. Curtin¹; S. Bengston¹; K. Matthews²; B. Nguyen²; I.K. Kim⁴; H.S. Yuk⁴; D.K. Lee⁴; B.Y. Lee⁴; A. Lochtefeld¹; R. Wise³; ¹ AmberWave Systems Corporation, Salem, NH, USA; ² Advanced Technology Development Facility, Austin, TX, USA; ³ Silicon Technology Development, Texas Instruments, Dallas, TX, USA; ⁴ LG Siltron, Gumi, Korea **136**

Session 6: Panel Discussion: *What's the next big thing for SiGe after strained Si and HBTs?* 8:00 PM – 9:30 PM, Friend 101

Session Chairs: Eugene Fitzgerald and Steven Koester

Tuesday, May 16, 2006

Registration and Breakfast

7:45 AM – 8:30 AM, Friend Center 113

Session 7: Invited: FET's and CMOS

8:30 AM – 10:30 AM, Friend 101

Session Chairs: Steven Koester and Brice de Jaeger

8:30: 7.1 **High mobility nano-scaled CMOS: some opportunities and challenges**, Thomas Ernst¹; Francois Andrieu¹; Olivier Weber^{1,2}; Cecilia Dupré^{1,2}; Olivier Faynot¹; Frédérique Ducroquet^{2,1}; Laurent Clavelier¹; Jean-Michel Hartmann¹; Sylvain Barraud¹; Gérard Ghibaudo²; Simon Deleonibus¹; ¹ CEA/DRT-LETI, 17 Rue des Martyrs, 38054 Grenoble Cedex 9, France; ² IMEP, UMR CNRS, ENSERG, BP 257, 38016 Grenoble, France **138**

9:00: 7.2 **Strained and relaxed SiGe for high-mobility MOSFETs**, Minjoo L Lee; Dimitri Antoniadis; Eugene A Fitzgerald; MIT, 77 Massachusetts Ave., 13-4154, Cambridge, MA, 02139, USA **140**

9:30: 7.3 **Strained-SOI/SGOI Dual Channel CMOS Technology Based on Ge Condensation Technique**, Tsutomu Tezuka¹; Shu Nakaharai¹; Yoshihiko Moriyama¹; Norio Hirashita¹; Eiji Toyoda²; Toshinori Numata¹; Toshifumi Irisawa¹; Koji Usuda¹; Naoharu Sugiyama¹; Tomohisa Mizuno^{3,4}; Shin-ichi Takagi^{3,5}; ¹ MIRAI-ASET, 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 212-8582, Japan; ² Toshiba Ceramics, Japan; ³ MIRAI-AIST, Japan; ⁴ Kanagawa Univ.; ⁵ Univ. of Tokyo, Japan **142**

10:00: 7.4 **Strained SOI/GOI**, M Kennard¹; ¹ SOITEC, Bernin, France **144**

Break

10:30 AM – 10:50 AM, Friend 113

[Parallel Session]

Session 8A: Strained Si FET's/Selective Epitaxy

10:50 AM – 12:05 PM, Friend 101

Session Chair: Yasuo Kunii

10:50: 8A.1 **Effective Surface Treatments for Selective Epitaxial SiGe Growth in Locally Strained pMOSFETs**, Chin-I Liao¹; Yi-Cheng Chen¹; Po-Lun Cheng¹; Hsiang-Ying Wang¹; Chin-Cheng Chien¹; Chan- **145**

- Lon Yang¹; K T Huang¹; S F Tzou¹; Jinsong Tang²; Rohini Kodali²; Lori Washington²; Vincent C Chang²; Tony Fu²; Yonah Cho²; ¹ United Microelectronics Corp., No 18, Nanke 2nd Rd. Tainan Science Park, Sinshih Township, Tainan County, 741, Taiwan R.O.C.; ² Applied Materials, 974 E. Arques Avenue, Sunnyvale, CA, 94086, USA **145**
- 11:05: 8A.2 **Selective Epitaxial Si/SiGe for V_T Shift Adjustment in High k pMOS Devices**, Roger Loo¹; Haruyuki Sorada²; Akira Inoue²; Byeong Chan Lee³; Sangjin Hyun³; Guilherme Lujan^{1*}; Thomas Y. Hoffmann¹; Matty Caymax¹; ¹IMEC, Kapeldreef 75,B-3001 Leuven (Heverlee), Belgium; ²assigned to IMEC from Matsushita Electric Industrial Co., Ltd., 3-1-1 Yagumo-naka-machi, Moriguchi, Osaka, 570-8501, Japan; ³assigned to IMEC from Samsung Electronics Co., San#24 Nongseo-Ri, Giheung-Eup, Yongin-City, Gyeonggi-Do, Korea 449-711 *current address: Austriamicrosystems AG, Schloss Premstätten, A 8141, Austria **147**
- 11:20: 8A.3 **High Density Planes Deposition Kinetics and Facets Propagation in Silicon Selective Epitaxial Growth**, N. Loubet; A. Talbot; D. Dutartre; STMicroelectronics, 850 rue Jen Monnet, 38926 Crolles Cedex, France **149**
- 11:35: 8A.4 **Growth kinetics of Si and SiGe on Si(100), Si(110) and Si(111) surfaces**, J. M. Hartmann; M. Burdin; G. Rolland; T. Billon; CEA-DRT, LETI/D2NT & DPTS, CEA/GRE – 17, Avenue des Martyrs 38054 Grenoble Cedex 9, France **151**
- 11:50: 8A.5 **Flexible Thin-film Transistors on Strained Si/SiGe Membranes**, Hao-Chih Yuan¹; Guogong Wang¹; Michelle M Roberts²; Donald E Savage²; Max G Lagally²; Zhenqiang Ma¹; ¹Dept. of Electrical and Computer Engineering; ²Dept. of Materials Science and Engineering, University of Wisconsin-Madison, 1415 Engineering Dr., Madison, WI, 53706, USA **153**

[Parallel Session]

Session 8B: Heterostructure Growth and Novel Characterization

10:50 AM – 12:05 PM, CS104

Session Chair: Hans von Kaenel

- 10:50: 8B.1 **Selective MBE of High-Quality Ge on Si Covered with SiO₂**, Qiming Li¹; Darin Leonhardt¹; Joshua L Krauss¹; Stephen Hersee²; Sang M Han¹; ¹Dept. of Chemical & Nuclear Engineering, University of New Mexico, 209 Farris Engineering Center, Albuquerque, NM 87131, USA ²Center for High Technology Materials, University of New Mexico, 1313 Goddard SE, Albuquerque, NM 87106, USA **155**
- 11:05: 8B.2 **High Growth Rate of Epitaxial Silicon-Carbon Alloys by High-Order Silane Precursor and Chemical Vapor Deposition**, K. Chung¹; J.C. Sturm¹; E. Sanchez²; S. Kuppuroa²; ¹ Princeton Institute for the Science and Technology of Materials (PRISM) and Dept. of Electrical Engineering, Princeton University, Princeton, NJ, 08544, USA; ²Applied Materials, 3050 Bowers Avenue, Santa Clara, CA, 95054 USA **157**
- 11:20: 8B.3 **Three-dimensional characterization of SiGe structures with a laser assisted local electrode atom probe**, Keith Thompson; David J Larson; Joseph H Buntun; Thomas F Kelly; Imago Scientific Instruments, 6300 Enterprise Ln. Suite 100, Madison, WI, 53719, USA **159**
- 11:35: 8B.4 **Characterization of a SiGe layer after isotropic etching of surrounding Si.**, Stephan Borel¹; Véronique Caubet²; Dominique Lafond¹; Olivier Kermarrec²; Yves Campidelli²; ¹CEA/Leti, 17 Rue des Martyrs, 38054 Grenoble Cedex 9, France; ² ST Microelectronics, 850 Rue Jean Monnet, 38926 Crolles, France **161**

11:50: 8B.5 **Intense photoluminescence from Ge(Si) self-assembled islands embedded in a tensile-strained Si layer**, A.V. Novikov¹; M.V. Shaleev¹; A. N. Yablonskiy¹; O. A. Kuznetsov²; Y. N. Drozdov¹; D. N. Lobanov¹; Z.F. Krasilnik¹; ¹Institute for Physics of Microstructures, RAS, 603950, Nizhny Novgorod, GSP-105, Russia; ²Physical-Technical Research Institute, Nizhny Novgorod State University, 603950, Nizhny Novgorod, Russia

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Session 9: Poster Session and Lunch

12:05 PM – 2:00 PM, Friend 113 and Atrium

Session 10: Invited: Quantum Devices and Novel Structures

2:00 PM – 3:30 PM, Friend 101

Session Chairs: Junichi Murota and James Kolodzey

2:00: 10.1 **SiGe Quantum Cascade Structures: Physics, Growth and Technology**, Detlev Grützmacher¹; S. Tsujino¹; G. Mussler¹; V. Shushunova¹; M. Scheinert¹; E. Müller¹; N. Demarina¹; H. Sigg¹; J. Faist²; O. Kerrmarrec³; ¹Laboratory for Micro- and Nanotechnology, Paul Scherrer Institut, CH-5232, Villigen-PSI, Switzerland; ²Institute of Physics, University of Nuechatel, 1 A.-L. Breguet, CH-2000 Switzerland; ³STMICROELECTRONICS, Crolles, F-38926 France

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2:30: 10.2 **SiGe: Materials and Devices for Quantum Computing**, Mark A. Eriksson¹; L.J. Klein¹; M.M. Roberts¹; D.E. Savage¹; S. Goswami¹; K.A. Slinker¹; L.M. McGuire¹; M. Friesen¹; G. Celler²; M.G. Lagally¹ and S.N. Coopersmith¹; ¹University of Wisconsin-Madison, Madison, Wisconsin 53711, USA; ²Soitec USA, 2 Centennial Drive, Peabody, MA 01960 USA

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3:00: 10.3 **SiGe/Si "Micro-Origami" epitaxial MEMS device on SOI substrate**, Takashi Tokuda; Masahiro Nunoshita; Jun Ohta; Graduate School of Materials Science, Nara Institute of Science and Technology, Takayama 8916-5, Ikoma, Nara, 630-0101, Japan

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Break

3:30 PM – 3:45 PM, Friend 113

[Parallel Session]

Session 11A: Virtual Substrates

3:45 PM – 5:15 PM, Friend 101

Session Chair: Siegfried Mantl

3:45: 11A.1 **Formation of SGOI structures with low dislocation density by two step oxidation and condensation method**, N. Sugiyama¹; S. Nakaharai¹; N. Hirashita¹; T. Tezuka¹; Y. Moriyama¹; K. Usuda¹; S. Takagi^{2,3}; ¹MIRAI-ASET; ²MIRAI-AIST, University of Tokyo, 1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki, Japan

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4:00: 11A.2 **Fabrication of SiGe-On-Insulator by Improved Ge condensation technique**, J.F. Damlencourt¹; B. Vincent¹; P. Riyallin¹; P. Holliger¹; D. Rouchon¹; E. Nolot¹; C. Licitra¹; Y. Morand²; L. Iavelier¹; T. Billon¹; ¹CEA-DRT-LETI – CEA/GRE, 17 avenue des martyrs, Grenoble Cedex 9, France; ²ST Microelectronics, 12 rue Jules Horowitz, 38000 Grenoble, France

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4:15: 11A.3 **Single Wafer sSOI by SIMOX**, J. P de Souza; S. W Bedell; H. J. Hovel; K. Fogel; A. Reznicek; D.

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K Sadana; IBM, T. J. Watson Research Center, 1101 Kitchawan Rd / Rte 134, Yorktown Heights, NY, 10598; USA

- 4:30: 11A.4 **Strain Relaxation in Strained-Si Layer on SiGe-on-Insulator Substrate**, Norio Hirashita¹; Yoshihiko Moriyama¹; Eiji Toyoda²; Naoharu Sugiyama¹; Shin-ichi Takagi³; ¹MIRAI-ASET, 1, Komukai Toshiba-cho, Saiwaiku, Kawasaki, 212-8216, Japan; ² Toshiba Ceramics Co., Ltd., Seirou-machi, Kitakanbaragun, Nigata, 957-0197, Japan; ³MIRAI-AIST, Tsukuba, 305-8569, Japan **176**
- 4:45: 11A.5 **Generation of Crystal Defects in Ge-on-Insulator (GOI) Layers in Ge-condensation Process**, S. Nakaharai¹; T. Tezuka¹; N. Hirashita¹; E. Toyoda²; Y. Moriyama¹; N. Sugiyama¹; S. Takagi^{3,4}; ¹ MIRAI-ASET, 1, Komukai-toshiba-cho, Saiwai-ku, Kawasaki, 212-8582, Japan; ² Toshiba Ceramics, 6-864-5 Higashikou, Seirou-Machi, Kitakanbara-gun, 957-0197, Japan; ³ MIRAI(ASET), 1, Komukai-toshiba-cho, Saiwai-ku, Kawasaki, 212-8582; ⁴University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-8656, Japan **178**
- 5:00: 11A.6 **Reducing threading dislocation densities in SiGe mismatched layers by controlling strain rate and surface roughness**, Saurabh Gupta; Yu Bai; David M Isaacson; Eugene A Fitzgerald; Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA, 02139, USA **180**

[Parallel Session]

Session 11B: Novel/Quantum Devices

3:45 PM – 5:15 PM, CS 104

Session Chair: Mark Eriksson

- 3:45: 11B.1 **Direct Measurement of HH2-HH1 Intersubband Lifetimes in SiGe Quantum Cascade Structures**, P. Rauter¹; T. Fromherz¹; G. Bauer¹; N.Q. Vinh²; P.J. Phillips³; C.R. Pidgeon³; B.N. Murdin⁴; L. Diehl⁶; G. Dehlinger⁵; D. Grutzmacher⁵; ¹Institute for Semiconductor and Solid State Physics, Johannes-Kepler-University Linz, Austria, ²FOM Institute for Plasma Physics Rijnhuizen, Nieuwegein, Netherlands, ³Heriot-Watt University, Edinburgh, UK, ⁴University of Surrey, Guildford, UK, ⁵Paul Scherrer Institut, Villigen, Switzerland, ⁶ Princeton University, USA **182**
- 4:00: 11B.2 **Thermoelectric Power Generation using Large Area Si/SiGe pn-Junctions with varying Ge-content**, M. Wagner¹; G. Span²; T. Grasser¹; ¹Institute for Microelectronics, Gusshausstr. 27-29/E360, 1040 Vienna, Austria; ² SAM – Span and Mayrhofer KEG, 6112 Wattens, Austria **184**
- 4:15: 11B.3 **Lateral Quantum Dot in Si/SiGe realized by a Schottky Split-Gate Technique**, Thomas P Berer; Dietmar Pachinger; Georg Pillwein; Michael Mühlberger; Herbert Lichtenberger; Gerhard Brunthaler; Friedrich Schäffler; Institut für Halbleiter-und Festkörperphysik, Johannes Kepler University, Altenbergerstrasse 69, A-4040, Linz, Austria **186**
- 4:30: 11B.4 **Investigation of upper and lower limits of carrier concentration for two-dimensional electron gas in strained silicon**, Jian Liu¹; Bin Shi¹; Keji Lai²; Tzu-Ming Lu²; Ya-Hong Xie¹; Daniel C Tsui²; ¹ Dept. of Materials Science and Engineering, University of California at Los Angeles, Box 951595, Los Angeles, California 90095-1595, USA; ² Dept. of Electrical Engineering, Princeton University, Princeton, NJ, 08544 USA **188**
- 4:45: 11B.5 **Electroluminescence from the Ge quantum dot metal-oxide-semiconductor tunneling diodes**, M. H. Liao¹; T.-H Cheng²; T. C Chen²; C.-H Lai¹; C.-H Lee²; C W Liu^{1,2}; ¹ Dept. of Electrical Engineering and Graduate Institute of Electro-Optical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C. ² **190**

Dept. of Electrical Engineering and Graduate Institute of Electronic Engineering, National Taiwan University, Taipei, Taiwan, R.O.C.

5:00: 11B.6 **Metal-insulator-metal photodetectors with Ge quantum dots formed by selective oxidation of single crystalline-Si_{0.85}Ge_{0.15}/Si-on-insulator**, S. S. Tzeng; P.W. Li; W.M. Laio; W.T. Liah; Dept. of Electrical Engineering, National Central University, No.300, Chungda Rd., Taoyuan, Taiwan, R.O.C. 320

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Conference Banquet: Reception
6:00 PM – 7:00 PM, Prospect House

Conference Banquet: Dinner
7:00 PM – 9:00 PM, Prospect House

Wednesday, May 17, 2006

Registration and Breakfast
7:45 AM – 8:30 AM, Friend Center 113

Session 12: Invited: HBT's, FET's, and CMOS
8:30 AM – 10:30 AM, Friend 101

Session Chairs: Bruno Ghyselen and Brian Gaucher

8:30: 12.1 **SiGe BiCMOS Technologies for Improving Sensitivity and High-Speed Characteristics of the Communication LSIs**, Makoto Miura¹; Hiromi Shimamoto³; Reiko Hayami¹; Akihiro Kodama³; Tatsuya Tominari²; Takashi Hashimoto²; Katsuyoshi Washio¹; ¹ Central Research Laboratory, Hitachi, Ltd., Tokyo 185-8601, Japan; ² Micro Device Division, Hitachi Ltd. ³ Renesas Northern Japan Semiconductor, Inc. Japan

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9:00: 12.2 **High-Performance BiCMOS Technologies without Epitaxially-Buried Subcollectors and Deep Trenches**, Bernd Heinemann; R. Barth; D. Knoll H. Rücker; B. Tillack; W. Winkler; IHP, Im Technologiepark 25, Frankfurt (Oder), 15236, Germany

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9:30: 12.3 **Control and characterization of strain in SiGe/Si heterostructures with engineered misfit dislocations**, Akira Sakai¹; Noriyuki Taoka¹; Shogo Mochizuki¹; Katsunori Yukawa¹; Osamu Nakatsuka²; Shingo Takeda³; Shigeru Kimura^{3,4}; Masaki Ogawa⁵; Shigeaki Zaima¹; ¹ Graduate School of Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan; ² EcoTopia Science Institute, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan; ³ JASRI/Spring-8, Kouto, Mikazuki-cho, Sayo-gun, Hyogo 679-5198, Japan; ⁴ CREST, JST, Honmachi, Kawaguchi, Saitama 332-0012, Japan; ⁵ CCRASST, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan

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10:00: 12.4 **Uniaxial and Biaxial Strain for CMOS Performance Enhancement**, Bich-Yen Nguyen; Debby Eades; Victor H Vartanian; Jon Cheek; Da Zhang; Bruce E White; Suresh Venkatesan; Aaron Thean; Paul A Grudowski; Ted R White; Stefan Zollner; David Theodore; Brian J Goolsby; Heather Desjardins; Lata Prabhu; Ricardo Garcia; John Hackenberg; Veer Dhandapani; Sharon Murphy; Raghaw S Rai; James R Conner; Patrick

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K Montgomery; Colita M Parker; Jill Hildreth; Ross E Noble; Mo Jahanbani; Freescale Semiconductor, 3501 Ed
Bluestein Blvd., Mail Drop K10, Austin, TX, 78712, USA

Break

10:30 AM – 10:50 AM, Friend 113

[Parallel Session]

Session 13A: HBT Devices

10:50 AM – 11:55 AM, Friend 101

Session Chair: Marwan Khater

- 10:50: 13A.1 **Carbon effect on neutral base recombination in high-speed SiGeC HBTs**, Benoit Barbatat^{1,2}; **203**
Thierry Schwartzmann¹; Pascal Chevalier¹; Benoit Vandelle¹; Laurent Rubaldo¹; Fabienne Saguin¹; Nicolas
Zerounian²; Frédéric Aniel²; Alain Chantre¹; ¹ STMicroelectronics, 850 rue Jean Monnet, Crolles Cedex,
38926, France; ² Institut d'Electronique Fondamentale, Bat. 220, Université Paris Sud 11, F-91405 Orsay Cedex,
France
- 11:05: 13A.2 **Improved Carbon Incorporation in Selective Epitaxial Growth of SiGe:C for HBT** **205**
Applications, Florence Brossard; Benoît Vandelle; Pascal Chevalier; Didier Dutartre; STMicroelectronics, 850
rue Jean Monnet, F-38926 Crolles Cedex, 38926, France
- 11:20: 13A.3 **Influence of lateral device scaling and airgap deep trench isolation on reliability performance** **207**
of 200GHz SiGe:C HBTs, Andreas Piontek¹; Tony Vanhoucke²; Stefaan Van Huylbroeck¹; Li Jen Choi¹;
G.A.M. Hurkx²; E. Hijzen²; S. Decoutere¹; ¹ IMEC, Kapeldreef 75, Leuven, B-3001, Belgium; ² Philips
Research Leuven, Kapeldreef 75, Leuven, B-3001, Belgium
- 11:35: 13A.4 **Thermal Resistance of SiGe HBTs at High Power Densities**, Hui Li¹; Zhenqiang Ma¹; Pingxi **209**
Ma²; Marco Racanelli²; ¹ Department of Electrical and Computer Engineering, University of Wisconsin-
Madison, 1415 Engineering Drive, Madison, WI, 53705, USA ² Jazz Semiconductor, Inc., Newport Beach, CA,
92660; ³ Jazz Semiconductor, Inc., Newport Beach, CA, 92660 USA
- 11:50: 13A.5 **On the Scaling of Emitter Stripes of SiGe Power HBTs**, Guogong Wang; Hao-Chih Yuan; **211**
Zhenqiang Ma; University of Wisconsin, 1415 Engineering Drive, Madison, WI, 53706 USA

[Parallel Session]

Session 13B: Relaxation of Patterned/Asymmetric Structures

10:50 AM – 11:55 AM, CS 104

Session Chair: Naoharu Sugiyama

- 10:50: 13B.1 **Characterization of in-plane strain relaxation in strained layers after mesa isolation using a** **213**
newly developed plane-NBD method, Koji Usuda¹; Toshifumi Irisawa¹; Toshinori Numata¹; Norio Hirashita¹;
Shinichi Takagi²; ¹ MIRAI-ASET; MIRAI-AIST; ²University of Tokyo, Japan
- 11:05: 13B.2 **Fabrication and Characterization of Patterned Si/SiGe Lines with Asymmetric Biaxial Stress**, **215**
Dan M Buca¹; Bernd Holländer¹; Sebastian Feste¹; Helmut Trinkaus¹; Siegfried Mantl¹; R. Loo²; Matty

Caymax²; ¹ Center for Nanoelectronic Systems for Information Technology, Forschungszentrum Juelich, 52428, Germany; ² IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

11:20: 13B.3 **Dynamics of uniform Si/SiGe uniaxial strain generation on compliant insulation substrates**, Rebecca L Peterson; James C Sturm; Princeton Institute for the Science and Technology of Materials (PRISM) and Department of Electrical Engineering, Princeton University, 320 Bowen Hall, 70 Prospect Ave, Princeton, NJ, 08540, USA **217**

11:35: 13B.4 **Strain Control and Electrical Properties of Stripe Patterned Si/Si_{1-x}Ge_x/Si(100) Heterostructures**, Jangwoong Uhm; Masao Sakuraba; Junichi Murota; Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai, 980-8577, Japan **219**

11:50: 13B.5 **Strain relaxation of patterned Ge and SiGe layers on Si(001) substrates**, Shogo Mochizuki¹; Akira Sakai¹; Osamu Nakatsuka²; Hiroki Kondo¹; Katsunori Yukawa¹; Koji Izunome³; Takeshi Senda³; Eiji Toyoda³; Masaki Ogawa⁴; Shigeaki Zaima¹; ¹ Dept. of Crystalline Materials Science, Graduate School of Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan; ² EcoTopia Science Institute, Nagoya University; ³ Toshiba Ceramics Co., Ltd., 6-861-5 Higashikou, Seirou-machi, Kitakanbara-gun, Niigata 957-0197, Japan; ⁴ CCRASST, Nagoya University, Furo-cho, Chikusa-Ku, Nagoya 464-8603 Japan **221**

Lunch

12:05 PM – 1:30 PM, Friend Center 113

Session 14: Invited: HBT Circuits and Engineered Substrates

1:30 PM – 2:30 PM, Friend 101

Session Chair: Bernd Tillack

1:30: 14.1 **Progress in SiGe Technology Toward Full Integrated mmWave ICs**, Brian Gaucher¹; Scott K Reynolds¹; Brian Floyd¹; Ullrich Pfeiffer¹; Troy Beukema¹; Alvin Joseph²; Essam Mina²; Bradley Orner²; Richard Wachnick³; Keith Walter³; ¹IBM Research 1101 Kitchawan Rd./Rte.134, Yorktown Heights, NY, 10598, USA; ² IBM S&TG, 1000 River St. Essex Junction, VT 05452 USA; ³ IBM S&TG, 2070 Rt. 52, M/S EM1, Hopewell Junction, NY 12533, USA **223**

2:00: 14.2 **Enhancing CMOS Transistor Performance using Lattice-Mismatched Materials in Source/Drain Regions**, Yee-Chia Yeo; Dept. of Electrical and Computer Engineering, National University of Singapore, S117576, Singapore **225**

Break

2:30 PM – 2:45 PM, Friend Atrium

[Parallel Session]

Session 15A: HBT Devices and Circuits

2:45 PM – 4:00 PM, Friend 101

Session Chair: Bernd Heinemann

2:45: 15A.1 **SiGe HBT design for CMOS compatible SOI**, Alain Chantre¹; Grégory Avenier^{1,2}; Pascal Chevalier¹; Benoit Vandelle¹; Fabienne Saguin¹; Cristell Maneux²; Didier Dutartre¹; Thomas Zimmer²; ¹ **227**

STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France ² Laboratoire de Microelectronique IXL, CNRS UMR 5818, Universite Bordeaux 1, F-33405, Talence, France

3:00: 15A.2 **SiGe HBT Linearity Comparison Between CE and CB Configurations**, Guoxuan Qin; Ningyue Jiang; Guogong Wang; Zhenqiang Ma; University of Wisconsin-Madison, Dept. of Electrical and Computer Engineering, 1415 Engineering Drive, Madison, WI 53706 USA **229**

3:15: 15A.3 **p-i-n Diodes for Monolithic Millimeter Wave BiCMOS Applications**, Bradley A Orner¹; Qizhi Liu¹; Jeffrey Johnson¹; Robert Rassel¹; Xuefeng Liu¹; David Sheridan¹; Alvin Joseph¹; Brian Gaucher²; ¹ IBM, Systems and Technology Group, 1000 River Road, Essex Junction, Vermont 05452 USA; ² IBM, T.J. Watson Research Center, 1101 Kitchawan Ave., Yorktown Heights, NY 10598 USA **231**

3:30: 15A.4 **SiGe Impulse Generator for Single-Band Ultra-Wideband Applications**, Jochen Dederer; Andreas Trasser; Hermann Schumacher; University of Ulm, Dept. of Electron Devices and Circuits, Albert-Einstein-Allee 45, 89069, Ulm, Germany **233**

3:45: 15A.5 **X-band and K-band low-phase-noise VCOs using SiGe BiCMOS technology**, Jean-Guy Tartarin^{1, 2}; King W. Wong³; Eric Tournier^{1, 2}; Olivier Llopis²; ¹ Paul Sabatier University ² LAAS-CNRS, 7 av. du Colonel Roche, 31.077, Toulouse cedex 4, FRANCE; ³ Institute of Microelectronics, 11 Science Park Road, Singapore Science Park II, Singapore, 117685 **235**

[Parallel Session]

Session 15B: Process Technology

2:45 PM – 4:00 PM, CS 104

Session Chair: Chee-Wee Liu

2:45: 15B.1 **Surface Segregation and Electrical Studies of Heavily Arsenic and Phosphorus in situ Doped Epi and Poly Silicon.**, Gaël Borot¹; Laurent Rubaldo¹; Nicolas Breil¹; Jumana Boussey²; Xavier Mescot³; Gérard Ghibaudo³; Didier Dutartrec¹; ¹ STMicroelectronics, 850, rue Jean Monnet, 38926 Crolles Cedex , France; ² Laboratoire des Technologies de la Microelectronique, LTM-CNRS-CEA-LETI-D2NT; ³ Institut de Microelectronique, Electromagnetisme and Photonique (IMEP), ENSERG, France **237**

3:00: 15B.2 **Phosphorus Segregation Control for SiGe:C Epitaxy**, Yuji Yamamoto; Klaus Köpke; Peter Zaumseil; Bernd Tillack; IHP, Im Technologiepark 25, Frankfurt (Oder), 15236, Germany **239**

3:15: 15B.3 **Thermal Stability of strained-SOI (sSOI)**, Atsushi Fukumoto¹; Kentaro Sawano¹; Yusuke Hoshi¹; Makoto Yoshimi^{1, 2}; Yasuhiro Shiraki³; ¹ Musashi Institute of Technology, 8-15-1 Todoroki, Setagaya-ku, Tokyo, 158-0082, Japan; ² SOITEC Asia, 3-3-1 Marunouchi, Chiyoda-ku, Tokyo, 100-0005, Japan; ³ Musashi Institute of Technology, 8-15-1 Todoroki, Setagaya-ku, Tokyo, Japan **241**

3:30: 15B.4 **Interdiffusion in SiGe/Si Epitaxial Heterostructures**, Guangrui Xia¹; Michael Canonico²; Judy L Hoyt¹; ¹ Microsystems Technology Laboratories, Massachusetts Institute of Technology, 60 Vassar Street, Rm. 39-661, Cambridge, MA, 02139, USA; ² Physical Analysis Laboratory Arizona (PALAZ), Freescale Semiconductor, Inc., Tempe, AZ, 85284, USA **243**