Advanced signal processing, circuits, and system design techniques for communications

edited by:
V. Paliouras, T. Stouraitis, and A. Ioinovici

Advanced signal Processing, circuits, and system design techniques for communications

IEEE Catalog Number: 06TH8891
ISBN: 1-4244-0460-6
Library of Congress: 2006926273

© 2006 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Contents

1 Introduction **1**

2 Low-power EDA Technologies **3**
E. Macii and R. Zafalon
2.1 Introduction and Background 4
2.2 Low-Power Design Flow 6
2.3 Low-Power Design Technologies 7
2.3.1 Dynamic Power Control 8
2.3.2 Leakage Power Control 29
2.4 Conclusions 40
2.5 Bibliography 40

3 Extensible and Configurable Processors for SoC Design **45**
Jari Nurmi, Steve Leibson, Fabio Campi, and Christian Panis
3.1 Introduction 46
3.2 Accelerating Single-Processor Cores – a Co-Processor Approach 47
3.2.1 COFFEE RISC Core 47
3.2.2 Reconfigurable Algorithm Accelerator 49
3.2.3 Mapping Algorithms on RAA 52
3.3 Scalable Instruction-Word VLIW DSP Architecture 55
3.3.1 xDSPcore 58
3.3.2 DSPxPlore 59
3.3.3 Summary 66
3.4 Extensible RISC Processor – Xtensa 66
3.4.1 Xtensa Configurable Registers and Register Files . 68
3.4.2 The Xtensa Program Counter 68
3.4.3 Memory Address Space 70
3.4.4 Configurable Byte Ordering 70

3.4.5 Fast Endian Conversion with One Instruction Extension . . . 71
3.4.6 The TIE Language . . . 74
3.4.7 Improving Application Performance using TIE . . 74
3.4.8 Adding SIMD Instructions using TIE . . . 78
3.4.9 Adding FLIX Instructions using TIE . . . 79
3.5 Run-Time Reconfigurable DSP RISC Processor . . . 80
3.5.1 XiRisc: a VLIW Processor . . . 83
3.5.2 Pipelined Configurable Gate Array (PiCoGA) . . . 85
3.5.3 Software Development Flow . . . 89
3.5.4 Results . . . 92
3.6 Conclusions – The Future of SoC Design . . . 94
3.7 Bibliography . . . 96

4 UWB radio in Distributed Wireless Networks 99
M.-G. Di Benedetto, G. Giancola, and D. Domenicali
4.1 Introduction . . . 99
4.2 The UWB Radio Signal and spectral characteristics . . . 101
4.3 Power issues and current standardization trends . . . 104
4.4 Multi User Interference in Impulse Radio UWB Networks 107
4.5 Ranging and Positioning in UWB Networks . . . 111
4.6 Medium Access Control for UWB networks . . . 114
4.7 Location-Aware Routing in UWB networks . . . 116
4.8 Introducing cognitive principles in UWB networks . . . 118
4.9 Bibliography . . . 128

5 Advances on Analog Filters for Telecommunications 131
A. Baschirotto, S. D'Amico, and M. De Matteis
5.1 Introduction . . . 132
5.2 Receiver Architectures for Silicon Implementation . . . 133
5.3 The base-band channel selection filter . . . 135
5.4 Active RC filters: the Rauch cell case . . . 136
5.4.1 A Rauch cell design example . . . 137
5.5 The Active-G_m-RC Low-Pass Cell . . . 139
5.5.1 A design example: a fourth-order reconfigurable UMTS/WLAN filter . . . 141
5.5.2 Automatic design toolbox . . . 148
5.6 A source-follower-based continuous-time filter . . . 152
5.6.1 A design example: a fourth-order filter for WLAN 153
5.7 The G_m-G_m-C Filter . . . 158

5.7.1 A design example: a baseband filter for a UWB node 160
5.8 Comparison between the different filter techniques 162
5.9 Conclusions 162
5.10 Bibliography 164

6 Time-Continuous Delta-Sigma A/D Converters 169
A. Buhmann, M. Keller, M. Ortmanns, F. Gerfers, and Y. Manoli
6.1 Introduction 170
6.2 Basics 171
6.2.1 Sampling and Quantization 171
6.2.2 Nyquist Rate, Oversampling and Noise-Shaping Converters 172
6.2.3 Performance Increase in ΣΔ Modulators 173
6.2.4 Stability Constraints and Scaling 174
6.2.5 CT Loop-Filter Synthesis 175
6.3 Architectures and Implicit Anti-Aliasing Feature 177
6.3.1 Single-Stage Architectures 177
6.3.2 Multi-Stage/Cascaded Architectures 182
6.4 Non-Idealities and Correction Techniques 187
6.4.1 Different Error Locations or Input Referred Non-Idealities 187
6.4.2 Errors of the Feedback DAC 188
6.4.3 Errors of the Filters 192
6.4.4 Errors of the Internal Quantizer 196
6.5 Recent Implementations of CT ΣΔ Modulators 196
6.5.1 CT Loop-Filter Implementation 196
6.5.2 Single- and Multi-bit Quantizer and Feedback DAC Realization 199
6.5.3 Implementation Example I: A 12-Bit 25kHz 1.5V CT ΣΔ Modulator 201
6.5.4 Implementation Example II: A CT ΣΔ Modulator with SCR-Feedback 203
6.5.5 Implementation Example III: A 70-mW 300-MHz CMOS Continuous-Time ΣΔ ADC With 15-MHz Bandwidth and 11 Bits of Resolution 204
6.5.6 Implementation Example IV: A Cascaded CT ΣΔ Modulator with 67dB Dynamic Range in 10MHz Bandwidth 207
6.6 Conclusion 209
6.7 Bibliography 210

7 ESD Protection Design in nano CMOS **217**
M.-D. Ker
7.1 Introduction to Electrostatic Discharge (ESD) 218
7.1.1 ESD Standards and Models 218
7.1.2 ESD Testing 223
7.1.3 ESD Testing for HBM / MM 223
7.2 Design Techniques of ESD Protection Circuit 231
7.2.1 Basic ESD Protection Concept 231
7.2.2 Turn-on Uniformity of ESD Protection Devices . . 233
7.2.3 ESD Implantation and Silicide Blocking 235
7.2.4 Some ESD Protection Guidelines 237
7.3 Whole-Chip ESD Protection Design 238
7.3.1 Power-Rail ESD Clamp Circuit 241
7.3.2 Location of Power-Rail ESD Clamp Circuit 245
7.3.3 Protection for ICs with Separated Power Lines . . 247
7.4 ESD Protection for Mixed-Voltage I/O Interface 248
7.4.1 Mixed-Voltage I/O 248
7.4.2 ESD Design Constraints in Mixed-Voltage I/O . . 251
7.4.3 ESD Protection Design for Mixed-Voltage I/O . . 255
7.4.4 High-Voltage-Tolerant Power-Rail ESD Clamp Circuit 264
7.5 Summary 268
7.6 Bibliography 270

List of Figures **281**

List of Tables **291**