

PRIME 

**2nd Conference
on
Ph.D. Research
in MicroElectronics and Electronics**

Otranto (Lecce), Italy
June 12-15, 2006

Proceedings

Editors: P. Malcovati, A. Baschiroto

© 2006 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

IEEE Catalog Number: 06EX1296
ISBN: 1-4244-0156-9
Library of Congress: 2006920529

Table of Contents

Session 1A1 - Analog Techniques 1

A Voltage Efficient PMOS Charge Pump Architecture	1
L. Mensi, A. Ricelli, L. Colalongo, Z. Kovacs Vajna University of Brescia	
Switched Capacitor Non-Linear Function Synthesizer Based on a Novel Iterative Method	5
N. Nizza, M. Schipani, P. Bruschi University of Pisa	
A Low-Ripple Fast-Settling CMOS Envelope Detector	9
J. Alegre, S. Celma, M. Sanz, P. Martínez University of Zaragoza	

Session 1A2 - Analog Filters

A 600mV Baseband Analog Filter for UMTS Receivers	13
S. D'Amico, M. De Blasi, M. De Matteis, V. Giannini, A. Baschiroto University of Lecce	
A Low Voltage Low Power DCCII and MRC-Based 2nd Order Multiple-Output Filter	17
G. Ferri, V. Stornelli, L. Giuli University of L'Aquila	
A Programmable Double Supply Filter&Drive Block for Telecommunication Applications	21
M. De Matteis ¹ , S. D'Amico ¹ , A. Baschiroto ¹ , A. Di Giandomenico ² , J. Hauptmann ² ¹ University of Lecce, ² Infineon - Villach	
A Fully Integrated Very Low Frequency Single-Ended Gm-C Filter Based on a Novel Transconductor	25
M. Schipani, F. Sebastiano, N. Nizza, P. Bruschi University of Pisa	

Session 1A3 - Power Electronics

Continuous vs. Piecewise Hysteresis Model of a Current Transformer	29
F. Uriarte, V. Centeno, J. De Laree Lopez, J. Depablos Texas A&M University	
Power Supply Generation in CMOS Passive UHF RFID Tags	33
A. Facen, A. Boni University of Parma	
An RTL-to-Grid Design Flow for Power Grid Verification Based on a Statistical Estimation Engine	37
D. Karampatzakis, N. Evmorfopoulos, M. Tsiampas, G. Stamoulis University of Thessaly	

Thermal Mapping of Power Devices with a Completely Automated Thermoreflectance Measurement System	41
L. Rossi, G. Breglio, A. Irace, P. Spirito University of Naples "Federico II"	
Comparison of Calculation Techniques of Constant VSWR Impedance Circle: Evaluation of Power Transistors Robustness	45
F. Blanchet ¹ , H. Bousbia ² , D. Pache ¹ , D. Barataud ² , J. Nebus ² ¹ STMicroelectronics, ² Xlim	
 <u>Session 1A4 - DC-DC Converters</u>	
Analysis of the Substrate Noise Effects due to DC-DC Converter Integration	49
R. Vinella ¹ , R. Antonicelli ² ¹ Politecnico di Bari, ² STMicroelectronics	
Randomised Switching Frequency in a Synchronous-Asynchronous Digital Voltage-Mode Control for DC-DC Converters	53
D. Trevisan ¹ , P. Mattavelli ¹ , S. Saggini ² ¹ University of Udine, ² STMicroelectronics	
Design, Assembly and Testing of Modular Multilevel Converter with Multicarrier PWM Method	57
M. Balzani, A. Reatti, G. Salvadori University of Florence	
 <u>Session 1B1 - Digital Techniques 1</u>	
A New Scheme to Reduce Leakage in Deep-Submicron Cache Memories with No Extra Dynamic Consumption	61
F. Frustaci, P. Corsonello, S. Perri, G. Cocorullo University of Calabria	
Minimizing Peak Power Consumption during Scan Testing: Structural Technique for Don't Care Bits Assignment	65
N. Badereddine ¹ , P. Girard ¹ , S. Pravossoudovitch ¹ , C. Landrault ¹ , A. Virazel ¹ , H. Wunderlich ² ¹ LIRMM CNRS - University of Montpellier II, ² University of Stuttgart	
Profiling Charge Distribution in NROM Devices	69
A. Padovani ¹ , L. Larcher ² , P. Pavan ² ¹ University of Ferrara, ² University of Modena e Reggio Emilia	
 <u>Session 1B2 - FPGA and DSP</u>	
An FPGA-Based Software Defined Radio Platform for the 2.4GHz ISM Band	73
A. Di Stefano, G. Fiscelli, C. Giaconia University of Palermo	
A Flexible FPGA/DSP Board for GNSS Receivers Design	77
M. Spelat ¹ , F. Doviš ¹ , P. Mulassano ² ¹ Politecnico di Torino, ² Istituto Superiore Mario Boella	

Designing an Independent Speaker Isolated Speech Recognition System on an FPGA.	81
C. Gonzalez-Concejero ¹ , V. Rodellar-Biarge ¹ , A. Alvarez-Marquina ² , E. Martinez de Icaya ² , P. Gomez-Vilda ³	
¹ Universidad Politecnica de Madrid, ² Lecturer, ³ Professor	
Evaluation of Hierarchical FPGA Partitioning Methodologies Based on Architecture Rent Parameter	85
Z. Marrakchi, H. Mrabet, H. Mehrez	
Université Paris 6, Pierre et Marie Curie	
 <u>Session 1B3 - Oscillators and VCO</u>	
Angular Modulation of Injection Locked Oscillators	89
T. Finateu ¹ , F. Badets ² , D. Belot ² , J. Begueret, Y. Deval	
¹ STMicroelectronics - IXL Laboratory, ² STMicroelectronics	
A Distributed Voltage Controlled Oscillator in a 65nm CMOS Process	93
N. Seller ¹ , E. Chataigner ¹ , H. Lapuyade ² , J. Begueret ²	
¹ STMicroelectronics, ² IXL Laboratory	
Reduction of CMOS Inverter Ring Oscillator Close-In Phase Noise by Current Mode Instead of Voltage Mode Supply	97
M. Grözing, M. Berroth	
University of Stuttgart	
A VCO Phase-Noise Reduction Technique	101
D. Mavridis, K. Efstathiou	
University of Patras	
A Fully-Integrated 60 GHz VCO in 130nm SOI-CMOS on High-Resistivity Substrate	105
B. Payet, P. Vincent	
CEA-LETI	
 <u>Session 1B4 - Video Processing 1</u>	
A Low-Power VLSI Architecture for Intra and Inter Prediction in H.264	109
M. Koziri ¹ , G. Stamoulis ¹ , I. Katsavounidis ²	
¹ University of Thessaly, ² InterVideo	
An Edge Preserving Spatial Error Concealment Technique for the H.264 Video Coding Standard	113
S. Beesley, A. Armstrong, C. Grecos	
Loughborough University	
Reduced Computation Mode Decision Using Error Domain Heuristics for the H264 Standard	117
M. Yang, C. Grecos, L. Chen	
Loughborough University	
 <u>Session 2A1 - Oversampled ADCs</u>	
Design Methodology for F-Sigma-Delta Modulators	121
R. Sobot ¹ , S. Stapleton ²	
¹ University of Western Ontario, ² Simon Fraser University	

An Incremental Data Converter with an Oversampling Ratio of 3	125
T. Caldwell, D. Johns University of Toronto	
High-IF Sampling Continuous-Time Bandpass DS Modulator	129
A. Mariano, D. Dallet, Y. Deval, J-B. Begueret IXL Laboratory - University of Bordeaux	
Low Power, Third Order SD Modulator with Cross-Coupled Paths for WCDMA Applications	133
C. Della Fiore, F. Maloberti, P. Malcovati University of Pavia	
 <u>Session 2A2 - Filter Design Techniques</u>	
An Electronically Tunable Voltage-Mode Universal Filter Using Two Current Conveyors	137
M. Sagbas, M. Koksai Fatih University	
Power-Minimization Design Procedure for Rauch Biquadratic Cells	141
M. De Matteis, S. D'Amico, A. Baschiroto University of Lecce	
Design Techniques for VHF Filtering in Digital CMOS Technologies	145
A. Otin, S. Celma, C. Aldea University of Zaragoza	
Design and Comparison of CMOS CCII Based Shapers for Detector Readout Front Ends	149
T. Noulis, C. Deradonis, S. Siskos Aristotle University of Thessaloniki	
 <u>Session 2A3 - Amplifiers</u>	
Reversed Double Pole-Zero Cancellation Frequency Compensation Technique for Three-Stage Amplifiers	153
A. Grasso, D. Marano, G. Palumbo, S. Pennisi University of Catania	
Development of a Design Platform for CMOS Amplifiers	157
P. Kasturi, G. Fischer University of Rhode Island	
Common Source Amplifier with Feedback Biasing in 90nm CMOS	161
T. Singh, T. Sæther, T. Ytterdal Norwegian University of Science & Technology	
A Low-Power Adaptive Biasing CMOS Operational Amplifier with Enhanced DC-Gain	165
F. Dalena ¹ , V. Giannini ² , A. Baschiroto ² ¹ STMicroelectronics, ² University of Lecce	
A Single-Ended-to-Differential Transimpedance Amplifier for a Voice Transceiver Analog Interface	169
M. De Matteis ¹ , M. Presicce ¹ , A. Baschiroto ¹ , S. D'Amico ¹ , R. Gaggi ² , D. Giotta ² ¹ University of Lecce, ² Infiniteon Villach	

Programmable OTA Based CMOS Shaping Amplifier for X-rays Spectroscopy	173
T. Noulis ¹ , C. Deradonis ¹ , S. Siskos ¹ , G. Sarabayrouse ²	
¹ Aristotle University of Thessaloniki, ² Laboratory of Analysis and Architecture of Systems	
 <u>Session 2A4 - Analog Techniques 2</u>	
Elimination of Switch On-State Resistance Effect on a Switched-Capacitor Filter Characteristic	177
L. Dolivka, J. Hospodka	
Czech Technical University	
1.5GHz Fully Differential Latched Current Comparator with 20nA of Sensitivity	181
V. Giannini ¹ , J. Craninckx ² , B. Come ² , P. Maleovati ³ , A. Baschiroto ¹	
¹ University of Lecce, ² IMEC, ³ University of Pavia	
An Analogue CMOS Neural Circuit for Improved Sensing	185
G. Zatorre, N. Medrano, M. Sanz, P. Martinez, S. Celma	
University of Zaragoza	
 <u>Session 2B1 - Device Simulation</u>	
Automatic Wavelet Localization and Adaptive Meshing of Physical Relevances in Device Simulation	189
E. Baravelli, L. De Marchi, F. Franzè, N. Speciale	
University of Bologna	
A Novel Methodology for Defining the Boundaries of Geometrical Discontinuities in Electronic Packages	193
I. Ndip, H. Reichl, S. Guttowski	
Fraunhofer IZM	
Towards Very High Frequency Simulators for Active Device Modelling	197
G. Leuzzi, V. Stornelli	
University of L'Aquila	
VCSELs Modeling and Simulation	201
K. Minoglou ¹ , E. Kyriakis-Btzaros ¹ , G. Halkias ¹ , A. Arapoyianni ² , D. Syvridis ²	
¹ NCSR Demokritos, ² University of Athens	
 <u>Session 2B2 - CAD</u>	
An Integrated Flow from Pre-Silicon Simulation to Post-Silicon Verification	205
M. Melani ¹ , F. D'Ascoli ¹ , C. Marino ¹ , L. Fanucci ¹ , A. Giambastiani ² , A. Rocchi ² , M. De Marinis ² , A. Monterastelli ²	
¹ University of Pisa, ² SensorDynamics AG	
A Fully-Automatic CAD Toolbox for a MOS Drain Current Model and its Parameters Extraction	209
W. Prodanov, M. Valle	
University of Genoa	
LAYGEN – Automatic Layout Generation of Analog ICs from Hierarchical Template Descriptions	213
N. Lourenço ¹ , M. Vianello ² , J. Guilherme ³ , N. Horta ¹	
¹ Instituto Superior Técnico, ² University of Padova, ³ Instituto de Telecomunicações	

A New Paradigm and Associated Tools for TLM/T Modeling of MPSoCs	217
E. Viaud, F. Pêcheux Université Paris 6, Pierre et Marie Curie	
 <u>Session 2B3 - Digital Circuits</u>	
Router IP Macrocell for Radiation Tolerant SpaceWire Networking	221
M. Tonarelli, E. Petri, S. Saponara, L. Fanucci University of Pisa	
An Error-Correcting Line Encoding ASIC for a HEP Rad-Hard Multi-GigaBit Optical Link	225
G. Papotti CERN	
A VHDL Model and Implementation of a Coarse-Grain Reconfigurable Coprocessor for a RISC Core	229
C. Brunelli ¹ , F. Cinelli ² , D. Rossi ¹ , J. Nurmi ¹ ¹ Tampere University of Technology, ² University of Bologna	
Power-Delay Optimized Design of Cascaded ECL Gates	233
A. Grasso ¹ , G. Palumbo ¹ , M. Alioto ² ¹ University of Catania, ² University of Siena	
Tanh-Like Activation Function Implementation for High-Performance Digital Neural Systems	237
S. Marra, M. Iachino, F. Morabito University of Reggio Calabria	
Programmable Switch for Shared Bus Replacement	241
T. Ahonen, J. Nurmi Tampere University of Technology	
 <u>Session 2B4 - Video Processing 2</u>	
Reduced Complexity Eye Detector for Colour Images Using Harris Corners, Color Heuristics and Edge Maps	245
L. Chen, C. Grecos, M. Yang Loughborough University	
Selection of Initial Quantisation Parameter for Rate Controlled H.264 Video Coding	249
S. Beesley, A. Armstrong, C. Grecos Loughborough University	
Cellular Neural Networks for Object-Oriented Segmentation	253
G. Grassi, P. Vecchio University of Lecce	
 <u>Session 3A1 - Imagers</u>	
A Reconfigurable CMOS Imager for Real-Time, Spatio-Temporal Image Processing with On-Chip ADC	257
G. Angotzi, M. Barbaro, L. Raffo University of Cagliari	

3DJAM: A Linear CMOS Sensor for 3D Vision with Merged I-TOF and OT Techniques	261
F. Ficorella ¹ , G. Dalla Betta ¹ , L. Viarani ² , M. Perenzoni ² , D. Stoppa ² , L. Gonzo ² ¹ University of Trento, ² ITC-IRST	
Alternative Color Filter Array Layouts for Digital Photography	265
K. Gorokhovskiy, J. Flint, S. Datta Loughborough University	
A 120dB CMOS Imager with a Light Adaptive System and Digital Outputs	269
E. Labonne, G. Sicard, M. Renaudin TIMA Laboratory	
 <u>Session 3A2 - Sensor Interfaces 1</u>	
Sensitivity Analysis of a Passive Inductive Telemetry System for a Capacitive Sensor	273
M. Nowak, N. Delorme CEA-LETI	
Using an Electric Programmable Analog Array for IEEE 1451 Compliant Transducer Applications	277
O. Reimer, J. Kampe Technical University Ilmenau	
VLSI Electronics Design and Testing for the Silicon Drift Sensor System of the ALICE Experiment	281
S. Martoiu ¹ , L. Toscano ² ¹ University of Torino, ² INFN Torino	
 <u>Session 3A3 - Nyquist-Rate ADCs</u>	
Design of a 1.8V 6bits Low Power F/I CMOS A/D Converter with a Novel Folder-Reduction Technique	285
S. Hwang, M. Song Dongguk University	
DAC Nonlinearity and Residue Gain Error Correction in a Pipelined ADC Using a Split-ADC Architecture	289
I. Ahmed, D. Johns University of Toronto	
A Very Low-Power CMOS 11-b Cyclic A/D Converter with Mismatch Compensation	293
B. Bechen, T. Boom, D. Weiler, B. Hosticka Fraunhofer IMS	
Efficient Calibration through Statistical Behavioral Modeling of a High-Speed Low-Power ADC	297
P. Nuzzo ¹ , F. De Bernardinis ¹ , G. Van der Plas ² , P. Terreni ¹ ¹ University of Pisa, ² IMEC	
A 6-Bit, 1.2 GHz Interleaved SAR ADC in 90nm CMOS	301
S. Dondi, D. Vecchi, A. Boni, M. Bigi University of Parma	

Session 3A4 - Mixed-Signal Techniques

- ESD Protection Design for CMOS Integrated Circuits with Mixed-Voltage I/O Interfaces** 305
W. Chang, M. Ker
National Chiao-Tung University
- Mathematical Analysis of Digital MASH Delta-Sigma Modulators for Fractional-N Frequency Synthesizers** 309
K. Hosseini, M. Kennedy
University College Cork
- Efficient Polynomial Inversion for the Linearization of Pipeline ADCs** 313
P. Nuzzo, F. De Bernardinis, P. Terreni
University of Pisa

Session 3B1 - Modeling 1

- The O-Sequence: Representation of 3D-Floorplan Dissected by Rectangular Walls** 317
H. Ohta¹, T. Yamada², C. Kodama¹, K. Fujiyoshi¹
¹Tokyo University of Agriculture and Technology, ²Saitama University
- Hierarchical Graph-Based Sizing for Analog Cells Through Reference Transistors** 321
R. Iskander¹, M. Louerat¹, A. Kaiser²
¹Université Paris 6, Pierre et Marie Curie, ²ISEN
- A Generic Modeling Approach for Molecule-Gated Nanowire Transistors Using VHDL-AMS** 325
A. Jalabert¹, F. Clermidy¹, A. Amara²
¹CEA-LETI, ²ISEP
- A Model to Understand Current Consumption, Maximum Operating Frequency and Scaling Trends of MCML Frequency Dividers** 329
R. Nonis, E. Palumbo, P. Palestri, L. Selmi
University of Udine

Session 3B2 - Modeling 2

- Design of FPGA-Based Hardware Accelerators for On-Line Fingerprint Matcher Systems** 333
M. Fons, F. Fons, E. Cantó
Rovira i Virgili University
- A TLM Design for Verification Methodology** 337
N. Bombieri
University of Verona
- Paper Withdrawn** 341
—
—
- Quantized Conductance: an Overview From the Electronic Engineering Side** 345
D. Rondoni, J. Hoekstra
Delft University of Technology

Session 3B3 - Digital Techniques 2

- HDL Library of Processing Units for an Automatic LDPC Decoder Design** 349
G. Falcão, M. Gomes, J. Gonçalves, P. Faia, V. Silva
University of Coimbra
- Simultaneous Multi-Standard Support in Programmable Baseband Processors** 353
A. Nilsson¹, E. Tell², D. Liu¹
¹Linköping University, ²Coresonic AB
- RNS-Based Watermarking for IP Cores** 357
E. Castillo¹, U. Meyer-Baese², A. Garcia¹, L. Parrilla¹, A. Lloris¹
¹University of Granada, ²Florida State University
- Using Multiple-Valued Gates to Implement Reversible Logic** 361
O. Mirmotahari, Y. Berg, J. Lomsdalen, V. Øverås
University of Oslo
- Synchronous to Asynchronous Conversion of Digital Circuits** 365
R. Cassia¹, F. Franca¹, V. Alves²
¹Federal University of Rio de Janeiro, ²SimpleTech

Session 3B4 - Signal Processing 1

- How to Add the Integrity Checking Capability to Block Encryption Algorithms** 369
R. Elbaz¹, L. Torres¹, G. Sassatelli¹, P. Guillemin², M. Bardouillet², J. Rigaud³
¹LIRMM - UMR CNRS, ²STMicroelectronics, ³CMP-GC
- Design, Testing and Prototyping of a Software Programmable I2C/SPI IP on AMBA Bus** 373
L. Bacciarelli¹, G. Lucia¹, S. Saponara¹, L. Fanucci¹, M. Forliti²
¹University of Pisa, ²SensorDynamics AG
- A Low Power 128-Pt Implementation of FFT/IFFT for High Performance Wireless Personal Area Networks** 377
J. Mathew, K. Maharatna, D. Pradhan
University of Bristol

Session 4A1 - Sensor Interfaces 2

- Pile Up Rejection and Multiple Simultaneous Events Acquisition with the PDD ASIC** 381
A. Dragone¹, G. De Geronimo², J. Fried², A. Kandasamy², P. O'Connor², P. Siddons², E. Vernon², F. Corsi¹
¹Politecnico di Bari, ²Brookhaven National Laboratory
- A Switched Capacitor Interface for a Capacitive Microphone** 385
S. Jawed¹, M. Gottardi¹, A. Baschiroto²
¹ITC-IRST, ²University of Lecce
- ASIC for Fast and High Resolution Linear Position Measurement** 389
J. Podrzaj, A. Sesek
University of Ljubljana
- Fast Prototyping Flow for Sensor Interfaces** 393
F. Iozzi¹, L. Fanucci¹, A. Giambastiani²
¹University of Pisa, ²SensorDynamics AG

Session 4A2 - Optoelectronics

- Fabrication of Low-Threshold 1.3- μ m InAs/InGaAs/GaAs Quantum-Dot Lasers Operating at Room Temperature** 397
L. Martiradonna¹, E. De Benedetto¹, L. Fortunato¹, R. Cingolani¹, M. De Vittorio¹, A. Salhi², V. Tasco², M. De Giorgi², A. Passaseo², G. Visimberga³
¹ISUFI - University of Lecce, ²CNR-INFM, ³University of Lecce
- Parallel Chains Based Read-out System for a Compton Enhanced 3D PET Scanner** 401
A. Dragone¹, F. Corsi¹, C. Marzocca¹, V. Scarola¹, P. Losito², D. Pasqua², A. Argentieri², E. Nappi³, R. De Leo³, J. Séguinot⁴, A. Braem⁵, E. Chesi⁵, C. Joram⁵, P. Weilhammer⁵, F. Garibaldi⁶, H. Zaidi⁷
¹Politecnico di Bari, ²Microlaben, ³INFN Bari, ⁴Collège de France, ⁵CERN, ⁶Istituto Superiore di Sanità, ⁷Geneva University Hospital
- Synergies of Controller-Based LED Drivers and Quality Solid-State Lighting** 405
P. Pinho, E. Tetri, L. Halonen
Helsinki University of Technology

Paper Withdrawn 409

Session 4A3 - Sensors and Devices

- Multilayer PCB Planar Fluxgate Magnetic Sensor** 413
A. Rossini¹, A. Baschirotto², E. Dallago¹, P. Malcovati¹, M. Marchesi¹, G. Venchi¹
¹University of Pavia, ²University of Lecce
- Hard X-Ray SOI Sensor Prototype** 417
E. Martin¹, G. Varner¹, M. Barbero¹, J. Kennedy¹, H. Tajima², Y. Arai³
¹University of Hawaii, ²Stanford Linear Accelerator Center, ³KEK, High Energy Accelerator
- Integration of SAW Filter on PICS Substrate Using Polymer Sealing** 421
V. Georgel¹, F. Verjus², E. van Grunsven³, P. Poulichet⁴, G. Lissorgues⁴, S. Chamaly⁵
¹Philips Semiconductor, ESIEE, ²Philips Semiconductor, ³Philips Applied Technologies, ⁴ESIEE/ESYCOM Lab, ⁵TEMEX
- High Quality MOCVD AlGaIn/GaN Structure for HEMT Application** 425
B. Poti¹, A. Passaseo¹, M. De Vittorio¹, M. Peroni²
¹CNR-INFM, ²Selex S. I.

Session 4A4 - Sensing Systems

- A 1 cm³ Autonomous Sensor Node for Physical Activity Monitoring** 429
W. Bracke¹, P. Merken¹, R. Puers², C. Van Hoof¹
¹IMEC, ²KU Leuven
- Carbon-Monoxide (CO) Real Time Monitoring in Combustion Engines by an Optical Detection System** 433
M. Mello¹, A. De Risi², A. Passaseo¹, M. Lomascolo³, M. De Vittorio⁴
¹CNR-INFM, ²University of Lecce, ³IMM-CNR, ⁴CNRINFM
- Paper Withdrawn** 437

Bioimpedance Spectroscopy for Cell Characterization in the 50Hz-5MHz Frequency Range	441
C. Margo, J. Prado Laboratoire d'Instrumentation Electronique de Nancy	
<u>Session 4B1 - LNA and Mixers</u>	
CMOS Low-Noise Amplifier Analysis and Optimization for Wideband Applications	445
J. Kaukavuori, J. Ryyänen, K. Halonen Helsinki University of Technology	
A Wideband LNA for Wireless Multistandard Receiver in 130nm CMOS SOI Process	449
B. Martineau ¹ , C. Tinella ² , F. Gianesello ² , A. Cathelin ² , D. Belot ² , F. Danneville ³ , A. Kaiser ⁴ ¹ STMicroelectronics - IEMN, ² STMicroelectronics, ³ IEMN-CNRS, ⁴ IEMN-ISEN	
Graphical Optimization of Common-Gate LNA	453
T. Stücker, N. Christoffers, R. Kokozinski, S. Kolnsberg, B. Hosticka Fraunhofer Institute - IMS	
A 0.25-μm CMOS Low-Power Up-Conversion Mixer for 3.1-5 GHz Ultra-Wideband Applications	457
G. Sapone, G. Palmisano University of Catania	
<u>Session 4B2 - Transceivers</u>	
A Wideband FM Demodulator for UWB Applications	461
J. Gerrits ¹ , J. Farserotu ¹ , J. Long ² ¹ CSEM, ² Delft University of Technology	
UWB Receiver Design and Two-Way-Ranging Simulation Using VHDL-AMS	465
M. Crepaldi, M. Casu, M. Graziano, M. Zamboni Politecnico di Torino	
On the Design of Ultra Wideband FCC Compliant Integrated Radars	469
A. Cacciatori, L. Colalongo, Z. Kovacs Vajna University of Brescia	
A Frequency Plan Evaluation Tool for Multi-standard Wireless Transceivers	473
D. Rodríguez de Llera González ¹ , A. Rusu ¹ , M. Ismail ² ¹ Royal Institute of Technology, ² Royal Institute of Technology - Firstpass Semiconductors AB	
<u>Session 4B3 - RF Techniques</u>	
Linearity Measurements of Si/SiGe HBT Using a Large Signal Network Analyzer and an Harmonic Load-Pull Setup	477
F. Blanchet ¹ , M. El Yaagoubi ² , D. Barataud ² , J. Nebus ² , D. Pache ¹ , A. Giry ¹ ¹ STMicroelectronics, ² Xlim	
A 24-GHz Automotive Radar Transmitter with Digital Beam Steering in 130-nm CMOS	481
J. Wernehag, H. Sjöland Lund University	
The Effect of 1/f Noise on the Spectrum and the Jitter of a Free Running Oscillator	485
M. Grözing, M. Berroth University of Stuttgart	

Impact of Scaling on CMOS Radio Frequency Class-E Power Amplifiers	489
R. Brama ¹ , L. Larcher ¹ , A. Mazzanti ¹ , F. Svelto ² ¹ University of Modena and Reggio Emilia, ² University of Pavia	
<u>Session 4B4 - Signal Processing 2</u>	
T-Proc: An Embedded IEEE1500-Wrapped Cores Tester	493
M. Tuna, M. Benabdenbi, A. Greiner Université Paris 6, Pierre et Marie Curie	
Lightweight Time Encoded Signal Processing for Vehicle Recognition in Sensor Networks	497
G. Mazarakis, J. Avaritsiotis National Technical University of Athens	
On Checking Causality of Bandlimited Sampled Frequency Responses	501
P. Triverio, S. Grivet-Talocia Politecnico di Torino	
A Unified Synchronization Algorithm for OFDM Systems in Multipath Fading Channel	505
W. Chin, S. Chen National Chiao Tung University	
<u>Author Index</u>	509