

Proceedings of  
The 18th International Symposium on  
Power Semiconductor Devices & ICs

June 4<sup>th</sup>-8<sup>th</sup>, 2006

University of Naples Federico II  
Naples, ITALY

On the front cover:

Giovan Battista Lusieri, Veduta di Napoli con il borgo di Chiaia e Castel dell'Ovo

Cover page design: Antea Andriello

Proceedings of The 18th International Symposium on Power Semiconductor Devices & ICs

Copyright and Reprint Permission: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law, for private use of patrons, those articles in this volume that carry a code at the bottom of the first page, provided that the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. Other copying, reprint, or reproduction requests should be addressed to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331. All rights reserved.

Copyright © 2006 by the Institute of Electrical and Electronics Engineers, Inc.

IEEE Catalog Number: 06CH37817

ISBN: 1-4244-9714-2

Library of Congress: 2006927015

# TECHNICAL SESSIONS

**Monday, June 5<sup>th</sup> 2006**

## Plenary Sessions

Chair: Paolo Spirito – University of Naples "Federico II"  
Claudio Contiero – ST Microelectronics, Italy  
M.K. Han Seoul National University, Korea

- P-1 **Future Trend of Flat Panel Displays and Comparison of its Driving Methods**  
SHUICHI UCHIKOGA  
Toshiba Corporation, Corporate R & D Center, JAPAN xxvii
- P-2 **Power Drive Circuits for Diagnostic Medical Ultrasound**  
BRUNO HAIDER  
General Electric, Niskayuna, USA xxxiii
- P-3 **Trend and Challenges in Automotive Electronics**  
VALENTIN VON TILS  
Robert Bosch GmbH, GERMANY xl

## Session 1: Diodes and IGBT

Chair: Daniel Kinzer - International Rectifier, USA  
Stefan Linder - ABB, Switzerland

- 1-1 **Mechanical stress dependence of power device electrical characteristics**  
HIROAKI TANAKA, KOJI HOTTA, SATOSHI KUWANO, MASANORI USUI\*, MASAYASU ISHIKO\*  
TOYOTA MOTOR Corp., , Aichi, JAPAN  
\*TOYOTA CENTRAL R&D LABS. INC. Nagakute, Aichi, JAPAN 1
- 1-2 **Theoretical investigation of Silicon limit characteristics of IGBT**  
AKIO NAKAGAWA  
Semiconductor Company, Toshiba Corporation, Japan 5
- 1-3 **A novel diode structure with Controlled Injection of Backside Holes (CIBH)**  
MIN CHEN, JOSEF LUTZ, MARTIN DOMEIJ, HANS PETER FELSL\*, HANS-JOACHIM SCHULZE\*  
Chemnitz University of Technology, Chemnitz, Germany  
\*KTH Stockholm, 2Infineon Technologies AG, Munich 9
- 1-4 **Electro-thermal simulation of current filamentation in 3.3-kV silicon p-i-n diodes with different edge terminations**  
H. P. FELSL, E. FALCK, F. J. NIEDERNOSTHEIDE, \*S. MILADY, \*D. SILBER AND \*\*J. LUTZ  
Infineon Technologies AG, Munich, Germany  
\* University of Bremen, Germany  
\*\* Chemnitz University of Technology, Germany 13

## Session 2: IGBT 2

Chair: Thomas Stockmeier - Semikron, Germany  
Yasukazu Seki - Fuji Hitachi Power Semiconductor, Japan

- 2-1 **A Landmark in Electrical Performance of IGBT Modules Utilizing Next Generation Chip Technologies**  
A. KOPTA, M. RAHIMO, S. EICHER, U. SCHLAPBACH  
ABB Switzerland Ltd, Semiconductors, Lenzburg, Switzerland 17
- 2-2 **Source Side Thermal Runaway of Trench IGBTs, Dependence on Design Aspects**  
ANDREAS MÜLLER-DAUCH\*, FRANK PFIRSCH, MANFRED PFAFFENLEHNER, DIETER SILBER\*  
\*University of Bremen, Bremen, Germany  
Infineon Technologies, Munich, Germany 21
- 2-3 **A New Stored-Charge-Controlled Over-Voltage Protection Concept for Wide RBSOA in High-Voltage Trench-IEGTs**  
TSUNEO OGURA, KOICHI SUGIYAMA, ICHIRO OMURA, MASAKAZU YAMAGUCHI,  
SATOSHI TERAMAE, NOBUAKI YAMANO AND SUSUMU IESAKA  
Discrete Semiconductor Division, Toshiba Corporation, Japan 25
- 2-4 **A new isolation technique for reverse blocking IGBT with ion implantation and laser annealing to tapered chip edge sidewalls.**  
KAZUO SHIMOYAMA, MANABU TAKEI, YASUHISA SOUMA, AYAKO YAJIMA, SATOMI KAJIWARA  
AND HARUO NAKAZAWA.  
Fuji Electric Advanced Technology, Co. Ltd., Nagano, Japan 29
- 2-5 **Novel Enhanced-Planar IGBT technology rated up to 6.5kV, Lower Losses and Higher SOA Capability**  
M. RAHIMO, A. KOPTA, S. LINDER  
ABB Switzerland Ltd, Semiconductors, Lenzburg, Switzerland 33

## Tuesday, June 6<sup>th</sup> 2006

### Session 3: RF power and modeling

Chair: Vishnu Khemka - Freescale Semiconductor, USA  
Florin Udrea - Cambridge University, UK

- 3-1 **A Complementary RF-LDMOS Architecture Compatible with 0.13micron CMOS Technology**  
NIHAR R. MOHAPATRA, H. RUECKER, K. E. EHWALD, R. SORGE, R. BARTH, P. SCHLEY, D. SCHMIDT AND H. E. WULF  
IHP, Frankfurt (Oder), Germany 37
- 3-2 **Enhancing commercial CAD tools toward the electrothermal simulation of power transistors**  
F. M. DE PAOLA, V. D'ALESSANDRO, G. BREGGIO, N. RINALDI, AND P. SPIRITO  
Department of Electronics and Telecommunications Engineering  
University of Naples "Federico II", Naples, Italy 41
- 3-3 **Modeling and Analysis of Metal Interconnect Resistance of Power MOSFETs with Ultra Low On-Resistance**  
Y. CHEN, X. CHENG, Y. LIU, Y. FU, T. X. WU, AND Z. J. SHEN  
School of Electrical Engineering and Computer Science, University of Central Florida, Orlando, USA 45
- 3-4 **Trade-offs in RF Performance and Electrothermal Ruggedness of Multifinger SiGe Power Cells**  
M. SPIRITO\*, F. M. DE PAOLA\*\*, V. D'ALESSANDRO\*\*, K. BUISMAN\*, AND N. RINALDI\*  
\*HiTeC Laboratory, Delft University of Technology, Delft, The Netherlands  
\*\* University of Naples "Federico II", Naples, Italy. 49

## Session 4: Low voltage Si MOS

Chair: Mohamed Darwish - Fultec Semiconductor, USA  
C. Andre T. Salama - University of Toronto, Canada

- 4-1 **20V-40V Vertical Trench nMOS design for display driver**  
M. ANNESE, P. MONTANINI, F. TOIA, L. ZULLINO, C. CONTIERO  
STMicroelectronics, Italy 53
- 4-2 **Substrate deep depletion: an innovative design concept to improve the voltage rating of SOI power devices**  
ETTORE NAPOLI, FLORIN UDREA\*  
Electronic and Telecom. Engineering dept. University of Napoli, Napoli Italy  
\* Department of Engineering University of Cambridge, Cambridge, UK  
\* Cambridge Semiconductor (Camsemi), Cambridge, UK 57
- 4-3 **Break-through of the Si limit under 100V breakdown voltage with Super 3D MOSFET**  
HITOSHI YAMAGUCHI, YASUSHI URAKAMI AND JUN SAKAKIBARA  
DENSO CORPORATION, Japan 61
- 4-4 **200V Super Junction MOSFET Fabricated by High Aspect Ratio Trench Filling**  
SHOICHI YAMAUCHI, TAKUMI SHIBATA, SHOJI NOGAMI\*, TOMONORI YAMAOKA\*,  
YOSHIYUKI HATTORI\*\* AND HITOSHI YAMAGUCHI  
DENSO CORPORATION, Nissin, Aichi, 470-0111, Japan  
\*SUMCO CORPORATION, Japan  
\*\*TOYOTA CENTRAL R&D LABS., Japan 65

## Session 5: Diamond devices

Chair: Gehan Amaratunga Cambridge University, UK  
Anant Agarwal – Cree, USA

- 5-1 **RF diamond MISFETs using surface accumulation layer**  
K. HIRAMA, T. KOSHIBA, K. YOHARA, H. TAKAYANAGI, S. YAMAUCHI, M. SATOH, H. KAWARADA  
Waseda University, Okubo 3-4-1, Shinjyuku-ku, Tokyo, Japan 69
- 5-2 **Termination structures for diamond Schottky barrier diodes**  
M. BREZEANU<sup>1</sup>, M.AVRAM<sup>2</sup>, S. J. RASHID<sup>1</sup>, G. A. J. AMARATUNGA<sup>1</sup>, T. BUTLER<sup>1</sup>, N. L. RUPESINGHE<sup>1</sup>, F. UDREA<sup>1</sup>, A. TAJANI<sup>3</sup>, M. DIXON<sup>3</sup>, D. J. TWITCHEN<sup>3</sup>, A. GARRAWAY<sup>4</sup>, D. CHAMUND<sup>4</sup>, P. TAYLOR<sup>4</sup>, G. BREZEANU<sup>5</sup>  
<sup>1</sup>Department of Engineering, University of Cambridge, , UK  
<sup>2</sup>National Institute for R&D in Microtechnology (IMT-Bucharest), Romania  
<sup>3</sup>Element Six Ltd., King's Ride Park, Ascot, UK  
<sup>4</sup>Dynex Semiconductor Ltd., Lincoln, UK  
<sup>5</sup>University Politehnica Bucharest, Bucharest, Romania 73

## Session 6: Poster Session

- 6-1 **High density MOSBD (UMOS with built-in Trench Schottky Barrier Diode) for Synchronous Buck Converters**  
SYOTARO ONO, YOSHIHIRO YAMAGUCHI, NOBORU MATSUDA, AKIO TAKANO, MIWAKO AKIYAMA, YUSUKE KAWAGUCHI, AND AKIO NAKAGAWA  
Toshiba Corporation Semiconductor Company, Japan 77
- 6-2 **Reverse recovery in high density trench MOSFETs with regard to the body effect**  
TONI LÓPEZ, REINHOLD ELFERICH AND NICK KOPER\*  
PHILIPS RESEARCH LABORATORIES, AACHEN, GERMANY  
\*Philips Semiconductors, Stockport (Hazel Grove), United Kingdom 81
- 6-3 **High Performance and Reliability Trench Gate Power MOSFET with Partially Thick Gate Oxide Film Structure (PTOx-TMOS)**  
TAKA AKI AOKI, YUKIO TSUZUKI, SHOJI MIURA, YOSHIFUMI OKABE, MIKIMASA SUZUKI AND AKIRA KUROYANAGI  
DENSO CORPORATION, Japan 85
- 6-4 **Two-carrier current saturation in a lateral dmos**  
JOHN LIN AND PHILIP L HOWER  
Texas Instruments Inc, USA 89
- 6-5 **A new principle for self-protecting array design**  
V.A. VASHCHENKO AND P.J. HOPPER  
National Semiconductor Corporation, USA 93
- 6-6 **Accurate Large-Signal Modeling of AlGa<sub>N</sub>-Ga<sub>N</sub> HEMT Including Trapping and Self-Heating Induced Dispersion**  
ANWAR JARNDAL, BERND BUNZ AND GÜNTER KOMPA  
University of Kassel, Fachgebiet Hochfrequenztechnik, Kassel, Germany 97
- 6-7 **Self-aligned High Density Low Voltage P-channel Trench MOSFET with Ultra low Resistance and Robust Ruggedness**  
CHRISTOPHER KOCON, ASHOK CHALLA, PAUL THORUP  
Fairchild Semiconductor, USA 101
- 6-9 **Evaluation of Ga<sub>N</sub> HEMT Technology Development Through Nonlinear Characterization**  
A.ANGELINI, V.CAMARCHIA, F.CAPPELLUTI, S.DONATI GUERRIERI, M.PIROLA, F.BONANI, A.SERINO\* AND G.GHIONE  
Politecnico di Torino, Dipartimento di Elettronica, Torino, Italy  
\*Università di Roma "TorVergata", Dipartimento di Elettronica, Roma, Italy 105
- 6-10 **Industrialisation of Resurf Stepped Oxide Technology for Power Transistors**  
M. A. GAJDA, S. W. HODGSKISS, L. A. MOUNFIELD, N. T. IRWIN, G. E. J. KOOPS\*, R. VAN DALEN\*  
Philips Semiconductors, Stockport, United Kingdom  
\*Philips Research Europe, Kapeldreef 75, B-3001 Leuven, Belgium. 109
- 6-11 **Mechanism and Control Technology of Trench Corner Rounding by Hydrogen Annealing for Highly Reliable Trench MOSFET**  
RYOSUKE SHIMIZU, HITOSHI KURIBAYASHI\*, REIKO HIRUTA\*, KOICHI SUDOH\*\* AND HIROSHI IWASAKI\*\*  
Material and Science Laboratory, Fuji Electric Advanced Technology Co., Japan  
\*Device Technology Laboratory, Fuji Electric Advanced Technology Co., Japan  
\*\*Institute of Scientific and Industrial Research, Osaka University, Japan 113
- 6-12 **Low Specific On-Resistance AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT on Sapphire Substrate**  
MASAKI INADA, SHUICHI YAGI, YUKI YAMAMOTO, GUANXI PIAO, MITSUAKI SHIMIZU, HAJIME OKUMURA AND KAZUO ARAI, YOSHIKI YANO AND NAKAO AKUTSU  
National Institute of Advanced Industrial Science and Technology, Japan  
Taiyo Nippon Sanso Corporation, Japan 117

6-13	<p><b>4.5kV 120A SICGT and Its PWM Three Phase Inverter Operation of 100kVA</b>  Y.SUGAWARA, Y.MIYANAGI, K.ASANO, A.AGARWAL*, S.RYU, J.PALMOUR*, Y.SYOJI**,  S.OKADA, S.OGATA, T.IZUMI  Kansai Electric Power Co., Nakoji, Japan  * CREE Inc., Durham, USA  ** Asahi Denka Co., Tokyo, Japan</p>	121
6-14	<p><b>Low on-resistance in inversion channel IEMOSFET formed on 4H-SiC C-face substrate</b>  S. HARADA, M. KATO, M. OKAMOTO, T. YATSUO, K. FUKUDA, K. ARAI  National Institute of Advanced Industrial Science and Technology, Japan</p>	125
6-15	<p><b>Active Fuse</b>  S. E. BERBERICH, M. MÄRZ, A.J. BAUER, S.K. BEUER, H. RYSSEL  Fraunhofer Institute of Integrated Systems and Device Technology (IISB)  Erlangen, Germany</p>	129
6-16	<p><b>The Second Stage of a Thin Wafer IGBT Low Loss 1200V LPT-CSTBT with a Backside Doping Optimization Process</b>  KATSUMI NAKAMURA, YOSHIAKI HISAMOTO, TAMIO MATSUMURA, TADAHARU MINATO AND JUNICHI MORITANI  Power Device Works, Mitsubishi Electric Corporation, Japan</p>	133
6-17	<p><b>Fast Recovery Diode with Novel Local Lifetime Control</b>  J. VOBECKÝ AND P. HAZDRA  Microelectronics Dept., Czech Technical University, Prague, Czech Republic</p>	138
6-18	<p><b>High current gain silicon carbide bipolar power transistors</b>  MARTIN DOMEIJ, HYUNG-SEOK LEE, CARL-MIKAEL ZETTERLING, MIKAEL ÖSTLING AND ADOLF SCHÖNER*  KTH Royal Institute of Technology, Electrum 229, S-16440 Kista-Stockholm, Sweden  *Acree AB, Electrum 236, S-16440 Kista-Stockholm, Sweden</p>	141
6-19	<p><b>Analysis of Dynamic Avalanche Phenomenon of PiN Diode Using He Ion Irradiation</b>  TADASHI MISUMI, SHINJI NAKAGAKI, MASAKAZU YAMAGUCHI*, KOICHI SUGIYAMA*  FUMIO HIRAHARA* AND KATSUHIKO NISHIWAKI  Toyota Motor Corporation, Toyota, Aichi 470-0309, Japan  *Discrete Semiconductor Division, Toshiba Corporation, Kawasaki, Japan</p>	145
6-20	<p><b>Characterization of Unconventional Engineering Solutions for Superjunction Devices</b>  M. BUZZO*, **, M. CIAPPA**, M. RUEB*, AND W. FICHTNER**  *Infineon Technologies, Villach, Austria  **Swiss Federal Institute of Technology (ETH), Zurich, Switzerland</p>	149
6-21	<p><b>Helium implantation in silicon: detailed experimental analysis of resistivity and lifetime profiles as a function of the implantation dose and energy</b>  S.DALIENTO, L. MELE, P.SPIRITO, L.GIALANELLA*, M.ROMANO*, B.N.LIMATA*, R. CARTA** L. BELLEMO**  University of Napoli "Federico II" Napoli, Italy  * Dipartimento di Scienze Fisiche e INFN Napoli, Napoli, Italy  ** International Rectifier Corporation Italiana, Borgaro (TO), Italy</p>	153
6-22	<p><b>Dynamic Behavior of High-Power Diodes Analyzed by EBIC</b>  A. PUGATSCHOW, T. GEINZER, R. HEIDERHOFF, F.-J. NIEDERNOSTHEIDEÉ, H.-J. SCHULZE*, B. WIEDENHORST**, L.J. BALK  BERGISCHE UNIVERSITÄT WUPPERTAL, WUPPERTAL, GERMANY  *INFINEON TECHNOLOGIES AG, MÜNCHEN, GERMANY  **INFINEON AG, WARSTEIN, GERMANY</p>	157

6-23	<p><b>High temperature characterization of 4H-SiC normally-on vertical JFETs with buried gate and buried field rings</b>  A. MIHAILA, F. UDREA, S. J. RASHID, P. GODIGNON*, P. BROSSELDARD*, D. TOURNIER*, J. MILLAN*, G. AMARATUNGA  Engineering Department, Cambridge University, Cambridge, UK  *CNM, Campus Universidad Autonoma de Barcelona, Barcelona, Spain</p>	161
6-24	<p><b>Influence of layout geometries on the behavior of 4H-SiC 600 V Merged PiN Schottky (MPS) rectifiers</b>  V. D'ALESSANDRO*, A. IRACE*, G. BREGLIO*, P. SPIRITO*, A. BRICCONI**, R. CARTA**, D. RAFFO**, AND L. MERLIN**  *Department of Electronics and Telecommunications Engineering, University of Naples "Federico II", Naples, Italy  **IRCI-International Rectifier Corporation Italia, Turin, Italy</p>	165
6-25	<p><b>Silicon Dioxide Passivation of AlGaIn/GaN HEMTs for High Breakdown Voltage</b>  MIN-WOO HA, SEUNG-CHUL LEE, JOONG-HYUN PARK, JIN-CHERL HER, KWANG-SEOK SEO, AND MIN-KOO HAN  School of Electrical Engineering, Seoul National University, Korea</p>	169
6-26	<p><b>Investigation of carrier streaming effect for the low spike fast IGBT turn-off</b>  Y.ONOZAWA, M.OTSUKI AND Y.SEKI*  Fuji Electric Device Technology Co., Ltd., Nagano, Japan  *Fuji Electric Advanced Technology Co., Ltd., Nagano, Japan</p>	173
6-27	<p><b>High performance AlGaIn/GaN HEMT switches employing 500°C oxidized Ni/Au gate for very low leakage current and improvement of uniformity</b>  SEUNG-CHUL LEE, JIYONG LIM, MIN-WOO HA, JIN-CHERL HER, CHONG-MAN YUN*, AND MIN-KOO HAN  School of Electrical Engineering, Seoul National University, Korea  * Fairchild Semiconductor, Korea</p>	177
6-28	<p><b>Fabrication of Monolithic Bidirectional Switch (MBS) devices with MOS-controlled emitter structures</b>  M. BAUS*, B. N. SZAFRANEK*, ST. CHMIELUST†, M. C. LEMME‡, B. HADAM*, B. SPANGENBERG*, R. SITTIG† AND H. KURZ*‡  *Institut fur Halbleitertechnik, RWTH-Aachen, Aachen, Germany,  †Institut fur Halbleitertechnik, TU-Braunschweig, Braunschweig, Germany  ‡AMICA/AMO GmbH, Aachen, Germany</p>	181
6-29	<p><b>Experimental demonstration of a 1.2kV trench clustered insulated gate bipolar transistor in non punch through technology</b>  K. VERSHININ*, M. SWEET*, L. NGWENDSON*, JIM THOMSON**, P. WAIND**, J. BRUCE***AND E. M. SANKARA NARAYANAN*  *Emerging Technologies Research Centre, De Montfort University, Leicester, UK  **Dynex Semiconductor, Lincoln, UK  ***Semefab (Scotland) Ltd, Glenrothes, Fife, UK</p>	185
6-30	<p><b>The Optimized Monolithic Fault Protection Circuit for the Soft-shutdown behavior of 600V PT-IGBT by employing a New Blanking Filter</b>  IN-HWAN JI, YOUNG-HWAN CHOI, SOO-SEONG KIM*, KWANG-HOON OH* AND MIN-KOO HAN  School of Electrical Eng., Seoul Nat'l Univ., Korea  * Fairchild Semiconductor, Korea</p>	189
6-32	<p><b>Problems on the SRH Recombination Model and a Proposed Solution</b>  IKUNORI TAKATA  Mitsubishi Electric Corporation, Japan</p>	193
6-33	<p><b>Advanced 100V, 0.13um BCD process for next generation automotive applications</b>  PIET WESSELS, MAARTEN SWANENBERG, JAN CLAES, ERIC R. OOMS.  Philips Semiconductors, Nijmegen, The Netherlands.</p>	197



6-35	<b>A 75 V Lateral IGBT for Junction-Isolated Smart Power Technologies</b> B. BAKEROOT, J. DOUTRELOIGNE, AND P. MOENS* GHENT UNIVERSITY, GHENT, BELGIUM *AMI SEMICONDUCTOR BELGIUM BVBA, OUDENAARDE, BELGIUM	201
6-36	<b>Improved dielectric isolation HVIC technology (SODI) in Transfer Mold Package</b> H.AKIYAMA, N.YASUDA, J.MORITANI, K.TAKANASHI, AND G.MAJUMDAR Mitsubishi Electric Corporation, Japan	205
6-37	<b>Numerical Simulations for Electromagnetic Power Module Design</b> DIDIER COTTET, SAMUEL HARTMANN, ULRICH SCHLAPBACH* ABB SWITZERLAND LTD. CORPORATE RESEARCH, SWITZERLAND * ABB SWITZERLAND LTD. SEMICONDUCTORS, SWITZERLAND	209
6-38	<b>TherMos3: a 3D electrothermal simulator for smart Power Devices</b> ANDREA IRACE, GIOVANNI BREGGIO AND PAOLO SPIRITO University of Naples "Federico II", Naples, Italy	213
6-39	<b>Power Cycling at High Temperature Swings of Modules with Low Temperature Joining Technique</b> R. AMRO <sup>1</sup> , J. LUTZ <sup>1</sup> , J. RUDZKI <sup>2</sup> , R. SITTIG <sup>3</sup> AND M. THOBEN <sup>4</sup> <sup>1</sup> CHEMNITZ UNIVERSITY OF TECHNOLOGY-GERMANY <sup>2</sup> KIEL UNIVERSITY OF APPLIED SCIENCE-GERMANY <sup>3</sup> TECHNICAL UNIVERSITY AT BRAUNSCHWEIG-GERMANY <sup>4</sup> INFINEON TECHNOLOGIES AG, WARSTEIN-GERMANY	217
6-40	<b>Fully Isolated High-Side and Low-Side LIGBTs in Junction Isolation Technology</b> DAVID W. GREEN AND E. M. SANKARA NARAYANAN Emerging Technologies Research Centre, De Montfort University, Leicester, UK	221
6-41	<b>High-Frequency Monolithic DC/DC Converter for System-on-Chip Power Management</b> VINCENT PINON, BRUNO ALLARD*, CHRISTOPHE GARNIER STMicroelectronics, Crolles, France *CEGELY, INSA de Lyon	225
6-42	<b>Technology for Power Integrated Circuits with Multiple Vertical Power Devices</b> PETAR IGIC, PAUL HOLLAND, STEVE BATCUP, RALF LERNER* AND ANDREAS MENZ** Electronics Systems Design Centre, University of Wales, Swansea, UK *X-FAB Semiconductor Foundries, Erfurt, Germany ** Protron Mikrotechnik GmbH, Bremen, Germany	229
6-43	<b>Design and Optimization of a Versatile 700 V SPIC Process Using a Fully Implanted Triple-well Technology</b> WANJUN CHEN, BO ZHANG, ZEHONG LI, ZHAOJI LI, XIAOCHUAN DENG, JIANBING CHENG University of Electronic Science and Technology of China, Chengdu, P. R. China	233
6-44	<b>High efficiency Piezoelectric Transformer Driver in BCD6-20V technology, generating up to positive or negative 1700V output voltage, from 1V input supply</b> GIULIO RICOTTI, ALBERTO DANIONI STMicroelectronics, Italy	237
6-45	<b>Monolithic integrated over voltage protection circuits For Power MOSFET and IGBT – topology, validation and thermal analysis</b> F. ALKAYAL, J-C CREBIER, C. SCHAEFFER LEG - ENSIEG, INPG, St Martin d'Hères, France	241
6-46	<b>interaction analysis and insulation techniques for short-circuit integrated protection structure</b> C.CARAMEL, P.AUSTIN, J-L. SANCHEZ, E. IMBERNON, B. ROUSSET LAAS-CNRS, Toulouse, France	245

6-47	<b>Investigations of all lead free IGBT module structure with low thermal resistance and high reliability</b> Y.NISHIMURA, A.MOROZUMI, E.MOCHIZUKI, AND Y.TAKAHASHI Fuji Electric Device Technology Co., Ltd., Nagano, Japan	249
6-48	<b>JFET Transistor used for power devices integrated over voltage protection</b> L.VINCENT, B. NGUYEN-DAC, J-C CREBIER, F. ALKAYAL, C. SCHAEFFER LEG - ENSIEG, INPG, St Martin d'Hères, France	253
6-49	<b>Analytical design rules for field compensated structures (paper not available at the time of proceedings print)</b> IGOR SANKIN	
6-50	<b>Fast transient infrared thermal analysis of smart Power MOSFETs in permanent short circuit operation</b> G. BREGLIO*, A. IRACE*, P. SPIRITO*, R. LETOR*, S. RUSSO**. * DIET, UNIVERSITY OF NAPLES FEDERICO II, NAPLES, ITALY **STMICROELECTRONICS CATANIA, CATANIA, ITALY	257

### Wednesday, June 7<sup>th</sup> 2006

#### **Session 7: SiC Unipolar**

Chair: Jose Millan - CNM, Spain  
Masakatsu Hoshi - Nissan, Japan

7-1	<b>Successful Development of 1.2 kV 4H-SiC MOSFETs with the Very Low On-Resistance of 5 mohmcm<sup>2</sup></b> NARUHISA MIURA, KEIKO FUJIHIRA, YUKIYASU NAKAO, TOMOKATSU WATANABE, YOICHIRO TARUI, SHIN-ICHI KINOUCHI, MASAYUKI IMAIZUMI AND TATSUO OOMORI Advanced Technology R&D Center, Mitsubishi Electric Corporation, Japan	261
7-2	<b>10 kV, 5A 4H-SiC Power DMOSFET</b> SEI-HYUNG RYU, SUMI KRISHNASWAMI, BRETT HULL, JAMES RICHMOND, ANANT AGARWAL, AND ALLEN HEFNER* Cree, Inc., Durham, USA *Natnl. Inst. of Standards and Tech., USA	265
7-3	<b>„2nd Generation“ SiC Schottky diodes: A new benchmark in SiC device ruggedness.</b> ROLAND RUPP <sup>1</sup> , MICHAEL TREU <sup>2</sup> , STEPHAN VOSS <sup>1</sup> , FANNY BJÖRK <sup>2</sup> , TOBIAS REIMANN <sup>3</sup> <sup>1</sup> Infiniteon Technologies AG Munich, Germany <sup>2</sup> Infiniteon Technologies AG Villach, Austria <sup>3</sup> ISLE Steuerungstechnik und Leistungselektronik GmbH Ilmenau, Germany	269
7-4	<b>Dose designing and fabrication of 4H-SiC double RESURF MOSFETs</b> M. NOBORIO, J. SUDA, AND T. KIMOTO Department of Electronic Science and Engineering, Kyoto University, Japan	273

#### **Session 8: SiC Bipolar**

Chair: P. Chow - Rensselaer Polytechnic Institute, USA  
Jean L. Sanchez - LAAS-CNRS, France

8-1	<b>A 180 A/4.5 kV 4H-SiC PiN Diode for High Current Power Modules</b> BRETT A. HULL, MRINAL K. DAS, JAMES T. RICHMOND, JOSEPH J. SUMAKERIS, ROBERT LEONARD, JOHN W. PALMOUR, AND SCOTT LESLIE* Cree, Inc., Durham, USA *Powerex, Inc., Youngwood, USA	277
-----	--	-----

- 8-2 **Analysis of SiC BJTs RBSOA**  
 Y. GAO, A. Q. HUANG, B. CHEN, A. K. AGARWAL\*, S. KRISHNASWAMI\*, C. SCOZZIE#  
 North Carolina State University, Raleigh, USA  
 \* Cree Inc, Durham, USA  
 # US Army Research Laboratory, 2800 Powder Mill Road, Adelphi, USA 281
- 8-3 **Design and Fabrications of High Voltage IGBTs on 4H-SiC**  
 QINGCHUN ZHANG, CHARLOTTE JONAS, SEI-HYUNG RYU, ANANT AGARWAL AND JOHN PALMOUR  
 Cree, Inc. , Durham, USA 285
- 8-4 **4 kV, 10 A Bipolar Junction Transistors in 4H-SiC**  
 SUMI KRISHNASWAMI, ANANT AGARWAL, JAMES RICHMOND, T. PAUL CHOW\*,  
 BRUCE GEIL\*\*, KEN JONES\*\*, AND CHARLES SCOZZIE\*\*  
 Cree, Inc., 4600 Silicon Drive, USA  
 \*Rensselaer Polytechnic Institute, USA  
 \*\*Army Research Laboratory, USA 289

### Session 9: SuperJunction devices

Chair: D. Pattanayak - Vishay-Siliconix, USA  
 L. Lorenz - Infineon Technologies, Germany

- 9-1 **A 15.5 mOhmcm<sup>2</sup>-680V Superjunction MOSFET Reduced On-Resistance by Lateral Pitch Narrowing**  
 WATARU SAITO, ICHIRO OMURA, SATOSHI AIDA, SHIGEO KODUKI, MASARU IZUMISAWA,  
 HIRONORI YOSHIOKA, HIDEKI OKUMURA, MASAKAZU YAMAGUCHI AND TSUNEO OGURA  
 Toshiba Corp. Semiconductor Company, Kawasaki, Japan 293
- 9-2 **20mohm-cm<sup>2</sup> 660V Super junction MOSFETs fabricated by deep trench etching and epitaxial growth**  
 K. TAKAHASHI, H. KURIBAYASHI, T. KAWASHIMA, S. WAKIMOTO, K. MOCHIZUKI AND H. NAKAZAWA  
 Fuji Electric Advanced Technology Co., Ltd., Nagano, Japan 297
- 9-3 **Electrical and Physical Characterization of 150-200V FLYMOSFETs**  
 JAUME ROIG, YANN WEBER\*, J-M. REYNÈS, F. MORANCHO, E. STEFANOV, M. DILHAN,  
 G. SARRABAYROUSE  
 LAAS / CNRS, Toulouse, France  
 Freescale Semiconducteurs France SAS, Toulouse, France 301
- 9-4 **A 600V, 8.70hmm<sup>2</sup> Lateral Superjunction Transistor**  
 M.RÜBA, M.BÄRA , G.DEMLB\*, H. KAPELSC\*\*, M.SCHMITTC\*\*, S.SEDLMAIERC\*\*,  
 C.TOLKSDORFC\*\*, A.WILLMEROHC\*\*  
 INFINEON TECHNOLOGIES AUSTRIA AG, VILLACH  
 \*INFINEON ASIA PACIFIC PTE. LTD., SINGAPORE  
 \*\*INFINEON TECHNOLOGIES AG, NEUBIBERG 305

### Session 10: GaN devices

Chair: H.R. Chang ASCE Power, USA  
 P. Mawby University of Wales Swansea, UK

- 10-1 **Enhancement-Mode n-Channel GaN MOSFETs on p and n- GaN/Sapphire substrates**  
 W. HUANG, T. KHAN AND T. P. CHOW  
 Center for Power Electronics Systems, Rensselaer Polytechnic Institute, USA 309

10-2	<b>High temperature operation AlGaIn/GaN HFET with a low on-state resistance, a high breakdown voltage and a fast switching capability</b> TAKEHIKO NOMURA, KAMBAYASHI HIROSHI, MITSURU MASUDA, SONOMI ISHII, NARIAKI IKEDA AND SEIKOH YOSHIDA The Furukawa Electric Co., Ltd., Yokohama, Japan	313
10-3	<b>Fabrication of an AlGaIn/GaN HFET with a high breakdown voltage of over 1050 V</b> S. YOSHIDA, J. LI, H. TAKEHARA, H. KAMBAYASHI, AND N. IKEDA The Furukawa Electric Co., Ltd., Yokohama, Japan	317
10-4	<b>GaN Switching Devices For High-Frequency, KW Power Conversion</b> K. S. BOUTROS, S. CHANDRASEKARAN, W.B. LUO, AND V. MEHROTRA Rockwell Scientific Company LLC, , Thousand Oaks, CA, USA	321

### **Thursday, June 8<sup>th</sup> 2006**

#### **Session 11: Integration - power devices**

Chair: T. Efland - Texas Instruments, USA, Chair  
W.T. Ng - University of Toronto, Canada

11-1	<b>Novel power transistor design for a process independent high voltage option in standard CMOS</b> A. HERINGA AND J. ŠONSKÝ Philips Research Leuven, Leuven, Belgium	325
11-2	<b>Low gate charge 20V class trench-aligning lateral power MOSFET</b> S. MATSUNAGA, M. SAWADA, A.SUGI, K. TAKAGIWA AND N. FUJISHIMA Device Technology Laboratory, Fuji Electric Advanced Technology, Nagano, Japan	329
11-3	<b>Stepped-Drift LDMOSFET: A Novel Drift Region Engineered Device for Advanced Smart Power Technologies</b> R. ZHU, V. KHEMKA, A. BOSE, T. ROGGENBAUER Freescale Semiconductor, , Tempe, USA	333
11-4	<b>Experimental Implementation and Characterization of a CMOS Compatible Buffered Super Junction LDMOST</b> IL-YONG PARK AND C. ANDRE T. SALAMA Edward S. Rogers Sr. Dept. of ECE, University of Toronto, Toronto, Canada	337

#### **Session 12: Integration technology 1**

Chair: J. Sin - Hong Kong University of Science and Technology, China  
S. Ekkanath Madathil - De Montfort University, UK

12-1	<b>Wide Voltage Power Device Implementation in 0.25um SOI BiC-DMOS</b> T. NITTA, S. YANAGI, T. MIYAJIMA*, K. FURUYA*, Y. OTSU*, H. ONODA, AND K. HATASAKO RENESAS TECHNOLOGY CORP. JAPAN * Renesas Semiconductor Engineering Corp., Japan	341
12-2	<b>LDMOSFETs with Current Diverter for Advanced Smart Power Technologies</b> VISHNU KHEMKA, RONGHUA ZHU, TODD ROGGENBAUER AND AMITAVA BOSE SMARTMOS Technology Center, Freescale Semiconductor, USA	345

- 12-3 **High Voltage (up to 20V) Devices Implementation in 0.13 um A035 BiCMOS Process Technology for System-On-Chip (SOC) Design**  
R. PAN, B. TODD, P. HAO, R. HIGGINS, D. ROBINSON, V. DROBNY, W. TIAN, J. WANG, J. MITROS, M. HUBER, S. PILLAI AND S. PENDHARKAR  
Texas Instruments Inc., , Dallas, USA 349
- 12-4 **High Voltage CMOS Line-up for Display Driver Applications based on 0.13µm CMOS with Aluminum metallization Scheme**  
TAKAHIRO OOHORI, HIROSHI SAITO\*, HIDEHIKO KAMIZONO, HIROYUKI MIYAKAWA AND TOSHIRO KUBOTA  
Toshiba Corporation Semiconductor Company, Japan 353

### Session 13: Integration technology 2

Chair: R. Zhu Freescale Semiconductor, USA  
D. Disney Advanced Analogic Technologies, USA

- 13-1 **650V SOI LIGBT for Switch Mode Power Supply Application**  
T. LETAVIC<sup>1</sup>, J. PETRUZZELLO<sup>1</sup>, J. CLAES<sup>2</sup>, P. EGGENKAMP<sup>2</sup>, E. JANSSEN<sup>2</sup>, A. VAN DER WAL<sup>2</sup>  
<sup>1</sup> PHILIPS RESEARCH NORTH AMERICA, , NY, USA  
<sup>2</sup> PHILIPS SEMICONDUCTORS, NIJMEGEN, THE NETHERLANDS 357
- 13-2 **Development of ESD protection structures for BULK and SOI BCD6 technology**  
A. TAZZOLI, L. CERATI\*, M. DISSEGNA\*, A. ANDREINI\*, E. ZANONI, G. MENEGHESO  
UNIVERSITY OF PADOVA, DEI, PADOVA, ITALY.  
\* STMicroelectronics FTM R&D , Italy 361
- 13-3 **Self-Heating Driven Vth Shifts in Integrated VDMOS Transistors**  
P. MOENS\*, J.F. CANO\*, C. DE KEUKELEIRE\*, B. DESOETE\*, S. ARESU\*\*,\*\*\*, W. DE CEUNINCK\*\*, H. DE VLEESCHOUWER\* AND M. TACK\*.  
\*AMI Semiconductor Belgium, Oudenaarde, Belgium  
\*\*Institute for Material Research, Diepenbeek, Belgium  
\*\*\*Now with Infineon Technologies, Munich, Germany. 365
- 13-4 **1200V Interconnection Technique with Isolated Self-Shielding Structure**  
SUNG-LYONG KIM, CHANG-KI JEON, MIN-SUK KIM AND JONG-JIB KIM  
Fairchild Semiconductor, Kyonggi-Do, Korea 369

### Session 14: Applications

Chair: G. Majumdar Mitsubishi, Japan  
D. Silber University of Bremen, Germany

- 14-1 **A Digitally Controlled DC-DC Converter Module with a Segmented Output Stage for Optimized Efficiency**  
O. TRESCASES<sup>1</sup>, WAI TUNG NG<sup>1</sup>, H. NISHIO<sup>2</sup>, MASAHARU EDO<sup>2</sup> AND TETSUYA KAWASHIMA<sup>2</sup>  
<sup>1</sup>University of Toronto, Toronto, Canada  
<sup>2</sup>Fuji Electric Advanced Technology Co., Japan 373
- 14-2 **Design of a CMOS Integrated Controller for High Current Low Voltage DC-DC Converters with Variable Switching Frequency**  
XIAOMING DUAN, JINSEOK PARK, KENDYWU\*, ALEX Q. HUANG  
Semiconductor Power Electronics Center, NCSU, Raleigh, USA  
\* NIKO Semiconductor Co., Ltd. Taipei, Taiwan 377
- 14-3 **Simulation, Design and Testing of Integrated Power Supply for Insulated Gate Transistors**  
N.ROUGER, J-C CREBIER, R. MITOVA, L. AUBARD, C. SCHAEFFER  
LEG - ENSIEG, INPG, St Martin d'Hères, France 381