

International Symposium on Code Generation and Optimization

CGO 2006

26-29 March 2006 • New York, New York

Co-sponsored by

IEEE Computer Society TC-uARCH

Association for Computing Machinery SIGMICRO

Association for Computing Machinery SIGPLAN



Los Alamitos, California

Washington • Tokyo

Copyright © 2006 by The Institute of Electrical and Electronics Engineers, Inc.
All rights reserved.

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries may photocopy beyond the limits of US copyright law, for private use of patrons, those articles in this volume that carry a code at the bottom of the first page, provided that the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

Other copying, reprint, or republication requests should be addressed to: IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, P.O. Box 133, Piscataway, NJ 08855-1331.

The papers in this book comprise the proceedings of the meeting mentioned on the cover and title page. They reflect the authors' opinions and, in the interests of timely dissemination, are published as presented and without change. Their inclusion in this publication does not necessarily constitute endorsement by the editors, the IEEE Computer Society, or the Institute of Electrical and Electronics Engineers, Inc.

IEEE Computer Society Order Number P2499
ACM Order Number 520063
ISBN-13: 978-0-7695-2499-3
ISBN-10: 0-7695-2499-0
Library of Congress Number 2005935652

Additional copies may be ordered from:

ACM Order Department
P.O. Box 11405
New York, NY 10286-1405
Tel: + 1-800-342-6626
(U.S. and Canada)
Tel: +1-212-626-0500
(all other countries)
Fax: + 1-212-944-1318
E-mail: acmhelp@acm.org

IEEE Computer Society
Customer Service Center
10662 Los Vaqueros Circle
P.O. Box 3014
Los Alamitos, CA 90720-1314
Tel: + 1 800 272 6657
Fax: + 1 714 821 4641
<http://computer.org/cspress>
csbooks@computer.org

IEEE Service Center
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
Tel: + 1 732 981 0060
Fax: + 1 732 981 9667
[http://shop.ieee.org/store/
customer-service@ieee.org](http://shop.ieee.org/store/customer-service@ieee.org)

IEEE Computer Society
Asia/Pacific Office
Watanabe Bldg., 1-4-2
Minami-Aoyama
Minato-ku, Tokyo 107-0062
JAPAN
Tel: + 81 3 3408 3118
Fax: + 81 3 3408 3553
tokyo.ofc@computer.org

Individual paper REPRINTS may be ordered at: reprints@computer.org

Editorial production by Stephanie Kawada

Cover art production by Joe Daigle/Studio Productions

Printed in the United States of America by Applied Digital Imaging



IEEE Computer Society
Conference Publishing Services
<http://www.computer.org/proceedings/>

Proceedings

CGO 2006

Table of Contents

Message from the General Co-Chairs	x
Message from the Program Chair	xi
Committees	xii
Reviewers	xiv
Corporate Sponsors	xv

Workshops

Workshop on Software Tools for Multi-core Systems

Organizer: Mary Hall (USC/ISI)

Workshop on Optimizations for DSP and Embedded Systems

Organizers: Deepu Talla (Texas Instruments) and Lizy John (University of Texas at Austin)

Workshop on EPIC Architectures and Compiler Technology

Organizers: Kalyan Muthukumar (Intel) and Rick Hank (Hewlett-Packard)

Tutorials

Phoenix: A Framework for Code Generation and Program Analysis

Presenters: Andy Ayers and Mark Lewin (Microsoft)

Compiler Mediated Performance of a Cell Processor

Presenters: Kathryn O'Brien, Alexandre Eichenberger, Kevin O'Brien, and Michael Gschwind (IBM)

Dynamic Compilation at the System Level

Presenters: Michael Gschwind and Erik Altman (IBM)

Keynotes

Wei Li, Sr., Principal Engineer, Intel Corporation

Guy Steele, Fellow, Sun Microsystems

Kevin Stoodley, Fellow and CTO of Compilation Technology, IBM

Session 1: Dynamic Optimization

A Cross-Architectural Interface for Code Cache Manipulation	17
<i>Kim Hazelwood (University of Virginia) and Robert Cohn (Intel Corporation)</i>	
Thread-Shared Software Code Caches	28
<i>Derek Bruening, Vladimir Kiriansky, Timothy Garnett, and Sanjeev Banerji (Determina, Inc.)</i>	
Tailoring Graph-Coloring Register Allocation for Runtime Compilation.....	39
<i>Keith D. Cooper and Anshuman Dasgupta (Rice University)</i>	
A Self-Repairing Prefetcher in an Event-Driven Dynamic Optimization Framework.....	50
<i>Weifeng Zhang, Brad Calder, and Dean M. Tullsen (University of California, San Diego)</i>	

Session 2: Object-Oriented Code Generation and Optimization

Java JNI Bridge: A Framework for Mixed Native ISA Execution	65
<i>Miaobo Chen, Shalom Goldenberg, Suresh Srinivas, Valery Ushakov, Young Wang, Qi Zhang, Eric Lin, and Yoav Zach (Intel Corporation)</i>	

Space-Efficient 64-bit Java Objects through Selective Typed Virtual Addressing	76
<i>Kris Venstermans, Lieven Eeckhout, and Koen De Bosschere (Ghent University)</i>	
Experiences with Multi-threading and Dynamic Class Loading in a Java Just-In-Time Compiler	87
<i>Vijay Sundaresan, Daryl Maier, Pramod Ramarao, and Mark Stoodley (IBM Canada Ltd.)</i>	
Dynamic Class Hierarchy Mutation	98
<i>Lixin Su and Mikko H. Lipasti (University of Wisconsin-Madison)</i>	

Session 3: Phase Detection and Profiling

Online Phase Detection Algorithms	111
<i>Priya Nagpurkar (University of California, Santa Barbara), Michael Hind (IBM T. J. Watson Research Center), Chandra Krintz (University of California, Santa Barbara), Peter F. Sweeney, and V. T. Rajan (IBM T. J. Watson Research Center)</i>	
Region Monitoring for Local Phase Detection in Dynamic Optimization Systems	124
<i>Abhinav Das, Jiwei Lu, and Wei-Chung Hsu (University of Minnesota)</i>	
Selecting Software Phase Markers with Code Structure Analysis.....	135
<i>Jeremy Lau, Erez Perelman, and Brad Calder (University of California, San Diego)</i>	
Profiling over Adaptive Ranges.....	147
<i>Shashidhar Mysore, Banit Agrawal, Timothy Sherwood, Nisheeth Shrivastava, and Subhash Suri (University of California, Santa Barbara)</i>	
2D-Profiling: Detecting Input-Dependent Branches with a Single Input Data Set.....	159
<i>Hyesoon Kim, M. Aater Suleman, Onur Mutlu, and Yale N. Patt (University of Texas at Austin)</i>	

Session 4: Tiled and Multicore Compilation

Constructing Virtual Architectures on a Tiled Processor	173
<i>David Wentzlaff and Anant Agarwal (Massachusetts Institute of Technology)</i>	
Compiling for EDGE Architectures	185
<i>Aaron Smith (University of Texas at Austin), Jim Burrill (University of Massachusetts, Amherst), Jon Gibson, Bertrand Maher, Nick Nethercote, Bill Yoder, Doug Burger, and Kathryn S. McKinley (University of Texas at Austin)</i>	
Data and Computation Transformations for Brook Streaming Applications on Multiprocessors	196
<i>Shih-wei Liao, Zhaohui Du, Gansha Wu, and Guei-Yuan Lueh (Intel Corporation)</i>	
Compiler-Directed Data Partitioning for Multicore Processors.....	208
<i>Michael L. Chu and Scott A. Mahlke (University of Michigan)</i>	

Session 5: Static Code Generation and Optimization Issues DSA

Inline Analysis: Beyond Selection Heuristics.....	221
<i>Dhruva R. Chakrabarti and Shin-Ming Liu (Hewlett-Packard Company)</i>	
Practical Structure Layout Optimization and Advice	233
<i>Robert Hundt, Sandya Mannarswamy, and Dhruva Chakrabarti (Hewlett-Packard Company)</i>	
Post Register Allocation Spill Code Optimization	245
<i>Christopher Lupo and Kent D. Wilken (University of California, Davis)</i>	
A Compiler-Guided Approach for Reducing Disk Power Consumption by Exploiting Disk Access Locality	256
<i>Seung Woo Son, Guangyu Chen, and Mahmut Kandemir (Pennsylvania State University)</i>	

Session 6: SIMD Compilation

Optimizing Dynamic Binary Translation for SIMD Instructions	269
<i>Jianhui Li, Qi Zhang, Shu Xu, and Bo Huang (Intel China Software Center)</i>	
Multi-platform Auto-vectorization	281
<i>Dorit Nuzman (IBM Haifa Research Lab) and Richard Henderson (Red Hat)</i>	

Session 7: Optimization Space Exploration

Using Machine Learning to Focus Iterative Optimization.....	295
<i>F. Agakov, E. Bonilla, J. Cavazos, B. Franke, G. Fursin, M. F. P. O'Boyle, J. Thomson, M. Toussaint, and C. K. I. Williams (University of Edinburgh)</i>	
Exhaustive Optimization Phase Order Space Exploration.....	306
<i>Prasad A. Kulkarni, David B. Whalley, Gary S. Tyson (Florida State University), and Jack W. Davidson (University of Virginia)</i>	
Fast and Effective Orchestration of Compiler Optimizations for Automatic Performance Tuning	319
<i>Zhelong Pan and Rudolf Eigenmann (Purdue University)</i>	

Session 8: Security and Reliability

Software-Based Transparent and Comprehensive Control-Flow Error Detection.....	333
<i>Edson Borin (IC-UNICAMP), Cheng Wang, Youfeng Wu (PSL-Intel Corporation), and Guido Araujo (IC-UNICAMP)</i>	
Compiler Optimizations to Reduce Security Overhead.....	346
<i>Tao Zhang, Xiaotong Zhuang, and Santosh Pande (Georgia Institute of Technology)</i>	

BIRD: Binary Interpretation Using Runtime Disassembly.....358
Susanta Nanda, Wei Li, Lap-Chung Lam, and Tzi-cker Chiueh
(SUNY at Stony Brook)

Author Index371