

2007 International Symposium on VLSI Design, Automation, and Test

**Hsinchu, Taiwan
25-27 April 2007**



IEEE Catalog Number: 07TH8910
ISBN: 1-4244-0582-3

Table of Contents

Novel Configurable Architecture of ML-Decomposed Binary Arithmetic Encoder for Multimedia Applications.....	1
<i>Yu-Jen Chen, Chen-Han Tsai, Liang-Gee Chen</i>	
A Hardwired Context-Based Adaptive Binary Arithmetic Encoder for H.264 Advanced Video Coding	5
<i>Po-Sheng Liu, Jian-Wen Chen, Youn-Long Lin</i>	
A Joint Architecture of Error-Concealed Deblocking Filter for H.264/AVC Video Transmission.....	9
<i>Wen-Ping Lee, Tsu-Ming Liu, Chen-Yi Lee</i>	
A 2.4-GHz 18-mW Two-Point Delta-Sigma Modulation Transmitter for IEEE 802.15.4.....	13
<i>Ching-Lung Ti, Tsung-Hsien Lin</i>	
A Digital Envelope Modulator for an OFDM WLAN Polar Transmitter in 90 nm CMOS.....	17
<i>P.T.M. van Zeijl, M. Collados</i>	
On-Chip Transmission Line Modeling and Applications to Millimeter-Wave Circuit Design in 0.13um CMOS Technology.....	21
<i>Chun-Lin Ko, Chien-Nan Kuo, Ying-Zong Juang</i>	
Two-Stage Scattered Pilot Synchronization with Channel Estimation Scattered Pilots Pre-Filling for DVB-T/H	25
<i>Wei-Chang Liu, Ting-Chen Wei, Shyh-Jye Jou</i>	
Low Power and Power Aware Design for DVB-T/H Baseband Inner Receiver.....	29
<i>Chi-Yao Tseng, Ting-Chen Wei, Wei-Chang Liu, Shyh-Jye Jou</i>	
Multilevel LINC System Design for Wireless Transmitters.....	33
<i>Yuan-Jyue Chen, Kai-Yuan Jheng, An-Yeu (Andy) Wu, Hen-Wai Tsao, Bosen Tzeng</i>	
A 4-54GHz Static Frequency Divider with Back-Gate Coupling	37
<i>Jung-Yu Chang, Shen-Iuan Liu</i>	
A Lc-Tank Injection Locked Frequency Dividerwith Complementary Structure.....	41
<i>Shao-Hua Lee, Sheng-Lyang Jang, Jian-Feng Lee, Yun-Hsueh Chung, Huang-Mei Chen</i>	
Low Phase Noise Differential Cmos Vco Based On Tapped-Inductor Resonator	45
<i>Yun-Hsueh Chuang, Sheng-Lyang Jang, Chien-Feng Lee, Shao-Hua Lee, Cheng-Bing Liu</i>	
Microprocessor Modeling and Simulation with SystemC.....	49
<i>Yen-Ju Lu, Chen-Tung Lin, Chi-Feng Wu, Shih-Arn Hwang, Ying-Hsi Lin</i>	
A Memory-Efficient Progressive JPEG Decoder	53
<i>Kun-Bin Lee, Chi-Cheng Ju</i>	
An LLC-OCV Methodology for Statistic Timing Analysis	57
<i>Jerry Hong, Kevin Huang, Peter Pong, JD Pan, Jason Kang, KC Wu</i>	
A Matching-based Placement and Routing System for Analog Design	61
<i>Po-Hung Lin, Ho-Che Yu, Tian-Hau Tsai, Shyh-Chang Lin</i>	
Test Power IR Drop Closure Flow for NetComposer-I Platform Design	65
<i>Augusli Kifli, W.J. Chen, Y.W. Chen, KC Wu</i>	
Efficient Memory-Based FFT Architectures for Digital Video Broadcasting (DVB-T/H).....	69
<i>Chin-Long Wey, Wei-Chien Tang, Shin-Yo Lin</i>	
Power Gating Technique for Embedded Pseudo SRAM.....	73
<i>Ching-Yun Cheng, Ming-Hung Chang, Wei Hwang</i>	
Efficient Calculation of Timed Cumulative Probability Density Function.....	77
<i>Yu-Shih Su, Yi-Hsin Weng, Shih-Chieh Chang</i>	
Input Selection Encoding for Low Power Multiplexer Tree	81
<i>Hsiao-En Chang, Juinn-Dar Huang, Chia-I Chen</i>	

Table of Contents

Automation of Synchronous Bias Transmission Line Pulsing System.....	85
<i>Bor-Wei Chang, Hsin-Chyh Hsu, Ming-Dou Ker</i>	
An Efficient Design-for-Testability Scheme for Motion Estimation in H.264/AVC	89
<i>Tung-Hsing Wu, Yi-Lin Tsai, Soon-Jyh Chang</i>	
Characterization of Supply and Substrate Noises in CMOS Digital Circuits	93
<i>Hsien-Hung Wu, Chin-Hsin Fu, Yaw-Feng Wang, Pei-Wen Luo, Yen-Ming Chen, Liang-Chia Cheng, Cheng-Hsing Chien</i>	
Hardware Architecture Design of CABAC Codec for H.264/AV.....	97
<i>Lingfeng Li, Yang Song, Takeshi Ikenaga, Satoshi Goto</i>	
Design and Implementation of Reconfigurable RSA Cryptosystem	101
<i>Yun-Lu Chen, Chih-Yeh Tseng, Hsie-Chia Chang</i>	
On-Chip VDC Circuit for SRAM Power Management.....	105
<i>C.F. Lee, Wesley Lin, F.S. Lai, S.C. Lin</i>	
Switch Controlled Source Amplifier for Low Power Mobile TFT-LCD Driver IC.....	109
<i>J. H. Woo, J. G. Lee, K. Y. Chung, W. S. Kang, S. C. Kim, G. S. Lee, I. S. Kang, B. N. Kim</i>	
The novel Chinese abacus adder	111
<i>Zi-Yi Zhao, Chien-Hung Lin, Yu-Zhi Xie, Yen-Ju Chen, Yi-Jie Lin, Shu-Chung Yi</i>	
Theoretical Analysis and Implementation of a Variable Gain Even Harmonic Mixer	115
<i>Jian-Yu Hsieh, Shuenn-Yuh Lee</i>	
Fast-Lock Dual Charge Pump Analog DLL using Improved Phase Frequency Detector	119
<i>Soh Lip-Kai, Mohd-Shahiman Sulaiman, Zubaida Yusoff</i>	
A Realization of Low Noise Silicon Acoustic Transducer Interface Circuit.....	124
<i>Yu-Chun Hsu, Wen-Chieh Chou, Lu-Po Liao, Ji-Ching Tsai</i>	
Challenges for Low-power Embedded SOC's	128
<i>Toshihiro Hattori</i>	
Mixed Hardware Software Multilevel Modeling and Simulation for Multithreaded Heterogeneous MPSoC	132
<i>Katalin Popovici, Xavier Guerin, Lisane Brisolara, Ahmed Jerraya</i>	
Low-Power Instruction Cache Architecture Using Pre-Tag Checking.....	136
<i>Shi-You Cheng, Juinn-Dar Huang</i>	
Low Cost Testing of Quadruple Band GSM RFCMOS SOC	140
<i>Bobby Lai, Chris Rivera, Khurram Waheed</i>	
Testing Crosstalk Faults of Data and Address Buses in Embedded RAMs.....	144
<i>Jiunn-Der Yu, Jin-Fu Li, Tsu-Wei Tseng</i>	
A Power-Saved 1Gbps Irregular LDPC Decoder based on Simplified Min-Sum Algorithm	148
<i>Qi Wang, Kazunori Shimizu, Takeshi Ikenaga, Satoshi Goto</i>	
A low-Power Viterbi Decoder Based On Scarce State Transition And Variable Truncation Length.....	152
<i>Dah-Jia Lin, Chien-Ching Lin, Chih-Lung Chen, Hsie-Chia Chang, Chen-Yi Lee</i>	
Generalized MLP/BP-based MIMO DFEs for Overcoming ISI and ACI in Band-limited Channels.....	156
<i>Terng-Ren Hsu, Chi-Shi Chen, Terng-Yin Hsu, Chen-Yi Lee</i>	
A Dynamic Phase-Frequency Recovery for Power Reduction in OFDM Systems.....	160
<i>Mei-Hui Yang, Jui-Yuan Yu, Juinn-Ting Chen, Chen-Yi Lee</i>	
Challenges and Solutions in Modern VLSI Placement.....	164
<i>Zhe-Wei Jiang, Hsin-Chen Chen, Tung-Chieh Chen, Yao-Wen Chang</i>	
Microarchitecture-Aware Floorplanning for Processor Performance Optimization	169
<i>Chi-Ying Chen, Juinn-Dar Huang, Hung-Ming Chen</i>	

Table of Contents

Interleaving of Gate Sizing and Constructive Placement for Predictable Performance	173
<i>Sungjae Kim, Eugene Shragowitz, George Karypis, Rung-Bin Lin</i>	
-Geometry clock tree construction with wirelength and via minimization.....	177
<i>Chun-Hao Wang, Wai-Kei Mak</i>	
A Low-Complexity Fractional Delay All-Pass Filter Design for Time-Domain Interpolation.....	181
<i>To-Ping Wang, Tzi-Dar Chiueh</i>	
JQRPSD Detection with Low Complexity for SDM MIMO Wireless Communication System	185
<i>Hsin-Lei Lin, Hung-Lien Chen, Robert C. Chang</i>	
Synchronous Sampling and SNR-Based Gain Control in DS/CDMA Systems	189
<i>You-Hsien Lin, Shih-Lin Lo, Wei-Chi Lai, Ta-Yang Juan, Terng-Yin Hsu</i>	
A1V5-BIT 5Gsample/SEC CMOS ADC FORUWB Receivers.....	193
<i>I-Hsin Wang, Shen-Iuan Liu</i>	
A4-BIT, 13.5Gsample/SEC Track-And-Hold Circuit.....	197
<i>I-Hsin Wang, Shen-Iuan Liu</i>	
A 1V 10-Bit 400MS/s Current-Steering D/A Converter in 90-nm CMOS	201
<i>Chueh-Hao Yu, Wen-Hui Chen, Day-Uei Li, Wan-Ju Huang</i>	
Post-Silicon Design Methodology on Chip Power Characterization, Validation, and Debug Applied on High Performance Per Watt Microprocessor.....	205
<i>Yuan-Chuan Steven Chen, Daniel Lu, Gang Yuan</i>	
Toward Automatic Synthesis of SOC Test Platforms	209
<i>Wen-Cheng Huang, Chin-Yao Chang, Kuen-Jong Lee</i>	
Stable Performance MAC Protocol for HOY Wireless Tester under Large Population	213
<i>Te-Wen Ko, Yu-Tsao Hsing, Cheng-Wen Wu, Chih-Tsun Huang</i>	
A30phase 500MHZ PLL For 3X Over-Sampling Clock Data Recovery.....	217
<i>Kuo-Hsing Cheng, Chao-An Chen, Wei-Bin Yang, Feng-Hsin Cho</i>	
A Self-Calibrated Multiphase DLL-Based Clock Generator	221
<i>Hsin-Shu Chen, Chao-Ching Hung</i>	
4-Mb SPI Flash Compatible Phase-Change Memory.....	225
<i>Shyh-Shyuan Sheu, Lieh-Chiu Lin, Wen-Han Wang, Pei-Chia Chiang, Keng-Li Su, Ming-Jer Kao, Ming-Jinn Tsai</i>	
A Low-Power Low-Swing Single-Ended Multi-Port SRAM.....	229
<i>Hao-I Yang, Ming-Hung Chang, Ssu-Yun Lai, Hsiang-Fei Wang, Wei Hwang</i>	
A 256x128 Energy-Efficient TCAM with Novel Low Power Schemes	233
<i>Po-Tsang Huang, Shu-Wei Chang, Wen-Yen Liu, Wei Hwang</i>	
Design on Mixed-Voltage I/O Buffers with Consideration of Hot-Carrier Reliability	237
<i>Ming-Dou Ker, Fang-Ling Hu</i>	
Minimizing Energy Consumption with Variable Forward Body Bias for Ultra-Low Energy LSIs.....	241
<i>SenthilKumar Jayapal, Yiannos Manoli</i>	
Maximizing Full-Chip Simulation Signal Visibility for Efficient Debug	245
<i>Yu-Chin Hsu</i>	
Reducing Transaction-Level Modeling Effort while Retaining Low Communication Overhead for HW/SW Co-Emulation System.....	250
<i>Young-II Kim, Moo-Kyoung Chung, Ando Ki, Chong-Min Kyung</i>	
Designing Globally Optimal Delta-Sigma Modulator Topologies via Signomial Programming	254
<i>Hing-Kit Kwan, Yuen-Hong Alvin Ho, Ngai Wong, Ka-Leung Ho</i>	

Table of Contents

On-Chip Bus Encoding For Power Minimization Under Delay Constraint	258
<i>Tzu-Wei Lin, Shang-Wei Tu, Jing-Yang Jou</i>	
A 4-Channel Poly-Phase Filter for Cognitive Radio Systems	262
<i>Guan-Jun Chen, Hsien-Hsiang Chiu, Tai-Cheng Lee</i>	
Analysis and Design of a 1V Charge Sampling Readout Amplifier in 90nm CMOS for Medical Imaging.....	266
<i>Linga Reddy Cenkeramaddi, Trond Ytterdal</i>	
A 6Gbps Serial Link Transmitter with Pre-emphasis	270
<i>Chang-Min Chu, Chih-Hua Chuang, Chi-Hsien Lin, Shyh-Jye Jou</i>	
Native-Mode Self Test for Embedded Systems on a Chip.....	272
<i>Jacob A. Abraham</i>	
Nanoelectronics: challenges and opportunities	273
<i>Giovanni De Micheli</i>	
Challenges of Digital Consumer and Mobile SoC's: More Moore Possible?.....	274
<i>Tohru Furuyama</i>	