

2007 IEEE International Interconnect Technology Conference

**Burlingame, CA
3-6 June 2007**



**IEEE Catalog Number:
ISBN:**

**07TH8946
1-4244-1069-X**

Table of Contents

Materials and Processes for High Signal Propagation Performance and Reliable 32 Nm Node BEOL	1
<i>V. Arnal, A. Farcy, M. Aimadeddine, V. Jousseau, L.G. Gosset, J. Guillan, M. Assous, L. Favennec, A. Zenasni, T. David, K. Hamioud, L-L. Chapelon, N. Jourdan, T. Vanypre, T. Mourier, P. Chausse and S. Maitrejea</i>	
Highly-Oriented PVD Ruthenium Liner for Low-Resistance Direct-Plated Cu Interconnects	4
<i>M. Abe, M. Ueki, M. Tada, T. Onodera, N. Furutake, K. Shimura, S. Saito and Y. Hayashi</i>	
Self-Formed Barrier Technology Using Cumn Alloy Seed for Copper Dual-Damascene Interconnect with Porous-Sioc/ Porous-Par Hybrid Dielectric	7
<i>T.Watanabe, H. Nasu, T. Usui, G. Minamihaba, N.Kurashima,A.Gawase, M.Shimada, Y.Yoshimizu, Y. Uozumi and H. Shibata</i>	
The Influence of the Size Effect of Copper Interconnects on RC Delay Variability Beyond 45nm Technology	10
<i>H. Kitada, T. Suzuki, T. Kimura, H. Kudo, H. Ochimizu, S. Okano, A. Tsukune, S. Suda, S. Sakai, N. Ohtsuka, T. Tabira, T. Shirasu, M. Sakamoto, A. Matsuura, Y. Asada, and T. Nakamura</i>	
Chip-Package-Interaction Modeling of Ultra Low-K/Copper Back End of Line.....	13
<i>X. H. Liu, T. M. Shaw., M. W. Lane, E. G. Liniger, B. W. Herbst and D. L. Questad</i>	
A Comparative Study of Thermal and Plasma Enhanced ALD Ta-N-C Films on Sio2, Sicoh and Cu Substrates	16
<i>H.Wojcik, M.Friedemann, F.Feustel, M.Albert, S.Ohsiek, J.Metzger, J.Voss, J.W.Bartha and C.Wenzel</i>	
Integration and Interconnect Reliability of Warm A1 Process with CVD-A1 Seed Layer Deposited Using a Novel Precursor of TMAAE3 (Trimethylarninealane Borane).....	19
<i>Choon-Hwan Kim, Sung-Won Lim, Hyun-Phil Kim, In-Cheol Ryu, Byung-Soo Eun, Soo-Hyun Kim,Il-Cheol Rho, Yong-Sun Sohn, Hyo-Sang Kang and Hyeong-Joon Kim</i>	
The Development of an Innovative Process of Large Grained and Low Resistivity Cu Wires for Less Than Hp 45nm ULSI	22
<i>Suguru TASHIRO, Khyoupin KHOO, Takahiro NAGANO, Jin ONUKI, Yasunori CHONAN1, Haruo AKAHOSHI2, Toshimi TOBITA3, Masahiro CHIBA3, Kensuke ISHIKAWA4 and Nobuhiro ISHIKAWA5</i>	
Cu Resistivity Scaling Limits for 20nm Copper Damascene Lines.....	25
<i>J. Van Olmen, S. List, Zs. Tökei, L. Carbonell, S. H. Brongersma, H. Volders, E. Kunnen, N. Heylen, I. Ciofi, A. Khandelwal, J. Gelatos T. Mandrekar and P. Boelen</i>	

Cu / Barrier Metal Stack Film Characterization for Reliability Estimation	28
<i>Shinichi Ogawa, Toshiyuki Ohdaira, Nobuki Hosoi, Nobuaki Tarumi, Ryoichi Suzuki, and Shuichi Saito</i>	
Reliability of CU Interconnects with TA Implant	31
<i>J. Gambino, T. D. Sullivan, F. Chen, J. Gill, S. Mongeon, E. Adams, J. Burnham and K. Rodbell</i>	
Development of an Eco-Friendly Copper Interconnect Cleaning Process	34
<i>Yoshihiro Uozumi, Takahito Nakajima, Tsuyoshi Matsumura, Yasuhito Yoshimizu and Hiroshi Tomita</i>	
Design for Manufacturability in Backend Reliability and Packaging of Nanoscale Technologies	37
<i>Y.K. Lim, J.B. Tan, K.L. Pey, E.C. Chua, Y.H. Yeo, Thomas Fu and L.C. Hsia</i>	
Electromigration Failure Mechanism and Lifetime Expectation for Bi-Modal Distribution in Cu/Low-K Interconnect	40
<i>Young Jin Wee, Andrew T. Kim, Jung Eun Lee, Jae Yeol Maeng, Woon Hyuk Choi, Seewoo Nam, Seungjin Lee, Kyoung Woo Lee, Jaehak Kim, Keeyoung Jun, Seung Man Choi, Jaeouk Choo, Jungshik Heo, Hong Jae Shin and Nae in Lee</i>	
Air-Gap Transmission Lines for Multiprocessor Interconnects on FR-4 and BT Substrates	43
<i>Todd J. Spencer and Paul A. Kohl</i>	
Formation of Ni(Pt) Germanosilicide Using a Sacrificial Si Cap Layer	46
<i>Yi-Wei Chen, Yu-Lan Chang, Yi-Cheng Chen, Kevin Shieh, Climbing Huang and S. F. Tzou</i>	
The Impact of Size Effects and Copper Interconnect Process Variations on the Maximum Critical Path Delay of Single and Multi-Core Microprocessors	49
<i>Gerald Lopez, Raghunath Murali, Reza Sarvari, Keith Bowman, Jeffrey Davis and James Meindl</i>	
Advanced Cu/Low-K BEOL Integration, Reliability, and Extendibility	52
<i>Daniel C. Edelstein</i>	
Multi-Level Cu Interconnects Integration and Characterization with Air Gap As Ultra-Low K Material Formed Using a Hybrid Sacrificial Oxide / Polymer Stack	53
<i>L.G. Gosset, F. Gaillard, D. Bouchu, R. Gras, J. de Pontcharra, S. Orain, O. Cueto, Ph. Lyan, O. Louveau, G. Passemard and J. Torres</i>	
Multi-Level Air Gap Integration for 32/22nm Nodes Using a Spin-On Thermal Degradable Polymer and a Sioc CVD Hard Mask.	56
<i>R. Daamen, P.H.L. Bancken, D. Ernur Badaroglu, J. Michelin, V.H. Nguyen, G.J.A.M. Verheijden, A. Humbert, J. Waeterloos, A. Yang, J.K. Cheng, L.Chen, T. Martens and R.J.O.M. Hoofman</i>	

A Highly Reliable Cu Interconnect Technology for Memory Device	59
<i>H.B. Lee, J.W. Hong, G.J. Seong, J.M. Lee, H. Park, J.M. Baek, K.I. Choi, B.L. Park, J.Y. Bae, G.H. Choi, S.T. Kim, U.I. Chung, J.T. Moon, J.H. Oh, J.H. Son, J.H. Jung, S. Hah and S.Y. Lee</i>	
Integration of High Performance and Low Cost Cu/Ultra Low-K Sioc(K=2.0) Interconnects with Self-Formed Barrier Technology for 32nm-Node and Beyond	62
<i>Y. Ohoka, Y. Ohba, A. Isobayashi, T. Hayashi, N. Komai, S. Arakawa, R. Kanamura and S. Kadomura</i>	
Full Copper Electrochemical Mechanical Planarization (Ecmp) As a Technology Enabler for the 45 and 32nm Nodes	65
<i>M. Mellier, T. Berger, R. Duru, M. Zaleski, M. C. Luche, M. Rivoire, C. Goldberg, G. Wyborn, K-L. Chang, Y. Wang, V. Ripoché, S. Tsai, M. Thothadri, W-Y. Hsu and L. Chen</i>	
Toward a Real System Integration; a Direction of IC Technology	68
<i>Akira Matsuzawa</i>	
CMOS Integration of Capacitive, Optical, and Electrical Interconnects	71
<i>Jon Lexau, Xuezhe Zheng, Jon Bergey, Ashok V. Krishnamoorthy, Ron Ho, Robert Drost and Jack Cunningham</i>	
Three Dimensional Chip Stacking Using a Wafer-To-Wafer Integration	74
<i>Ritwik Chatterjee, Murielle Fayolle, Patrick Leduch, Scott Pozdera, Bob Jones, Eddie Acosta, Barbara Charlet, Thierry Enot, Michel Heitzmann, Marc Zussyb, Antonio Romanb, Olivier Louveauc; Sylvain, Maitrejeanb, Didier Louisb, Nelly Kernevezb, Nicol</i>	
Technology and Design Cooperation: High-K MIM Capacitors for Microprocessor, IO, and Clocking	77
<i>Héctor Sánchez, Om P. Mandhana, Bill Johnstone, Doug Roberts, Joshua Siegel, Brad Melnick, Muhsin Celik, Mike Baker, Jim Hayden, Byoung Min, John Edgerton and Bruce White</i>	
Impact of Cu Microstructure N Electromigration Reliability	83
<i>C.-K. Hu, L. Gignac, B. Baker, E. Liniger and R. Yu</i>	
A Study of Adhesion and Improvement of Adhesion Energy Using Hybrid Low-K (Porous-Par / Porous-Sioc(K=2.3/2.3)) Structures with Multi-Layered Cu Interconnects for 45-Nm Node Devices	86
<i>þT.Usami, C.Maruyama, M.Tagami, K.Watanabe, T.Kameshima, H.Masuda, M.Shimada, A.Gawase, Y.Kagawa3, N.Nakamura, H.Miyajima, H.Naruse, Y.Enomoto, T.Kitano and M.Sekine</i>	
Chemical and Plasma Oxidation Behaviors of Nisi and Niptsi Salicide Films in 65nm Node CMOS Process	89
<i>Yu-Lan Chang, Yi-Wei Chen, Yi-Cheng Chen, Kevin Shieh, Climbing Huang, and S F Tzou</i>	
An Alternative Low Resistance MOL Technology with Electroplated Rhodium As Contact Plugs for 32nm CMOS and Beyond	92
<i>I. Shao, J.M. Cotte, B. Haran, A.W. Topol, E.E. Simonyi, C. Cabral, Jr. and H. Deligianni</i>	

Optimizing ALD WN Process for 65nm Node CMOS Contact Application	95
<i>Y.-C. Chen, T.-Y. Hung, Y.-L. Chang, K. Shieh, C.-L. Hsu, C. Huang, WH Yan, K. Ashtiani, D. Pisharoty, W. Lei, S. Chang, F. Huang, J. Collins and S. F. Tzou</i>	
Mechanism and Application of Negative Charging Mode of Electron Beam Inspection for PMOS Leakage Detection	98
<i>Li-Lung Lai, Keren Xu, Daniel Deng and Jay Ning</i>	
Assessing the Effect of Die Sealing in Cu/Low-K Structures	101
<i>Andrew V. Kearney, Anand V. Vairagar, Holm Geisler, Ehrenfried Zschech and Reinhold H. Dauskardt</i>	
Extremely Low Keff (1.9) Cu Interconnects with Air Gap Formed Using Sioc	104
<i>T. Harada, A. Ueki, K. Tomita, K. Hashimoto, J. Shibata, H. Okamura, K. Yoshikawa, T. Iseki, M. Higashi, S. Maejima, K. Nomura, K. Goto, T. Shono, S. Muranaka, N. Torazawa, S. Hirao, M. Matsumoto, T. Sasaki, S. Matsumoto, S. Ogawa, M. Fujisawa, A. Ishii,</i>	
Capacitance Reduction Effect Using Capping-Layer Removal Process for Porous Low-K (K=2.5)/Cu System Toward 45nm Technology Node	107
<i>N. Ohashi, E. Soda, T. Suzuki, S. Kondo, N. Oda, S. Ogawa and S. Saito</i>	
Mechanistic Study of Plasma Damage and CH₄ Recovery of Low K Dielectric Surface	110
<i>J. J. Bao, H. L. Shi, J. J. Liu, H. Huang, P.S. Ho, M. D. Goodner, M. Moinpour and G. M. Kloster</i>	
BEOL Process Integrations with Cu/FSG Wiring At 90 Nm Design-Rule DDR DRAM and Their Effects on Yield, Refresh Time, and Wafer-Level Reliability	113
<i>Nohjung Kwak, Sang-Tae Ahn, Hyung-Soon Park, Seo-Min Kim, Jin-Ki Jung, Gyu-Hyun Kim, Geun-Young Choi, Dong-Chul Koo, Tae-Oh Jung, Ja-Chun Ku, Jae-Kwan Jung, Jinwoong Kim and Sungwook Park</i>	
Experimental Determination of the Toughness of Crack Stop Structures	116
<i>T. M. Shaw, E. Liniger, G. Bonilla, J. P. Doyle, B. Herbst, X. H. Liu and M. W. Lane</i>	
Scaling of a Low Capacitance Highly Selective Self Aligned Contact Process	119
<i>W. Graf, O. Genz, D. Köhler, H. Prenz, K. Schupke, A. Laessig, L. Bartholomaeus, S. Finsterbusch and L. Heineck</i>	
A Comparison of Voltage Ramp and Time Dependent Dielectric Breakdown Tests for Evaluation of 45nm Low-K Sicoh Reliability	122
<i>F. Chen, P. McLaughlin, J. Gambino and J. Gill</i>	
The Impact of Multi-Core Architectures on Design of Chip-Level Interconnect Networks	125
<i>Deepak C Sekar and James D Meindl</i>	
Balancing Resistance and Capacitance of Signal Interconnects for Power Saving	128
<i>V. Nguyen Hoang, G. Doornbos, J. Michelon, A. Kumar, A. Nackaerts and P. Christie</i>	

Stress and Slurry Chemistry Effects on CMP Damage of Ultra-Low-K Dielectrics	131
<i>Taek-Soo Kim, Qiping Zhong, Maria Peterson, Halbert Tam, Tomohisa Konno, and Reinhold H. Dauskardt</i>	
Performance Predictions of Prospective Air Gap Architectures for the 22 Nm Node	134
<i>M. Gallitre, L.G. Gosset, A. Farcy, B. Blampey, R. Gras , C. Bermond, B. Fléchet and J. Torres</i>	
The Delay, Energy, and Bandwidth Comparisons Between Copper, Carbon Nanotube, and Optical Interconnects for Local and Global Wiring Application.....	137
<i>Hoyeol Cho, Kyung-Hoae Koo, Pawan Kapur and Krishna C. Saraswat</i>	
Line Edge Roughness of Metal Lines and Time-Dependent Dielectric Breakdown Characteristics of Low-K Interconnect Dielectrics	140
<i>Andrew T. Kim, Tae-Young Jeong, Miji Lee, Young Joon Moon, Se Young Lee, Boung Ju Lee and Hyungoo Jeon</i>	
Impact of Tan/Ta Copper Barrier on Full PEALD Tin/Ta₂O₅/Tin 3D Damascene MIM Capacitor Performance	143
<i>M. Thomas, A. Farcy, E. Deloffre, M. Gros-Jean, C. Perrot, D. Benoit, C. Richard, P. Caubet, S. Guillaumet¹, R. Pantel, B. Chenevier and J. Torres</i>	
Study on Effect of Via Contour Distortion on Via Micro-Void Formation in 45nm-Node Process.....	146
<i>H.Kunishima , M. Tagami , T. Shin , Y.Goto , K.Oshima, T.Nishimura, Y. Miyamori, Y.Enomoto, T.Ema, N.Yamada, K.Akiyama and N.Okada</i>	
The Critical Role of the Metal / Porous Low-K Interface in Post Direct CMP Defectivity Generation and Resulting ULK Surface and Bulk Hydrophilisation.....	149
<i>Y. Travaly, F. Sinapi, N. Heylen, A. Humbert¹, M. Delande, R. Caluwaert, J. P. de Mussy, G. Vereecke, M. R. Baklanov, F. Iacopi, J.L. Hernandez, G. Beyer and P. Fischer</i>	
Moving Away From Silicon: the Role of Interconnect in New Memory Technologies	152
<i>Dirk J. Wouters</i>	
Effect of the Hydrophilic-Lipophilic Balance (HLB) of Surfactants Included in the Post-CMP Cleaning Chemicals on Porous Sioc Direct CMP.....	155
<i>S. Kondo, M. Shiohara, K. Maruyama, K. Fukaya, K. Yamada, S. Ogawa and S. Saito</i>	
Robust Integration of an ULK Sioc Dielectric (K=2.3) for High Performance 32nm Node BEOL.....	158
<i>M. Aimadeddine , V. Jousseau, V. Arnal, L. Favennec, A. Farcy, A. Zenasni, M. Assous, M. Vilmay, S. Jullian, P. Maury, V. Delaye, N. Jourdan, T. Vanypre, P. Brun, G. Imbert, Y. LeFric, M. Mellier, H. Chaabouni, L.L. Chapelon, K. Hamioud, F. Volpi, D. L</i>	
Strategies of RC Delay Reduction in 45 NM BEOL Technology	161
<i>H. Kudo, H. Ochimizu, A. Tsukune, S. Okano, K. Naitou, M Sakamoto, S. Takesako, T. Shirasu, A. Asneil, N. IdaniK. Sugimoto, S. Ozaki, Y. Nakata, T. Owada, H. Watatani, N. Ohara, N. Ohtsuka, M. Sunayama, H. Sakai, M. Oryoji, S. Akiyama, H. Iwata, H. Yamamo</i>	

45nm-Node Interconnects with Porous Sioc-Stacks, Tolerant of Low-Cost Packaging Applications	164
<i>N. Inoue, M. Tagami, F. Itoh, H. Yamamoto, T. Takeuchi, S. Saito, N. Furutake, M. Ueki, M. Tada, T. Suzuki and Y. Hayashi</i>	
Tera-Scale Computing ... the Role of Interconnects in Volume Compute Platforms.....	167
<i>Jerry Bautista</i>	
Design and Optimization for Nanoscale Power Distribution Networks in Gigascale Systems	170
<i>Reza Sarvari, Azad Naeemi, Payman Zarkesh-Ha and James D. Meindl</i>	
A Low-Latency and High-Power-Efficient On-Chip LVDS Transmission Line Interconnect for an RC Interconnect Alternative.....	173
<i>Hiroyuki Ito, Junki Seita, Takahiro Ishii, Hideyuki Sugita, Kenichi Okada and Kazuya Masu</i>	
Chip Package Interaction for 65nm CMOS Technology with C4 Interconnections	176
<i>Mukta Farooq, Ian Melville, Christopher Muzzy, Paul V. McLaughlin, Robert Hannon, Wolfgang Sauter, Jennifer Muncy, David Questad, Charles Carey, Mary Cullinan-Scholl, Vincent McGahay, Matthew Angyal, Henry Nye, Michael Lane, Xiao Hu Liu, Thomas Shaw and Co</i>	
Densification of Carbon Nanotube Bundles for Interconnect Application	179
<i>Z. Liu, N. Bajwa, L. Ci, S.H. Lee, S. Kar, P. M. Ajayan and J.-Q. Lu</i>	
Electrical Properties of Carbon Nanotube Via Interconnects Fabricated By Novel Damascene Process	182
<i>Mizuhisa Nihei, Takashi Hyakushima, Shintaro Sato, Tatsuhiko Nozue, Masaaki Norimatsu, Miho Mishima, Tomo Murakami, Daiyu Kondo, Akio Kawabata, Mari Ohfuti and Yuji Awano</i>	
Simultaneous Cu-Cu and Compliant Dielectric Bonding for 3D Stacking of Ics	185
<i>A. Jourdain, S. Stoukatch, P. De Moor, W. Ruythooren, S. Pargfrieder, B. Swinnen and E. Beyne</i>	
Challenges for 3D IC Integration: Bonding Quality and Thermal Management.....	188
<i>Patrick Leduca, François de Crécy, Murielle Fayollea, Barbara Charleta, Thierry Enota, Marc Zussya, Bob Jonesb, Jean-Charles Barbéa, Nelly Kerneveza, Nicolas Sillona, Sylvain Maitrejeana, Didier Louisa and Gérard Passemarde</i>	
Progress of 3D Integration Technologies and 3D Interconnects	191
<i>Scott Pozder, Ritwik Chatterjee, Ankur Jain, Zhihong Huang, Robert E. Jones and Eddie Acosta</i>	