

2007 IEEE Design and Diagnostics of Electronic Circuits and Systems

**Krakow, Poland
11-13 April 2007**



IEEE Catalog Number:
ISBN 10:
ISBN 13:

CFP07DDE-PRT
1-4244-1161-0
978-1-4244-1161-0

Table of contents

Keynote Presentations

New Strategies for System-Level Design Daniel D. GAJSKI	15
Design and Test of Microfluidic Biochips Krishnendu CHAKRABARTY	17
Logic Diagnosis and Yield Learning Janusz RAJSKI	19

Session I: DfT & Defect Analysis

A Testable Random Bit Generator Based on a High Resolution Phase Noise Detection Marco BUCCI, Raimondo LUZZI	23
Test Pattern Compression Based on Pattern Overlapping Jiří JENÍČEK, Ondřej NOVÁK	29
Layout to Logic Defect Analysis for Hierarchical Test Generation Maksim JENIHIN, Jaan RAIK, Raimund UBAR, Witold A. PLESKACZ, Michał RAKOWSKI	35

Session II: SOC Design & Test

Design Platform for Quick Integration of an Internet Connectivity into System-on-Chips Bartosz WOJCIECHOWSKI, Tomasz KOWALCZYK, Wojciech SAKOWSKI	43
Resource Constrained Co-synthesis of Self-reconfigurable SOPCs Radosław CZARNECKI, Stanisław DENIZIAK	49
Extended Fault Detection Techniques for Systems-on-Chip Paolo BERNARDI, Leticia BOLZANI, Matteo SONZA REORDA	55
A Heuristic for Concurrent SOC Test Scheduling with Compression and Sharing Anders LARSSON, Erik LARSSON, Petru ELES, Zebo PENG	61

Session III: Fault Analysis & Circuit Reliability

Memories in Scaled Technologies: A Review of Process Induced Failures, Test Methodologies, and Fault Tolerance Saibal MUKHOPADHYAY, Qikai CHEN, Kaushik ROY	69
Architecture for Highly Reliable Embedded Flash Memories Benoît GODARD, Jean-Michel DAGA, Lionel TORRES, Gilles SASSATELLI	75
Analysis of Noise Margins Due to Device Parameter Variations in Sub-100nm CMOS Technology Zhicheng LIANG, Makoto IKEDA, Kunihiro ASADA	81
Accurately Determining Bridging Defects from Layout Maria GKATZIANI, Rohit KAPUR, Qing SU, Ben MATHEW, Roberto MATTIUZZO, Laura TARANTINI, Cy HAY, Salvatore TALLUTO, Thomas W. WILLIAMS	87

Session IV: FPGA-Based Design

FPGA Implementation of Strongly Parallel Histogram Equalization Ernest JAMRO, Maciej WIELGOSZ, Kazimierz WIATR	93
Cost-Efficient Synthesis for Sequential Circuits Implemented Using Embedded Memory Blocks of FPGA's Grzegorz BOROWIK, Bogdan FALKOWSKI, Tadeusz ŁUBA	99
Instruction Memory Architecture Evaluation on Multiprocessor FPGA MPEG-4 Encoder Ari KULMALA, Erno SALMINEN, Timo D. HÄMÄLÄINEN	105

Poster Session I

A Low Noise and Low Power CMOS Image Sensor with Pixel-level Correlated Double Sampling Dongsoo KIM, Gunhee HAN	113
A PMT Interface for the Optical Module Front-end of a Neutrino Underwater Telescope Valeria SIPALA, Domenico LO PRESTI, Nunzio RANDAZZO, Luigi CAPONETTO	117
A Proposal for ASM++ Diagrams Santiago DE PABLO, Santiago CÁCERES, Jesús A. CEBRIÁN, Manuel BERROCAL	121
Lightweight Multi-threaded Network Processor Core in FPGA Piotr BUCIAK, Jakub BOTWICZ	125
Parts Obsolescence Challenges for the Electronics Industry Jim TORRESEN, Thor Arne LOVLAND	131
Simulation and Characterization of Wireless Data Acquisition RF Systems for Medical Diagnostic Application Khalil ARSHAK, Francis ADEPOJU, Essa JAFER	135
Two-level Logic Synthesis for Low Power Based on New Model of Power Dissipation Ireneusz BRZOZOWSKI, Andrzej KOS	139

A March-based Fault Location Algorithm with Partial and Full Diagnosis for All Simple Static Faults in Random Access Memories	145
Gurgen HARUTUNYAN, Valery A. VARDANIAN, Yervant ZORIAN	
Avoiding Crosstalk Influence on Interconnect Delay Fault Testing	149
Tomasz GARBOLINO, Krzysztof GUCWA, Michał KOPEĆ, Andrzej HŁAWICZKA	
Instance Generation for SAT-based ATPG	153
Daniel TILLE, Görschwin FEY, Rolf DRECHSLER	
Power Testing of an FPGA-based System Using Modelsim Code Coverage Capability	157
Khalil ARSHAK, Essa JAFER, Christian IBALA	
XSIM: An Efficient Crosstalk Simulator for Analysis and Modeling of Signal Integrity Faults in Both Defective and Defect-free Interconnects	161
Ajoy K. PALIT, Kishore K. DUGANAPALLI, Walter ANHEIER	

Session V: Memory Testing

Built in Defect Prognosis for Embedded Memories	167
Prashant DUBEY, Akhil GARG, Sravan Kumar BHASKARANI	
March CRF: an Efficient Test for Complex Read Faults in SRAM Memories	173
Luigi DILILLO, Bashir M. AL-HASHIMI	
Manifestation of Precharge Faults in High Speed DRAM Devices	179
Zaid AL-ARS, Said HAMDIOUI, Georgi GAYDADJIEV	
Analyzing Test and Repair Times for 2D Integrated Memory Built-in Test and Repair	185
Philipp ÖHLER, Sybille HELLEBRAND, Hans-Joachim WUNDERLICH	

Session VI: Logic Design

An Improved MDCT IP Core Generator with Architectural Model Simulation	193
Peter MALÍK, Marcel BALÁŽ, Tomáš PIKULA, Martin ŠIMLAŠTÍK	
A Low-Power High-Speed Hybrid CMOS Full Adder for Embedded System	199
Chiou-Kou TUNG, Yu-Cherng HUNG, Shao-Hui SHIEH, Guo-Shing HUANG	
Automatic Generation of Circuits for Approximate String Matching	203
Tomáš MARTÍNEK, Otto FUČÍK, Patrik BECK, Matej LEXA	

Poster Session II

About the Efficiency of Real Time Sequences FFT Computing	211
Costin CEPIȘCĂ, Sorin Dan GRIGORESCU, Mircea COVRIG, Horia ANDREI	
Clockless Implementation of LEON2 for Low-Power Applications	215
Martin ŠIMLAŠTÍK, Viera STOPJAKOVÁ, Libor MAJER, Peter MALÍK	

Decomposition of Logic Functions in Reed-Muller Spectral Domain Edward HRYNKIEWICZ, Stefan KOŁODZIŃSKI	219
Design of Addition and Multiplication Units for High Performance Interval Arithmetic Processor Alexandru AMĂRICĂI, Mircea VLĂDUȚIU, Lucian PRODAN, Mihai UDRESCU, Oana BONCALO	223
Establishing a New Course in Reconfigurable Logic System Design Jim TORRESEN, Jorgen NORENDAL, Kyrre GLETTE	227
Power Dissipation in Basic Global Clock Distribution Networks Artur Ł. SOBCZYK, Arkadiusz W. ŁUCZYK, Witold A. PLESKACZ	231
Partitioning Optimization by Recursive Moves of Hierarchically Built Clusters Roman BAZYLEVYCH, Ihor PODOLSKYY, Lubov BAZYLEVYCH	235
A Mixed Approach for Unified Logic Diagnosis Alexandre ROUSSET, Alberto BOSIO, Patrick GIRARD, Christian LANDRAULT, Serge PRAVOSSOUDOVITCH, Arnaud VIRAZEL	239
Design and Analysis of a New Self-Testing Adder Which Utilizes Polymorphic Gates Lukas SEKANINA	243
A HW/SW Architecture to Reduce the Effects of Soft-Errors in Real-Time Operating System Services Mohammad Hossein NEISHABURI, Mohammad Reza KAKOEE, M. DANESHTALAB, Saeed SAFARI, Zainalabedin NAVABI	247
Multiple Errors Detection Technique for RAM Sergei B. MUSIN, Alexander A. IVANIUK, Vyacheslav N. YARMOLIK	251
Test Pattern Generator for Delay Faults Tomasz RUDNICKI, Andrzej HŁAWICZKA	255
 Session VII: Fault Tolerance I <hr/>	
An Experimental Analysis of SEU Sensitiveness on System Knowledge-based Hardening Techniques Oscar RUANO, Pilar REYES, Juan A. MAESTRO, Luca STERPONE, Pedro REVIRIEGO	261
A Novel Parity Bit Scheme for SBox in AES Circuits Giorgio DI NATALE, Marie-Lise FLOTTES, Bruno ROUZEYRE	267
 Session VIII: Analog & RF Design <hr/>	
Designing Time-to-Digital Converter for Asynchronous ADCs Dariusz KOŚCIELNIK, Marek MIŚKOWICZ	275
Algorithm for DRM Signal Recognition in Time Domain and Hardware Realization Lukáš RUČKAY, Jiří NEDVĚD	281
RF Transformer Model Parameters Measurement Vytautas DUMBRAVA, Linas SVILAINIS	287

Session IX: Fault Tolerance II

Improving Tolerance to Power-Supply and Temperature Variations in Synchronous Circuits	295
Jorge SEMIÃO, J. FREIJEDO, Juan J. RODRÍGUEZ-ANDINA, Fabian VARGAS, Marcelino Bicho SANTOS, Isabel Maria CACHO TEIXEIRA, Joao Paulo TEIXEIRA	
A Framework for Self-Healing Radiation-Tolerant Implementations on Reconfigurable FPGAs	301
Manuel G. GERICOTA, Luís F. LEMOS, Gustavo R. ALVES, José M. FERREIRA	
Flip-Flops and Scan-Path Elements for Nanoelectronics	307
Rene KOTHE, Heinrich T. VIERHAUS	
Proposal of VLIW Architecture for Application Specific Processors with Built-in-Self-Repair Facility via Variable Accuracy Arithmetic	313
Paweł PAWŁOWSKI, ADAM DĄBROWSKI, Mario SCHÖLZEL	

Poster Session III

Dedicated Architecture for Double Precision Matrix Multiplication in Supercomputing Environment	321
Paweł RUSSEK, Kazimierz WIATR	
Design Issues of a Low Frequency Low-Pass Filter for Medical Applications Using CMOS Technology	325
András TIMÁR, Márta RENCZ	
Feasibility of Image Compression in FPGA-based Neural Networks	329
Vladimir HAVEL, Karel VLČEK	
IP Integration Overhead Analysis in System-on-Chip Video Encoder	333
Antti RASMUS, Ari KULMALA, Erno SALMINEN, Timo D. HÄMÄLÄINEN	
Quadrature-Phase Topology of a High Frequency Ring Oscillator	337
Ábel VÁMOS	
Reticle Exposure Plans for Multi-Project Wafers	341
Rung-Bin LIN, Da-Wei HSU, Ming-Hsine KUO, Meng-Chiou WU	
Low Cost, Low Power, Intelligent Brake Temperature Sensor System for Automotive Applications	345
Gyula BAKONYI-KISS, Zoltan SZUCS	
Determining MOSFET Parameters in Moderate Inversion	349
Matthias BUCHER, Antonios BAZIGOS, Władysław GRABIŃSKI	
Evolutionary System for Analog Test Frequencies Selection with Fuzzy Initialization	353
Tomasz GOLONEK, Damian GRZECHCA, Jerzy RUTKOWSKI	
Fault Injection and Simulation for Fault Tolerant Reconfigurable Duplex System	357
Pavel KUBALÍK, Jiří KVASNIČKA, Hana KUBÁTOVÁ	
Intrusion Detection System Intended for Multigigabit Networks	361
Jan KOŘENEK, Petr KOBIERSKÝ	
Open Defects Caused by Scratches and Yield Modelling in Deep Sub-micron Integrated Circuit	365
Włodzimierz JONCA	

Session X: Test Quality & Test Generation

- Transition Faults Testing Based on Functional Delay Tests** 371
Eduardas BAREIŠA, Vacius JUSAS, Kęstutis MOTIEJŪNAS, Rimantas ŠEINAUSKAS
- Redundancy and Test-Pattern Generation for Asynchronous Quasi-Delay-Insensitive Combinational Circuits** 377
Aristides EFTHYMIU
- Prototyping Generators for On-line Test Vector Generation Based on PSL Properties** 383
Yann ODDOS, Katell MORIN-ALLORY, Dominique BORRIONE

Session XI: Model Checking & Debugging

- On Variable Selection in SAT-LP-based Bounded Model Checking of Linear Hybrid Automata** 391
Marc HERBSTTRITT, Bernd BECKER, Erika ÁBRAHÁM, Christian HERDE
- SAT-Based Equivalence Checking Based on Circuit Partitioning and Special Approaches for Conflict Clause Reuse** 397
Fabricio V. ANDRADE, Márcia C. M. OLIVEIRA, Antônio O. FERNANDES, Claudionor José N. COELHO Jr.
- Debug Patterns for Efficient High-level SystemC Debugging** 403
Frank ROGIN, Erhard FEHLAUER, Christian HAUFE, Sebastian OHNEWALD

Session XII: Analog & MEMS testing

- Memory Based Analogue Signal Generation Implementation Issues for BIST** 411
Thomas O. SHEA, Ian GROUT, Jeffrey RYAN
- Developing Virtual ADC Testing Environment in MAPLE** 417
Petr STRUHOVSKÝ, Ondřej ŠUBRT, Jiří HOSPODKA, Pravoslav MARTINEK
- ESD Failures of Integrated Circuits and Their Diagnostics Using Transmission Line Pulsing** 423
Zbigniew PIĄTEK, Jerzy F. KOŁODZIEJSKI, Witold A. PLESKACZ
- MEMS Testing by Vibrating Capacitor** 429
János MIZSEI, M. REGGENTE