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IEEE RTP 2006

October 10, 2006

9:00AM-5:00PM Workshop:
Pattern Effect and its Impact on Advanced Thermal Processing of Semiconductors

October 11, 2006

8:15AM Conference Opening

8:30AM Keynote Presentation
Process-Integration Challenges with up-to-date Modulation of Scaling Laws 1
S. Nakai, Fujitsu, Japan

9:15AM Keynote Presentation
Growing Importance of Fundamental Understanding on the Source of Process Variations 5
S. Sato, NEC Yamagata, Japan

10:00AM Invited Presentation
Laser Annealing Technology and Device Integration Challenges 11
A. Shima, Hitachi, Tokyo, Japan

10:30AM Invited Presentation
Influence of the Atmosphere on Ultra-Thin Oxynitride Film for Precisely Controlled Plasma Nitridation Process 15
K. Saki, M. Tamaoki, T. Shimizu, S. Ito, S. Mori, A. Shimizaki, I. Mizushima, A. Yamamoto, Toshiba, Japan

11:00AM Invited Presentation
Double-Pulsed Laser Annealing Technologies and Related Applications 21
T. Kudo, Sumimoto Heavy Industries, Kanagawa, Japan

11:30AM Invited Presentation
Ni-silicide/Si and SiGe(C) Contact Technology for ULSI Applications 31
O. Nakatsuka, S. Zaima, A. Sakai, M. Ogawa, Nagoya University, Japan

12:00M -1:00PM Lunch Break

1:00PM Invited Presentation
Ultra-shallow Junction Formation by Plasma Doping and Flash Lamp Annealing 39
K. Tsutsui, K. Majima, Y. Fugakawa, K. Kakushima, Tokyo Institute of Technology, Yokohama, Japan
Y. Sasaki, C-G. Jim, H. Ito, B. Mizuno, Ultimate Junction Technologies, Osaka, Japan
H. Iwai, H. Sauddin, P. Ahmet, Frontier Collaborative Research Center, Tokyo Institute of Technology, Yokohama, Japan

1:30PM Invited Presentation
Millisecond Annealing with Flashlamps: Tool and Process Challenges 47
T. Gebel, L. Rebohle, R. Fendler, W. Hentsch, FHR Anlagebau, Ottendorf-Okrilla
W. Skorupa, M. Voelskow, W. Anwand, R. A. Yankov, Forschungszentrum Rossendorf

2:00PM Invited Presentation
The Progress in Ultra Thin Gate Dielectric for System LSI Application 57
J. Yugami, S. Tsujikawa, M. Inoue, M. Mizutani, T. Hayashi, Y. Nishida, H. Umeda, Renesas Technology, Hyogo, Japan

2:30PM Invited Presentation
Flash Lamp Annealing Latest Technology for 45nm Device and Future Devices 65
H. Kiyama, Dainippon Screen, Japan

3:00PM-3:15 Coffee Break

3:15PM Invited Presentation
Process Integration Issues with Spike, Laser and Flash Anneal Implementation for 90 and 65nm Technologies 73
Th. Feudel, M. Horstmann, L. Herrmann, M. Herden, M. Gerhardt, D. Greenlaw, AMD Saxony, Dresden, Germany
P. Fisher, J. Kluth, AMD Corporation/IBM, Hopewell Junction, USA

3:45PM Invited Presentation
Ultra-Shallow Junction Formed by Plasma Doping and Laser Annealing 79
S. Heo, H. Hwang, GIST, Gwang-Ju, Korea

4:15PM Invited Presentation
Kinetics of Shallow Junction Formation: Physical Mechanisms 85
Hal Kennel, M.D. Giles, M. Diebel, P.H. Keys, J. Hwang, S. Govindaraju, M. Liu, A. Budrevich, Intel, Hillsboro, USA

4:45PM Invited Presentation
Mechanical Stress in Silicon Based Materials: Evolution Upon Annealing and Impact on Device Performance 93
P. Morin, STMicroelectronics, Crolles, France

7:00PM Banquet Dinner
IEEE RTP'06 Achievement Award Ceremony

October 12, 2006

8:30AM
Flash Annealing Technology for USJ: Modeling and Metrology 103
J. Gelpey, S. McCoy, D. Camm, Mattson Technology Canada, Vancouver, Canada
W. Lerch, S. Paul, Mattson Thermal Products, Dornstadt, Germany
P. Pichler, Fraunhofer IISB, Erlangen, Germany
J. O. Borland, JOB Consulting, Aiea, USA
P. Timans, Mattson Technology, Fremont, USA

9:00AM Invited Presentation
Fundamental Mechanisms for Reduction of Leakage Current of Silicon Oxide and Oxynitride through RTP-Induced Phonon-Energy Coupling 111
Z. Chen, J. Guo, P. Ong, University of Kentucky, Lexington, USA

9:30AM Invited Presentation
Non-Destructive Characterization of Metal-Semiconductor Interfaces by Raman Scattering 117
H. Harima, Kyoto Institute of Technology, Kyoto, Japan

10:00AM
High-Resolution Transmission Electron Microscopy of Interfaces between Thin Nickel Layers on Si(001) after Nickel Silicide Formation under Various Annealing Conditions **121**
T. Isshiki, K. Nishio, T. Sasaki, H. Harima, M. Yoshimoto, Kyoto Institute of Technology, Kyoto, Japan
T. Fukada, W. S. Yoo WaferMasters, San Jose, USA

10:30AM
NBTI Immune First Plasma Nitridation SiON with Multiple Single-Wafer Tools for 45nm node Gate Dielectrics **127**
M. Tanaka, S. Koyama, E. Hasegawa, S. Shishiguchi, M. Hane, NEC Kanagawa, Japan
C. Olsen, Applied Materials, Santa Clara, USA

11:00AM
Non-contact, Non-destructive Crystal Quality Characterization of Ultra-shallow Ion Implanted Silicon Wafers before and after Annealing **133**
M. Yoshimoto, H. Nishigaki, H. Harima, T. Isshiki, Kyoto Institute of Technology, Kyoto, Japan
K. Kang, W. S. Yoo, WaferMasters, San Jose, USA

11:30AM
Thermal Controllability of High Temperature (> 1400 °C) Rapid Thermal Oxidation for SiC MOSFET **141**
S. Ogata, T. Oka, ULVAC, Kanagawa, Japan
K. Tsuda, M. Nakayama, ULVAC-RIKO, Kanagawa, Japan
R. Kosugi, National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba Ibaraki, Japan

12:00M -1:00PM Lunch Break

1:00PM
Sub-30nm MOSFET Fabrication Technology Incorporating Precise Dopant Profile Design Using Diffusion-less High-Activation Laser Annealing **147**
M. Narihiro, T. Iwamoto, T. Yamamoto, T. Ikezawa, K. Yakoh, M. Tanaka, A. Mineji, Y. Okuda, K. Uejima, S. Shishiguchi, M. Hane, NEC, Kanagawa, Japan

1:30PM
Micro-scale Sheet Resistance Measurement on Ultra Shallow Junctions **153**
C. L. Petersen, R. Lin, P.F. Nielsen, CAPRES A/S Burnabay, Canada
D. Petersen, CAPRES A/S Lingby, Denmark

2:00PM
Rapid Thermal Processing Strategies for Highly Uniform and Repeatable Process Results on Patterned Wafers **159**
Woo Sik Yoo, WaferMasters, San Jose, USA

2:30PM
Pattern Effects with the Mask Off… **177**
Z. Nenyei, J. Niess, W. Lerch, W. Dietl Mattson Thermal Products, Dornstadt, Germany
P. Timans, Mattson Technology, Fremont, USA
P. Pichler, Fraunhofer IISB, Erlangen, Germany

3:00PM-3:15 Coffee Break

3:15PM
Deep Melt Laser Thermal Annealing for Power Field Effect Transistor **193**
T. Gutt, Infenion Technologies, Neubiberg, Germany
H. Schulze, T. Rupp, Germany, Infenion Technologies, Austria,
J. Venturini, SOPRA, Gennevilliers, France

3:45PM
RTP Diffusion and Junction formation in Si, GaAs and InP **198**
S. Shishiyanu, Technical University of Moldova, Chisinau, Moldova

4:15PM
Low Thermal Budget Activation of B in Si
H. Bourdon, A. Halimaoui, A. Talbot, D. Dutartre, STMicroelectronics, Crolles, France
J. Venturini, SOPRA, Gennevilliers, France
O. Marcelot, CEMES, Toulouse, France

4:45PM
Raman Study on the Process of Si Advanced Integrated Circuits
S. Nishibe, T. Sasaki, H. Harima, Kyoto Institute of Technology, Kyoto, Japan
K. Kisoda, Wakayama University, Wakayama, Japan,
T. Yamazaki, W. S. Yoo, WaferMasters, San Jose, USA

October 13, 2006

8:30AM
Raman Study of Low-Temperature Formation of Nickel-Silicide Layers
T. Sasaki, S. Nishibe, H. Harima, T. Isshiki, M. Yoshimito, Kyoto Institute
of Technology, Kyoto, Japan
K. Kisoda, Wakayama University, Japan
W. S. Yoo, T. Fukada, WaferMasters, San Jose, CA

9:00AM
Laser Annealed Ni(Ti) Silicides Formation
Y. Setiawan, P.S. Lee, K. L. Pey, X.C. Wang, G. C. Lim, NTU, Singapore
F. L. Chow, Chartered Semiconductor Manufacturing, Woodland Industrial Park, Singapore

9:30AM
Cobalt Silicide Formation Characteristics in a Single Wafer Rapid Thermal
Furnace (SRTF) System
D. Erbetta, T. Marangon, STMicroelectronics, Agrate Brianza, Italy
T. Ueda, T. Fukada, M. Ouaknine, I. J. Malik, W. S. Yoo, WaferMasters, San Jose, USA

10.00AM
Impact of Ni Layer Thickness and Anneal Time on Nickel Silicide Formation
By Rapid Thermal Processing
T. Huelsmann, J. Niess, W. Lerch, Mattson Thermal Products, Dornstadt, Germany
O. Fursenko, D. Bolze, IHP, Im Technologiepark, Frankfurt (Oder), Germany

10:30AM
Changes in Optical Properties during Nickel Silicide Formation and Potential
Impact on Process Results using Various Heating Methods
W. S. Yoo, T. Fukada, I. J. Malik, WaferMasters, San Jose, U.S.A.

11:00AM
Optimization of Annealing for ClusterBoron® and ClusterCarbon™ PMOS SDE
K. Sekar, W. Krull, SemEquip, Inc., North Billerica, USA
K. Verheyden, K. Funk, ASM Europe, Almere, The Netherlands

11:30AM
Process Characterization of Single Wafer Rapid Thermal Furnace System
with a Vacuum Loadlock
D. Garroux, Altis Semiconductor, Corbeil Essonnes, France
T. Fukada, T. Ueda, M. Odera, M. Ouaknine, W. S. Yoo, WaferMasters, San Jose,

12:00M -1:00PM Lunch Break

1:00PM
Improvement of Within Wafer Uniformity of Device Parameters by Gradient
Temperature Control with Bell Jar Type Hot Wall RTP
K. W. Lee, S. Kim, P. Frisella, B. Jacobs, G. Cai, R. Reece, Axcelis Beverley, USA
N. Y. Kwak, C. Y. Ham, K. C. Joo, D. H. Lee, S. W. Park, S. K. Park, Hynix Semiconductor,
Kyungki-do, Korea

1:30PM
Device Scaling Effest on the Spectral Absorptance of Wafer Front Side
K. Fu, Yu-Bin Chen, Pei-feng Hsu, Florida Institute of Technology, Melbourne, USA,
Z.M. Zhang, Woodruff School of Mechanical Engineering,
Georgia Institute of Technology, Atlanta, USA

2:00PM
Insertion Error in LPRT Temperature Measurements
Y. Qu, E. Puttitwong, J. R. Howell, O. A. Ezekoye, The University of Texas, Austin, USA

2:30PM
Hot Plate Emissivity Effect in Low Temperature Annealing
T. Fukada, W. S. Yoo, WaferMasters, San Jose, USA

3:00PM
Calibration of Low Temperature Cable-Less Lightpipe Pyrometer
on the NIST PEB Test Bed Between 50 °C and 225 °C
B. K. Tsai, K. G. Kreider, W. A. Kimes, NIST, Gaithersburg, USA

3:30OM
Adjourn