

2006 13th IEEE International Conference on Electronics, Circuits and Systems

**Nice, France
10-13 December 2006**

Volume 1 of 3



IEEE Catalog Number:
ISBN 10:
ISBN 13:

CFP06773-PRT
1-4244-0394-4
978-1-4244-0394-3

Table of Contents

| | | |
|--|---|-----------------|
| A1L-A | PLENARY TALK – GEORG BOECK | |
| Time: | Monday, December 11, 2006, 9:30 - 10:20 | |
| Place: | Auditorium | |
| RF-CMOS Integrated Circuits for Wireless Communications | | No Paper |
| <i>Georg Boeck</i> | | |

| | | |
|--|---|----|
| A2L-A | ANALOG MODELING | |
| Time: | Monday, December 11, 2006, 10:40 - 12:20 | |
| Place: | Auditorium | |
| Chair: | <i>Andrei Vladimirescu; University of Berkeley, USA</i> | |
| 10:40 | Distributed RLC Interconnect: Analytical Modelling Expressions for Crosstalk Noise Estimation | 1 |
| H J Kadim, L.M. Coulibaly, Liverpool JM University | | |
| 11:00 | A New RF SiCMOS SDD Model for Quantifying Individual Contribution to Distortion from Transistor’s Nonlinear Parameters | 5 |
| Ali Abuelmaatti, Iain Thayne, University of Glasgow | | |
| 11:20 | Noise Modeling for Charge Amplification and Sampling | 9 |
| Patrick Pittet, Université Claude Bernard Lyon 1; Guo-Neng Lu, UCBL - LENAC; Laurent Quiquerez, UCBL LENAC | | |
| 11:40 | General Model for the Deployment of Time-Delay Elements in Transistorized Electronic Circuits | 13 |
| Luis Nero Alves, Universidade de Aveiro; Luis Barbosa, Instituto de Telecomunicações; Rui Aguiar, Universidade de Aveiro | | |
| 12:00 | Multiconductor Transmission Lines Sensitivity via Two-Dimensional Laplace Transform | 17 |
| <i>Lubomir Brancik, Brno University of Technology</i> | | |

| | | |
|---|--|----|
| A2L-B | BIOMEDICAL CIRCUITS & SYSTEMS I | |
| Time: | Monday, December 11, 2006, 10:40 - 12:20 | |
| Place: | Gallieni I | |
| Chair: | <i>Mohamad Sawan; Ecole Polytechnique Montreal, Canada</i> | |
| 10:40 | Design and Analysis of a Class-E Frequency-Controlled Transcutaneous Energy Transfer System | 21 |
| Ahmad Mizannojehdehi, Maitham Shams, Carleton University; Tofy Mussivand, Cardiovascular Devices Centre | | |
| 11:00 | Multiparameters Monitoring for Long Term In-Vivo Characterization of Electrode-Tissues Contacts | 25 |
| Guillaume Lesbros, École Polytechnique de Montréal; Mohamad Sawan, Ecole Polytechnique de Montréal | | |

| | | |
|--------------|---|-----------|
| 11:20 | An Efficient Micro-Stimulator Array Using Unitary-Size DAC with Adiabatic Baseband Scheme | 29 |
| | Cihun-Siyong Alex Gong, Chun-Hsien Su, Muh-Tian Shiue, National Central University; Yin Chang, National Yang-Ming University | |
| 11:40 | Design of Self-Sampling Based ASK Demodulator for Implantable Microsystem | 33 |
| | Cihun-Siyong Alex Gong, Muh-Tian Shiue, National Central University; Yin Chang, National Yang-Ming University; Chun-Hsien Su, National Central University | |
| 12:00 | Comparison of Transconductance Reduction Techniques for the Design of a Very Large Time-Constant CMOS Integrator..... | 37 |
| | Ioannis Pachnis, Andreas Demosthenous, Nick Donaldson, University College London | |

A2L-C SPECIAL SESSION - ADC

Time: Monday, December 11, 2006, 10:40 - 12:20
Place: Gallieni II
Chairs: Anas Hamoui; *McGill University, Montreal, Canada*
Franco Maloberti; *University of Pavia, Italy*

| | | |
|--------------|--|-----------|
| 10:40 | Continuous-time Sigma-Delta Modulators for Highly Digitised Receivers | 41 |
| | Lucien Breems, Robert van Veldhoven, NXP Semiconductors; Kathleen Philips, Philips; Robert Rutten, Gunnar Wetzker, NXP Semiconductors | |
| 11:00 | Quadrature Mismatch Shaping with a Complex, Data Directed Swapper | 46 |
| | Stijn Reekmans, Benoit Catteau, Pieter Rombouts, Ludo Weyten, Ghent University | |
| 11:20 | Design of Cascaded Continuous-Time Sigma-Delta Modulators | 50 |
| | Susana Paton, Manuel Sánchez-Renedo, Universidad Carlos III; Luis Hernandez, Enrique Prefasi, Universidad Carlos III de Madrid; Andreas Wiesbauer, Antonio Di Giandomenico, David San Segundo, Infineon Technologies Austria | |
| 11:40 | Use of the Step Invariant Transform to Design a 2nd Order Continuous Time Complex Sigma-Delta ADC | 54 |
| | Niall Duncan, University College Cork; Anthony Dunne, Freescale Semiconductor; Michael Peter Kennedy, University College Cork | |
| 12:00 | Sigma-Delta Solutions for Future Wireless Handhelds..... | 58 |
| | Ana Rusu, Ismail Mohammed, Royal Institute of Technology Stockholm | |

A2L-D RF LNA

Time: Monday, December 11, 2006, 10:40 - 12:20
Place: Gallieni III
Chair: Didier Belot; *STMicroelectronics, Grenoble, France*

| | | |
|--------------|--|-----------|
| 10:40 | Analysis of Wideband CMOS Low Noise Amplifiers Using Current-Reuse Configuration..... | 62 |
| | Saul Rodriguez, Royal Institute of Technology Stockholm; Li-Rong Zheng, Mohammed Ismail, KTH | |

| | | |
|--------------|---|-----------|
| 11:00 | Concurrent Dual-Band Low Noise Amplifier for 802.11a/g WLAN Applications | 66 |
| | Ouail El Gharniti, Eric Kerhervé, Jean Baptiste Begueret, IXL Laboratory; Didier Belot, ST Microelectronics, Crolles | |
| 11:20 | Design and Implementation of BiFET LNAs for W-CDMA / IEEE 802.11a Applications..... | 70 |
| | Cristian Pavão Moreira, University of Bordeaux; Eric Kerhervé, Pierre Jarry, IXL Laboratory; Didier Belot, ST Microelectronics, Crolles | |
| 11:40 | Inversion Coefficient Based Design of RF CMOS Low-Noise Amplifiers | 74 |
| | Nikolaos Mavredakis, Matthias Bucher, Technical University of Crete | |
| 12:00 | A Low-Voltage CMOS LNA Design Utilizing the Technique of Capacitive Feedback Matching Network | 78 |
| | Chung-Yu Wu, NCTU; Fadi Shahrouy, Nationa Chiao Tung University | |

A2L-E ANALOG FILTERS

Time: Monday, December 11, 2006, 10:40 - 12:20
Place: Gallieni A
Chair: Andreia Cathelin; *STMicroelectronics, Grenoble, France*

| | | |
|--------------|---|-----------|
| 10:40 | Differential-Mode/Common-Mode Feedforward Transconductor for Low-Voltage Gm-C Filters..... | 82 |
| | Phanumas Khumsat, Klanarong Noulkaew, Prince of Songkla University; Apisak Worapishet, Mahanakorn University of Technology; Theerachet Soorapanth, National Science and Technology Development Agency, Thailand | |
| 11:00 | A High-Linear Low-Voltage CMOS Tunable Transconductor for VHF Filtering | 86 |
| | Belen Calvo, Santiago Celma, Maria Teresa Sanz, University of Zaragoza; Jaime Ramirez-Angulo, New Mexico State University | |
| 11:20 | A Low-Voltage III-Order Log-Domain Filter in Standard CMOS Technology with Tunable Frequency | 90 |
| | Andrea Maniero, Andrea Bevilacqua, Andrea Gerosa, Andrea Neviani, Università di Padova | |
| 11:40 | Automatic Tuning of Continuous Time Adaptive Bandpass Filter..... | 94 |
| | Saleh Al-Araji, Kahtan Mezher, Etisalat University College; Hassan Al-Jasmi, Etisalat | |
| 12:00 | Oscillation-Based Test Structure and Method for OTA-C Filters | 98 |
| | Masood-UI Hasan, Yichuang Sun, University of Hertfordshire | |

A2L-F DSP I

Time: Monday, December 11, 2006, 10:40 - 12:20
Place: Gallieni B
Chair: Lars Wanhammar; *Linkoping University, Sweden*

| | | |
|--------------|--|------------|
| 10:40 | An FFT Core for DVB-T/DVB-H Receivers | 102 |
| | Ainhoa Cortés, Juan Francisco Sevillano, Igone Vélez, Andoni Irizar, CEIT and Tecnum | |

| | | |
|--------------|--|-----------------|
| 11:00 | An All-Digital Clock Frequency Capturing Circuitry for NRZ Data Communications..... | 106 |
| | Muhammad Elrabaa, King Fahd University of Petroleum and Minerals | |
| 11:20 | A Methodology for Design Space Exploration in Embedded DSP Applications | 110 |
| | George Economakos, Kostas Anagnostopoulos, Isidoros Sideris, National Technical University of Athens | |
| 11:40 | Design and Implementation of a Correlation-Based DSP Software for Narrowband Power Line Communication Receiver..... | 114 |
| | Housseem Hajji, CIRTA'COM; Adel Ghazel, SUP'COM | |
| 12:00 | A Novel Merged Multiplier-Accumulator Embedded in DSP Coprocessor..... | 119 |
| | Hadi Parandeh-Afshar, Mohsen Ahmadvand, Saeed Safari, University of Tehran | |
| <hr/> | | |
| A3L-A | PLENARY TALK – CHRISTIAN ENZ | |
| Time: | Monday, December 11, 2006, 13:50 - 14:40 | |
| Place: | Auditorium | |
| | Low-power Wireless Vision Sensors Network for Context Awareness | No Paper |
| | <i>Christian Enz</i> | |
| <hr/> | | |
| A4L-A | DATA CONVERTERS I | |
| Time: | Monday, December 11, 2006, 14:50 - 16:30 | |
| Place: | Auditorium | |
| Chair: | Dominique Dallet; <i>IXL Lab, Bordeaux, France</i> | |
| 14:50 | Delta-Sigma Modulators for Power-Efficient A/D Conversion in High-Speed Wireless Communications | 123 |
| | Anas Hamoui, McGill University; Franco Maloberti, University of Pavia | |
| 15:10 | A Segmented Analog Calibration Scheme for Low-Power Multi-Bit Pipeline ADCs..... | 128 |
| | Olujide Adeniran, Andreas Demosthenous, University College London | |
| 15:30 | Power Optimization for Pipelined ADCs with Open-Loop Residue Amplifiers | 132 |
| | Athon Zanicopoulos, Pieter Harpe, Hans Hegt, Arthur van Roermund, Eindhoven University of Technology | |
| 15:50 | A 2nd Order 1-Bit Complex Switched Capacitor Sigma-Delta ADC with 90dB SNR in a 180kHz Bandwidth | 136 |
| | Alan Bannon, Anthony Dunne, Daniel O'Hare, Matthew Miller, Freescale Semiconductor; Omid Oliaei, University of Massachusetts | |
| 16:10 | A 6b 100MS/s 0.28mm² 5mW 0.18um CMOS F/I ADC with a Novel Folder Reduction Technique | 140 |
| | Sanghoon Hwang, Junho Moon, Seunghwi Jung, Minkyu Song, Dongguk University | |

A4L-B DIGITAL ARCHITECTURES

Time: Monday, December 11, 2006, 14:50 - 16:30
Place: Gallieni I
Chair: Odysseas Koufopavlou; *University of Patras, Greece*

- 14:50 An Integrated Digital Architecture for the Real-Time Reconstruction in a VSiP Sensor** 144
Anthony Kolar, Universite Pierre et Marie Curie; Tarik Graba, Andréa Pinna, Olivier Romain, Laboratoire des Instruments et Systemes d'Ile-de-France; Thomas Ea, ISEP; Bertrand Granado, Laboratoire des Instruments et Systemes d'Ile-de-France
- 15:10 CodeRAKE: A New Small-Area Scalable Architecture for the Multi-User/Multi-Code RAKE Receiver** 148
Mazen Youssef, LICM, University Paul Verlaine-Metz; Camille Diou, LICM; Fabrice Monteiro, University of Metz; Abbas Dandache, LICM
- 15:30 An Experimental Analysis of a New Mixed Grain-Based Dynamically Reconfigurable Architecture** 152
Luca Sterpone, Politecnico di Torino
- 15:50 Rethinking Processor Design: Parameter Correlations** 156
Nana Sam, Sally McKee, Cornell University; Prabhakar Kudva, IBM Research
- 16:10 Supporting a Dynamic Program Signature: an Intrusion Detection Framework for Microprocessors** 160
Koji Inoue, Kyushu Univ.

A4L-C FPGA IMPLEMENTATION

Time: Monday, December 11, 2006, 14:50 - 16:30
Place: Gallieni II
Chair: Chiheb Rebai; *Supcom, Tunis, Tunisia*

- 14:50 Power Modeling and Efficient FPGA Implementation of Color Space Conversion** 164
Faycal Bensaali, University of Hertfordshire; Abbes Amira, Shrutisagar Chandrasekaran, Brunel University, West London
- 15:10 An Efficient Bit-Detection and Timing Recovery Circuit for FPGAs** 168
Paolo Zicari, University of Calabria Italy; Pasquale Corsonello, University of Calabria; Stefania Perri, University of Calabria Italy
- 15:30 Design Space Exploration of Division Over GF(2^m) on FPGA: a Digit-Serial Approach** 172
William Chelton, Mohammed Benaissa, University of Sheffield
- 15:50 FPGA Implementations of a Simplified Retinex Image Processing Algorithm** 176
Tommaso Balercia, Andrea Zitti, Henry Francesconi, DEIT; Simone Orcioni, Università Politecnica delle Marche; Massimo Conti, DEIT
- 16:10 High Throughput Architecture of JPEG Compressor for Color Images Targeting FPGAs** 180
Luciano Agostini, UFRGS; Ivan Silva, UFRN; Sergio Bampi, UFRGS

| | | |
|--------------|--|------------|
| A4L-D | RF OSCILLATORS | |
| Time: | Monday, December 11, 2006, 14:50 - 16:30 | |
| Place: | Gallieni III | |
| Chair: | Gilles Jacquemod; <i>LEAT, Sophia, France</i> | |
| 14:50 | Multi-Mode Wideband Voltage Controlled Oscillator | 184 |
| | Dr. Ulrich Rohde, Ajay Poddar, Synergy Microwave Corporation | |
| 15:10 | High-Performance VCO for 5-GHz WLANs in 0.35-um CMOS Standard Technology | 188 |
| | Domenico Zito, Domenico Pepe, Bruno Neri, University of Pisa | |
| 15:30 | Design of a 1.2 V Low Phase Noise 1.6 GHz CMOS Buffered Quadrature VCO with Automatic Amplitude Control | 192 |
| | Owen Casha, Ivan Grech, Joseph Micallef, Edward Gatt, University of Malta | |
| 15:50 | Analysis of Harmonic Distortion in the Colpitts Oscillator | 196 |
| | Melita Pennisi, Gaetano Palumbo, Salvatore Pennisi, University of Catania | |
| 16:10 | A Design Approach for Low Phase Noise 5GHz Complementary Quadrature Oscillator..... | 200 |
| | Yukio Hattori, Hiroki Sato, Akira Hyogo, Keitaro Sekine, Tokyo University of Science | |

| | | |
|--------------|---|------------|
| A4L-E | VOLTAGE REFERENCE | |
| Time: | Monday, December 11, 2006, 14:50 - 16:30 | |
| Place: | Gallieni A | |
| Chair: | Thierry Taris; <i>IXL Lab, Bordeaux, France</i> | |
| 14:50 | NMOS Low Drop-Out Regulator with Dynamic Biasing | 204 |
| | Gianluca Giustolisi, Gaetano Palumbo, University of Catania; Christian Falconi, Arnaldo D'Amico, University of Rome Tor Vergata | |
| 15:10 | Novel Approach to Low-Voltage Low-Power Bandgap Reference Voltage in Standard CMOS Process..... | 208 |
| | Christian Fayomi, Universite du Quebec A Montreal; Stephen J. Stratz, ASIC North Inc | |
| 15:30 | Design of Fuel-Cell Powered DC-DC Converter for Portable Applications in Digital CMOS Technology | 212 |
| | Andrea Boni, Alessandro Carboni, Alessio Facen, University of Parma | |
| 15:50 | High Linear Voltage References for on-Chip CMOS Temperature Sensor | 216 |
| | Joseph Tsai, Herming Chiueh, National Chiao Tung University | |
| 16:10 | Low-Power Wordline Voltage Generator for Low-Voltage Flash Memory | 220 |
| | Tzu-Ming Wang, Ming-Dou Ker, National Chiao-Tung University; Steve Yeh, Ya-Chun Chang, Winbond Electronics Corporation | |

| | | |
|--------------|---|------------|
| A4L-F | DSP II | |
| Time: | Monday, December 11, 2006, 14:50 - 16:30 | |
| Place: | Gallieni B | |
| Chair: | Stanislaw Piestrak; <i>University of Metz, France</i> | |
| 14:50 | Characterization of in-Phase/Quad-Phase Digital Downconversion via Special Sampling Scheme | 224 |
| | Jesse Somann, Yong Kim, Air Force Institute of Technology | |
| 15:10 | Multiple Input Digital Arbiter with Timestamp Assignment for Asynchronous Sensor Arrays..... | 228 |
| | Michael Hofstätter, Peter Schön, Ahmed Nabil Belbachir, Ernst Bodenstorfer, ARC Seibersdorf research GmbH | |
| 15:30 | Efficient Circuitry for Computing tau-adic Non-Adjacent Form | 232 |
| | Kimmo Järvinen, Juha Forsten, Jorma Skyttä, Helsinki University of Technology | |
| 15:50 | Time-Domain Synthesis of IIR Phase Equalizers | 236 |
| | Mladen Vucic, Goran Molnar, University of Zagreb | |
| 16:10 | Spread Spectrum PWM Signal Generator for Fully Digital Audio Amplifier..... | 240 |
| | Akihiko Yoneya, Nagoya Institute of Technology | |

A5P-G ANALOG CIRCUITS & SIGNAL PROCESSING

Time: Monday, December 11, 2006, 14:50 - 16:50
Place: Poster Area 1

| | | |
|--|--|------------|
| | Explaining Hysteresis in Electronic Circuits: Robust Design and Simulation Examples | 244 |
| | Ahmed Elwakil, University of Sharjah; Dr. Serdar Ozoguz, Istanbul Technical University | |
| | A Q-Enhanced Biquadratic Gm-C Filter for High Frequency Applications | 248 |
| | Ramin Zanbaghi, Mohsen Moezzi, Mojtaba Atarodi, Armin Tajalli, Sharif University of Technology | |
| | Hazard Free Sawtooth Oscillator and its Application in Ultra Low Current Monitoring..... | 252 |
| | Lei Zhang, Zhiping Yu, Xiangqing He, Tsinghua University | |
| | A Wide Bandwidth Voltage-Follower with Low Distortion and High Slew Rate..... | 256 |
| | Nikolaos Charalampidis, Khaled Hayatleh, Bryan Hart, John Lidgey, Oxford Brookes University | |
| | A Novel CMOS Mini-LVDS Receiver for Flat-Plane Application | 260 |
| | Chung-Yuan Chen, Tai-Ping Sun, National Chi Nan University | |
| | Design Guidelines for Two-Stage Cascode-Compensated Amplifiers | 264 |
| | Hamed Aminzadeh, Reza Lotfi, Ferdowsi University of Mashhad; Somayyeh Rahimian, University of Tehran | |

| | |
|---|------------|
| Simple Logic Threshold Conversion Circuits | 268 |
| Cong-Kha Pham, University of Electro-Communications | |
| High Speed High Precision Voltage-Mode MAX and MIN Circuits | 272 |
| Sarang Kazemi Nia, Abdollah Khoei, Kheirollah Hadidi, Urmia University | |
| A Sigma-Delta Closed-loop Digital Microfluxgate Magnetometer | 276 |
| Fabrice Gayral, Elisabeth Delevoye, Cyril Condemine, Eric Colinet, Marc Béranger, CEA LETI; Fabien Mieyeville, Frédéric Gaffiot, Ecole Centrale de Lyon | |
| Fully Integrated Headphone Detector | 280 |
| David Guilherme, Nuno Caldeira, João Risques, Chipidea - Microelectrónica S.A. | |
| Periodically Time-Varying Two-Terminals at a Steady State, Description and Identification..... | 284 |
| Radoslaw Klosinski, University of Zielona Góra | |
| Sub-1V Oguey's Current Reference Without Resistance..... | 288 |
| Fabrice Guignes, Edith Kussener, ISEN-Toulon L2MP | |
| CMOS Realization of a Quantized-Output Classifier Circuit..... | 292 |
| Merih Yildiz, Shahram Minaei, Cem Goknar, Dogus University | |
| Biobjective Hybrid Evolutionary Algorithm Applied to Resonator Filters of Arbitrary Topology..... | 296 |
| Maria José Pereira Dantas, Catholic University of Goiás; Paulo Henrique P. de Carvalho, University of Brasília; Leonardo Da C. Brito, Federal University of Goiás | |
| Transition from Sinusoidal to Relaxation Oscillations in Emitter-Coupled Multivibrators | 300 |
| Igor Filanovsky, University of Alberta; Chris Verhoeven, TU Delft | |

A5P-H SENSORS III

Time: Monday, December 11, 2006, 14:50 - 16:50

Place: Poster Area 2

| | |
|--|------------|
| Wireless System for Temperature Measurement in Wheels, Based on the ISM Band | 304 |
| Paul Bustamante, CEIT; Mikel Osinalde, Tecnun; Gonzalo Solas, Jon Del Portillo, CEIT | |
| Integrated Instrumental Chain for Magnetic Pulse measurement in Strong Static Field Environment..... | 310 |
| Vincent Frick, Joris Pascal, Luc Hebrard, Jean-Philippe Blonde, CNRS/ULP - UMR 7163 | |
| Global Shutter CMOS Image Sensor with Wide Dynamic Range | 314 |
| Alexander Belenky, Ben-Gurion University of the Negev; Alexander Fish, University of Calgary; Orly Yadid-Pecht, Ben-Gurion University of the Negev | |

The Performance Modeling of Ring Laser Gyro in Inertial Navigation318
Shahram Mohammad Nejad, Iran University of Science and Technology; Maryam Pourmahyabadi, IUST

A5P-J

RF

Time: Monday, December 11, 2006, 14:50 - 16:50
Place: Poster Area 3

Contributions to the Analysis and Design of an ADPLL322
Cyril Joubert, ESIEE; Jean Francois Bercher, ESYCOM/ESIEE; Genevieve Baudoin, ESIEE; Thierry Divel, Pierre Baudin, ST-Microelectronics

Analysis and Design of Antireflection and Frequency Selective Surfaces with Stratified and Inhomogeneous Media326
Mohsen Choubani, Fethi Choubani, Ali Gharsallah, Faculté des sciences de Tunis; J. David, Institut National Polytechnique de Toulouse; N.E Mastorakis, Hellenic Naval Academy

Design of a SiGe Reconfigurable Power Amplifier for RF Applications: Device and Multi-Standard Considerations331
Nathalie Deltimple, Eric Kerhervé, Yann Deval, IXL Laboratory; Didier Belot, ST Microelectronics, Crolles; Pierre Jarry, IXL Laboratory

Differential Cross-Coupled CMOS VCOs with Resistive and Inductive Tail Biasing.....335
Sergio Gagliolo, Giacomo Pruzzo, Daniele Caviglia, University of Genoa

Low Power CMOS Transmitter for Biomedical Sensing Devices339
Thierry Dupire, Ecole Polytechnique de Montréal; Louis-Francois Tanguay, Ecole Polytechnique; Mohamad Sawan, Ecole Polytechnique de Montréal

A Novel Compact Dual-Mode Bandpass Filter Using Fractal Shaped Resonators343
Elias Hanna, Pierre Jarry, Eric Kerhervé, Jean-Marie Pham, IXL Laboratory

A5P-K

BIOMEDICAL CIRCUITS & SYSTEMS II

Time: Monday, December 11, 2006, 14:50 - 16:50
Place: Poster Area 4

Fuzzy Logic Based System for Classification of Atrial Fibrillation Cardiac Arrhythmias347
Ali Messaoud, Ecole Nationale d'Ingénieurs de Sfax; Mohamed Ben Messaoud, Abdennaceur Kachouri, Faiçal Sellami, Laboratoire d'Electronique et de Technologies de l'Information

Design and Implementation of a Monolithic Programme-Controlled System for Retinal Prosthesis351
Cihun-Siyong Alex Gong, National Central University; Yin Chang, National Yang-Ming University; Muh-Tian Shiue, National Central University

| | |
|--|------------|
| Reduction of Color Variability in Color Image Segmentation | 355 |
| H. Ben M'hadheb, Unité de recherche ATSI; Ali Douik, Ecole Nationale d'Ingénieurs de Monastir; M.M. Fendri, Unité de recherche ATSI; Med. Annabi, Unité de recherche SEPE | |
| High-Resolution 1H NMR Microspectroscopy Using an Implantable Micro-Coil | 359 |
| Nicoleta Baxan, Adrian Rengle, LRMN CNRS UMR 5012; Jean-François Château, LENAC EA 3730; André Briguet, LRMN CNRS UMR 5012; Guillaume Pasquet, Pierre Morin, LENAC EA 3730; Latifa Fakri-Bouchet, LRMN CNRS UMR 5012 | |
| An FPGA-Based Genetic Microarray Processing Device | 363 |
| Pedro Gómez, Francisco Díaz, Bogdan Belean, Raul Malutan, Benjamin Stetter, Rafael Martínez, Victoria Rodellar, Universidad Politécnica de Madrid | |
| CMOS BDJ Detector Array with Charge Preamplifiers for Sensitive Biochemical Analysis | 367 |
| Genaro Carrillo, Guo-Neng Lu, LENAC laboratory; Patrick Pittet, Université Claude Bernard Lyon 1; Kai Zhao, LENAC laboratory | |

A5P-L

TEST IC

Time: Monday, December 11, 2006, 14:50 - 16:50
Place: Poster Area 5

| | |
|--|------------|
| Design of Reliable CMOS Phase-Locked Loops | 371 |
| Chin-Long Wey, Chi-Shu Huang, National Central University; Shaolei Quan, Michigan State University | |

| | |
|---|------------|
| Novel Current Sensing Circuit for IDDQ Testing | 375 |
| Jeong Beom Kim, Kangwon National University | |

| | |
|--|------------|
| Algorithms for Compositions of Arithmetic Transforms and Their Extensions | 379 |
| Yu Pang, Katarzyna Radecka, Concordia University; Zeljko Zilic, Mcgill University | |

| | |
|---|------------|
| A Low-Power and Low Silicon Area Testable CMOS LNA Dedicated to 802.15.4 Sensor Network Applications | 383 |
| Mikael Cimino, Magali de Matos, Hervé Lapuyade, IXL Laboratory; Thierry Taris, University of Bordeaux 1; Yann Deval, Jean Baptiste Bégueret, IXL Laboratory | |

| | |
|---|------------|
| Tamper Resistivity Analysis for Nano-Meter LSI with Process Variations | 387 |
| Makoto Ikeda, Hiroshi Yamauchi, Kunihiro Asada, University of Tokyo | |

A5P-M

ADVANCED TECHNOLOGIES (NANO, BAW, ETC) II

Time: Monday, December 11, 2006, 14:50 - 16:50
Place: Poster Area 6

| | |
|--|------------|
| Synthesis Method for BAW Filters Computation | 391 |
| Ji Fan, Matthieu Chatras, Dominique Cros, Limoges university | |

| | |
|---|------------|
| Reconfiguration of Bulk Acoustic Wave Filters: Application to WLAN 802.11b/g (2.40-2.48 GHz) | 395 |
| Moustapha El Hassan, Eric Kerhervé, Yann Deval, Alexandre Shirakawa, IXL Laboratory; Didier Belot, ST Microelectronics, Crolles | |
| Unbalancing the I/O Pins Partitioning for Minimizing Inter-Tier Vias in 3D VLSI Circuits | 399 |
| Sandro Sawicki, Renato Hentschke, Marcelo Johann, Ricardo Reis, UFRGS | |
| Limits to a Correct Evaluation in RTD-Based Ternary Inverters | 403 |
| Juan Núñez, José María Quintana, María José Avedillo, Instituto de Microelectrónica de Sevilla | |
| Tunable Photonic Crystals with Ferroelectric Materials | 407 |
| Valerie Vigneras, Laurent Oyhenart, PIOM Laboratory | |

A6L-A DATA CONVERTERS II

Time: Monday, December 11, 2006, 16:50 - 18:30

Place: Auditorium

Chair: Chiheb Rebai; *Supcom, Tunis, Tunisia*

| | |
|--|------------|
| 16:50 Nyquist-Criterion Based Design of a CT Sigmadelata-ADC with a Reduced Number of Comparators | 411 |
| Jeroen De Maeyer, Pieter Rombouts, Ludo Weyten, Ghent University | |
| 17:10 An Ultra Low Power Successive Approximation ADC with Selectable Resolution in 0.13 Um CMOS Technology | 415 |
| Anna Arbat, Angel Dieguez, Josep Samitier, Universitat de Barcelona | |
| 17:30 Optimizing Resistances and Capacitances of a Continuous-Time Sigma-Delta ADC | 419 |
| Laurent de Lamarre, University of Paris VI; Marie-Minerve Louerat, LIP6; Andreas Kaiser, IEMN-ISEN | |
| 17:50 Pixel-Level ADC by Small Charge Quantum Counting | 423 |
| Arnaud Peizerat, CEA/LETI; Marc Arquès, Patrick Villard, Jean-Luc Martin, CEA; Gerard Bouvier, INPG | |
| 18:10 Enhanced Split-Architecture Delta-Sigma ADC | 427 |
| KyeHyung Lee, Gabor C. Temes, Oregon State Univ. | |

A6L-B RF POWER AMPLIFIERS & ARCHITECTURES

Time: Monday, December 11, 2006, 16:50 - 18:30

Place: Gallieni I

Chair: Fadhel Ghannouchi; *Ecole Polytechnique Montreal, Canada*

| | |
|--|------------|
| 16:50 Generalized Analytical Design Equations for Variable Slope Class-E Power Amplifiers | 431 |
| Mustafa Acar, Anne Johan Annema, Bram Nauta, University of Twente | |

| | | |
|--------------|--|------------|
| 17:10 | ACPR Performance Study for Modified LINC Amplifier | 435 |
| | Mohamed Abd El-Aal, Fadhel Ghannouchi, École Polytechnique de Montréal | |
| 17:30 | Issues on the Design of a Variable Power LINC Amplifier System in SiGe Operating at 2.4 GHz..... | 439 |
| | Ivan Grech, Charmaine Demanuele, Joseph Micallef, Edward Gatt, University of Malta | |
| 17:50 | Envelope/Phase Delays Correction in an EER Radio Architecture..... | 443 |
| | Jean Francois Bercher, ESYCOM/ESIEE; Corinne Berland, ESYCOM / Groupe ESIEE | |
| 18:10 | Integrated MM-Wave MIMO Antenna with Directional Diversity Using MEMS Technology | 447 |
| | Sylvain Ranvier, TKK; Fabien Ferrero, Cyril Luxey, Robert Staraj, Gilles Jacquemod, LEAT; Clemens Icheln, Pertti Vainikainen, TKK | |

A6L-C IMAGE PROCESSING

Time: Monday, December 11, 2006, 16:50 - 18:30
Place: Gallieni II
Chairs: Hussain Al-Ahmad; *Etisalat University College, UAE*
Orly Yadid-Pecht; Ben Gurion University, Israel

| | | |
|--------------|---|------------|
| 16:50 | A Robust Blind Image Watermarking Scheme in the SPIHT-Compressed Bit- Stream..... | 451 |
| | Fouad Khelifi, Ahmed Bouridane, Fatih Kurugollu, Queen's university Belfast | |
| 17:10 | Contribution of Custom Instructions on SoPC for Iris Recognition Application..... | 455 |
| | Thomas Ea, Frédéric Amiel, Alicja Michalowska, Florence Rossant, Amara Amara, ISEP | |
| 17:30 | A Threshold-Based Deinterlacing Algorithm Using Motion Compensation and Directional Interpolation..... | 459 |
| | Hossein Mahvash Mohammadi, École Polytechnique de Montréal; Pierre Langlois, Yvon Savaria, Ecole Polytechnique de Montréal | |
| 17:50 | Coefficient, Pass and Code-Block Parallel Architecture for FBP Coding in JPEG2000..... | 463 |
| | Xin Fan, Chao Xu, Peking University | |
| 18:10 | Design of an Area-Efficient Multiplierless Processing Element for Fast Two Dimensional Image Convolution | 467 |
| | Deepak Gangadharan, Mahesh Raveendranath, Andrzej Sluzek, Nanyang Technological University | |

| | | |
|--------------|--|------------|
| A6L-D | RF PASSIVE COMPONENTS | |
| Time: | Monday, December 11, 2006, 16:50 - 18:30 | |
| Place: | Gallieni III | |
| Chair: | Matthieu Chatras; <i>XLIM Lab, Limoges, France</i> | |
| 16:50 | Modeling and Design of the CMOS Boot-Strapped Inductor for 5-6 GHz Applications..... | 471 |
| | Domenico Zito, Domenico Pepe, Bruno Neri, University of Pisa; Graziella Scandurra, University of Messina | |
| 17:10 | Integrated RF Devices in Suspended Technology..... | 475 |
| | Herve Leblond, Dominique Baillargeat, Pierre Blondy, XLIM, UMR CNRS 6172 | |
| 17:30 | Wide-Band Frequency-Independent Equivalent Circuit Model for Integrated Spiral Inductors on (Bi)CMOS Technology | 478 |
| | Domenico Zito, Domenico Pepe, Bruno Neri, University of Pisa | |
| 17:50 | Performance of Si-Integrated Wide-Band Single-Ended Switched Capacitor Arrays | 482 |
| | Luis Mendes, Instituto Politécnico de Leiria / Instituto de Telecomunicações; João Vaz, Maria Rosário, Instituto de Telecomunicações | |

| | | |
|--------------|--|------------|
| A6L-E | HIGH LEVEL CIRCUITS & SYSTEMS | |
| Time: | Monday, December 11, 2006, 16:50 - 18:30 | |
| Place: | Gallieni A | |
| Chair: | Jean-Baptiste Begueret; <i>IXL Lab, Bordeaux, France</i> | |
| 16:50 | GA-SVM Optimization Kernel Applied to Analog IC Design Automation | 486 |
| | Manuel Barros, Instituto Politecnico de Tomar; Jorge Guilherme, Instituto Politecnico Tomar; Nuno Horta, Instituto Superior Tecnico | |
| 17:10 | AIDA: Analog IC Design Automation Based on a Fully Configurable Design Hierarchy and Flow | 490 |
| | Gonçalo Neves, Barros Manuel, IT/IST; Nuno Horta, Instituto Superior Tecnico | |
| 17:30 | Impact of Charge Injection on System-Level Performance of a Discrete-Time GSM Receiver | 494 |
| | Rayan Mina, Jean-Charles Grasset, STMicroelectronics; Jean-Francois Naviner, Ecole Nationale Supérieure des télécommunications | |
| 18:10 | A New Active Pixel Design Using μ-Si TFT Technology to Improve Brightness Uniformity of Organic Displays | 498 |
| | Archanmael Gaillard, Régis Rogel, Samuel Crand, Tayeb Mohammed-Brahim, IETR | |

| | | |
|--------------|--|------------|
| A6L-F | MULTIPLIERS, ADDERS & DIVIDERS | |
| Time: | Monday, December 11, 2006, 16:50 - 18:30 | |
| Place: | Gallieni B | |
| Chair: | Eric Tournier; <i>LAAS, Toulouse, France</i> | |
| | | |
| 16:50 | A Parallel-in Serial-Out Multiplier Using Redundant Representation for A Class of Finite Fields | 502 |
| | Ashkan Hosseinzadeh Namin, Univerity Of Windsor; Huapeng Wu, Majid Ahmadi, University of Windsor | |
| 17:10 | Delay Efficient 32-Bit Carry-Skip Adder | 506 |
| | Yu Shen Lin, Damu Radhakrishnan, State University of New York | |
| 17:30 | Request-Skip Adders: CMOS Standard Cell Data Dependent Adders | 510 |
| | Robin Perrot, Nadine Azémard, Philippe Maurine, LIRMM | |
| 17:50 | Delay Optimized Redundant Binary Adders | 514 |
| | Bijoy Jose, Damu Radhakrishnan, State University of New York | |
| 18:10 | Modeling of Delay Variability Due to Supply Variations in Pass-Transistor and Static Full Adders..... | 518 |
| | Massimo Alioto, University of Siena; Gaetano Palumbo, University of Catania | |
| <hr/> | | |
| B1L-A | PLENARY TALK - MOHAMAD SAWAN | |
| Time: | Tuesday, December 12, 2006, 08:30 - 09:20 | |
| Place: | Auditorium | |
| Chair: | Jean-Baptiste Begueret; <i>IXL Lab, Bordeaux, France</i> | |
| | | |
| 8:30 | Implantable Smart Medical Microsystems: Limits and Challenges | 522 |
| | Mohamad Sawan, Ecole Polytechnique de Montréal | |
| <hr/> | | |
| B2L-A | ANALOG AMPLIFIERS I | |
| Time: | Tuesday, December 12, 2006, 09:30 - 10:50 | |
| Place: | Auditorium | |
| Chair: | Andreas Kaiser; <i>IEMN, Lille, France</i> | |
| | | |
| 9:30 | Cryogenic SiGe Hetero-Junction Bipolar Transistors from Standard Technologies for Low Noise FLL..... | 525 |
| | Damien Prele, Universite Pierre et Marie Curie-Paris6; Gérard Sou, Geoffroy Klisnick, Michel Redon, UPMC-LISIF; Eric Breelle, Michel Piat, Fabrice Voisin, APC | |
| 9:50 | Improved Chopper Stabilized Amplifier for Offset and 1/f Noise Cancellation | 529 |
| | Andrea Agnes, Franco Maloberti, Giuseppe Martini, University of Pavia | |
| 10:10 | Optimum Sizing and Compensation of Two-Stage CMOS Amplifiers Based on a Time-Domain Approach..... | 533 |
| | Rui Santos-Tavares, Nuno Paulino, João Goes, João Oliveira, UNINOVA | |

10:30 **A 5.2-mW, 2.5-Gb/s Limiting Amplifier for OC-48 SONET System**537
Kwisung Yoo, Gunhee Han, Yonsei University; Sung Min Park, Ewha Womans
University

B2L-B **CODING/DECODING ALGORITHMS**
Time: Tuesday, December 12, 2006, 09:30 - 10:50
Place: Gallieni I
Chair: Bertrand Le Gal; *IXL Lab, Bordeaux, France*

9:30 **Optimized Arithmetic Hardware Design with the Aid of Hierarchical Formal
Verification**.....541
Nikhil Kikkeri, Peter-Michael Seidel, Southern Methodist University

9:50 **An Efficient H.264 VLSI Advanced Video Encoder**545
Konstantinos Babionitakis, George Lentaris, Konstantinos Nakos, NKUA; Dionysios
Reisis, Nikolaos Vlassopoulos, National and Kapodistrian University of Athens; Gregory
Doumenis, George Georgakarakos, John Sifnaios, GDT

10:10 **A VLSI Decoder for the Golden Code**.....549
Barbara Cerato, Guido Maserà, Emanuele Viterbo, Politecnico di Torino

10:30 **A Low Power Pulsed Edge-Triggered Latch for Survivor Memory Unit of Viterbi
Decoder**.....553
Wei-Li Su, National Chiao-Tung University; Po-Tsang Huang, Harming Chiueh, National
Chiao Tung University; Wei Hwang, National Chiao-Tung University

B2L-C **CIRCUIT TECHNIQUES & OPTIMIZATION I**
Time: Tuesday, December 12, 2006, 09:30 - 10:50
Place: Gallieni II
Chair: Nathalie Deltimple; *IXL Lab, Bordeaux, France*

9:30 **RC-Chain: a Simple Model of Delay with a Ramp Input**557
Giuseppe Di Cataldo, Rosario Mita, Gaetano Palumbo, University of Catania; Massimo
Poli, University of Siena

9:50 **Error Detection Code Efficiency for Secure Chips**561
Vincent Maingot, Regis Leveugle, TIMA Laboratory

10:10 **A Hybrid Method for the Recognition of Acceptor Splice Sites**565
Mahmood Akhtar, Eliathamby Ambikairajah, University of New South Wales; Julien
Epps, National Information Communication Technology, Australia.

10:30 **A Variable Duty Cycle with High-Resolution Synchronous Mirror Delay**569
Kai-Wei Hong, Chien-Hsien Lee, Kuo-Hsing Cheng, Chen-Lung Wu, National Central
University; Wei-Bin Yang, Industrial Technology Research Institute

| | | |
|--------------|--|------------|
| B2L-D | RF BUILDING BLOCKS | |
| Time: | Tuesday, December 12, 2006, 09:30 - 10:50 | |
| Place: | Gallieni III | |
| Chair: | Georg Boeck; <i>TU Berlin, Germany</i> | |
| 9:30 | Optimized Design of a Digital IQ Demodulator Suitable for Adaptive Predistortion of 3rd Generation Base Station PAs | 573 |
| | Chiheb Rebai, Haythem Ayari, Adel Ghazel, SUP'COM; Slim Boumaiza, Fadhel Ghannouchi, University of Calgary | |
| 9:50 | Design of Sampling-Based Downconversion Stage for Multistandard RF Subsampling Receiver..... | 577 |
| | Rim Barrak, Adel Ghazel, SUP'COM; Fadhel Ghannouchi, University of Calgary | |
| 10:10 | Shot-Noise Analysis in Circuits with Large Signal Excitations Using Harmonic Balance Simulators | 581 |
| | Mike Tempel, Georg Boeck, Technische Universität Berlin | |
| 10:30 | Maximum Frequency of Operation of CMOS Static Frequency: Theory and Design Techniques | 584 |
| | Kaushik Sengupta, Indian Institute of Technology Kharagpur; Hossein Hashemi, University of Southern California, LA | |

| | | |
|--------------|---|------------|
| B2L-E | CURRENT MODE | |
| Time: | Tuesday, December 12, 2006, 09:30 - 10:50 | |
| Place: | Gallieni A | |
| Chair: | Herve Barthelemy; <i>L2MP, Marseille, France</i> | |
| 9:30 | Programmable Gain Amplifiers Based on High-Linearity MOS Current Dividers..... | 588 |
| | Maria Teresa Sanz, Santiago Celma, Belen Calvo, University of Zaragoza | |
| 9:50 | Compact, Low-Power, Analogue Building Blocks Derived from MOSFETs Translinear Loops | 592 |
| | Massimo Barbaro, Gian Nicola Angotzi, University of Cagliari | |
| 10:10 | Constant gm, Rail-to-Rail Input Transconductance Stage with Output Common Mode Current Compensation..... | 596 |
| | Kirill Kozmin, Jonny Johansson, Luleå University of Technology | |
| 10:30 | New 1.5-V CMOS Current Feedback Operational Amplifier | 600 |
| | Ahmed Madian, Cairo University; Soliman Mahmoud, German University, Cairo; Ahmed Soliman, Cairo University | |

| | | |
|--------------|---|------------|
| B2L-F | TEST & RELIABILITY I | |
| Time: | Tuesday, December 12, 2006, 09:30 - 10:50 | |
| Place: | Gallieni B | |
| Chair: | Herve Lapuyade; <i>IXL Lab, Bordeaux, France</i> | |
| 9:30 | Simulating the Effects of Process Variation on Capacitive Crosstalk..... | 604 |
| | Arani Sinha, Cadence; Shahin Nazarian, USC; T.M. Mak, Intel | |

| | | |
|--------------|--|------------|
| 9:50 | Power and Failure Analysis of CAM Cells Due to Process Variations..... | 608 |
| | Mahmoud Bennaser, Csaba Andras Moritz, University of Massachusetts | |
| 10:10 | An Embedded Rectifier-Based Built-in-Test Circuit for CMOS RF Circuits..... | 612 |
| | Guoyan Zhang, Ronan Farrell, Institute of Microelectronics and Wireless Systems | |
| 10:30 | System-Level ESD Protection Design with On-Chip Transient Detection Circuit | 616 |
| | Cheng-Cheng Yen, Ming-Dou Ker, Pi-Chia Shin, National Chiao-Tung University | |

B3L-A ANALOG AMPLIFIERS II

Time: Tuesday, December 12, 2006, 11:10 - 12:30
 Place: Auditorium
 Chair: Nathalie Deltimple; *IXL Lab, Bordeaux, France*

| | | |
|--------------|---|------------|
| 11:10 | A Low-Power Highly Linear CMOS Transconductance Topology..... | 620 |
| | Hashem Zare-Hoseini, Izzet Kale, Richard Cs Morling, University of Westminster | |
| 11:30 | A Low-Noise Low-Offset Op Amp in 0.35um CMOS Process | 624 |
| | Zhineng Zhu, Raghu Tumati, Scott Collins, Rosemary Smith, David Kotecki, University of Maine | |
| 11:50 | Bandwidth Extension of High-Gain CMOS Stages Using Active Negative Capacitance | 628 |
| | David Comer, Donald Comer, Jonathan Perkins, Kevin Clark, Adrian Genz, Brigham Young University | |
| 12:10 | A 1.5-V, Constant-Gm, Rail-to-Rail Input Stage Operational Amplifier | 632 |
| | Akram Masoom, Khayrollah Hadidi, Urmia University | |

B3L-B IMAGE PROCESSING & CODING

Time: Tuesday, December 12, 2006, 11:10 - 12:30
 Place: Gallieni I
 Chair: Majid Ahmadi; *University of Windsor, Canada*

| | | |
|--------------|---|------------|
| 11:10 | A Time-Consistent Video Segmentation Algorithm Designed for Real-Time Implementation..... | 636 |
| | Mohammed El Hassani, philips semiconductors; Stéphanie Jehan-Besson, Greyc Laboratory; Delphine Rivasseau, philips semiconductors; David Tschumperlé, Luc Brun, Marinette Revenu, Greyc Laboratory; Marc Duranton, philips research nat.lab | |
| 11:30 | Fuzzy Classification, Image Segmentation and Shape Analysis for Human Face Detection..... | 640 |
| | M. Ben Hmida, National Engineering School of Sfax; Yousra Ben Jemaa, ENIS | |
| 11:50 | Research on an Improved Anisotropic High-pass Filtering Algorithm Based on the Step Angle Searching | 644 |
| | Pan Qing, Yan Guoping, Huazhong University of Science and Technology | |

12:10 Unequal Error Protective and Standard Compatible Multiple Descriptions Coding for Image Communication.....648
Arash Behgoo, Ali Aghagolzadeh, University of Tabriz; Mohammad Shahram Moin, Iranian Telecommunication Research Center

B3L-C CIRCUIT TECHNIQUES & OPTIMIZATION II

Time: Tuesday, December 12, 2006, 11:10 - 12:30

Place: Gallieni II

Chair: Christian Piguet; *CSEM, Neuchatel, Switzerland*

11:10 Comparison of Three Methods of Eliminating Musical Tones in Speech Denoising Subtractive Technique.....652
Anis Ben Aicha, Sofia Ben Jebara, SUP'COM

11:30 Arithmetic Reduction of the Static Power Consumption in Nanoscale CMOS656
Peter Nilsson, Lund University

11:50 A New Transistor-Level Layout Generation Strategy for Static CMOS Circuits660
Cristiano Lazzari, Cristiano Santos, Ricardo Reis, UFRGS

B3L-D RF DEVICES

Time: Tuesday, December 12, 2006, 11:10 - 12:30

Place: Gallieni III

Chair: Cyril Luxey; *LEAT, Nice, France*

11:10 Analysis of the Intermodulation Distortion and Nonlinearity of Common-Base SiGeC HBTs664
Farah Guillot, IMEP; Patrice Garcia, STMicroelectronics; Mireille Mouis, IMEP; Didier Belot, ST Microelectronics, Crolles

11:50 A High Speed, Low Voltage to High Voltage Level Shifter in Standard 1.2V, 0.13um CMOS668
Bert Serneels, Catholic University of Leuven; Michiel Steyaert, Katholieke Universiteit Leuven; Wim Dehaene, Catholic University of Leuven

12:10 Broadband Modelling of a High Efficiency Rectenna for Batteryless RFID Systems.....672
Alexandre Douyere, Jean Daniel Lan Sun Luk, Alain Celeste, Frédéric Alicalapa, University of La Reunion

B3L-E ANALOG TELECOM

Time: Tuesday, December 12, 2006, 11:10 - 12:30

Place: Gallieni A

Chair: Didier Belot; *STMicroelectronics, Grenoble, France*

11:10 Analysis and Optimization of Powerline Coupling Circuit for CENELEC-PLC Modem.....676
Kamel Fezzani, EBSYS; Chiheb Rebai, Adel Ghazel, SUP'COM

| | | |
|--------------|---|------------|
| 11:30 | Analog Circuits for Symbol-Likelihood Computation | 680 |
| | Matthias Frey, Signal and Information Processing Laboratory; Hans-Andrea Loeliger, ETH Zurich; Patrick Merkli, Sensirion AG | |
| 11:50 | A Simple Method for Transmission with Reduced Crosstalk and Echo | 684 |
| | Frédéric Broydé, Evelyne Clavelier, Excem | |
| 12:10 | Benefits of Prior Speech Segmentation for Best Time- Frequency Visualisation Using Renyi's Entropy..... | 688 |
| | Daoud Boutana, University of Jijel, Algeria; Messaoud Benidir, Univ. of Paris-Sud | |

B3L-F TEST & RELIABILITY II

Time: Tuesday, December 12, 2006, 11:10 - 12:30

Place: Gallieni B

Chair: Ming-Dou Ker; *National Chiao-Tung University, Taiwan*

| | | |
|--------------|---|------------|
| 11:10 | A Pipeline Architecture Incorporating a Low-Cost Error Detection and Correction Mechanism..... | 692 |
| | Andreas Floros, Yiorgos Tsiatouhas, University of Ioannina; Angela Arapoyanni, University of Athens; Themistoklis Haniotakis, Southern Illinois Univesity | |
| 11:30 | Arithmetic Transforms of Imprecise Datapaths by Taylor Series Conversion | 696 |
| | Yu Pang, Katarzyna Radecka, Concordia University; Zeljko Zilic, Mcgill University | |
| 11:50 | Testing QCA Modular Logic..... | 700 |
| | Sayeeda Sultana, Shahriar Al Imam, Katarzyna Radecka, Concordia University | |
| 12:10 | Timing-Driven Redundant Contact Insertion for Standard Cell Yield Enhancement..... | 704 |
| | Tetsuya Iizuka, Makoto Ikeda, Kunihiro Asada, University of Tokyo | |

B4L-A PLENARY TALK - MITSUO USAMI

Time: Tuesday, December 12, 2006, 14:00 - 14:40

Place: Auditorium

Chair: Mohamad Sawan; *Ecole Polytechnique Montreal, Canada*

| | | |
|--------------|--|------------|
| 14:00 | Ultra-Small RFID Chip Technology..... | 708 |
| | Mitsuo Usami, Hitachi, Ltd. | |

B5L-A ANALOG BUILDING BLOCKS I

Time: Tuesday, December 12, 2006, 15:00 - 16:20

Place: Auditorium

Chair: Akira Hyogo; *Tokyo University of Science, Japan*

| | | |
|--------------|--|------------|
| 15:00 | A Compensation Method for Magnitude Response Mismatches in Two-Channel Time-Interleaved Analog-to-Digital Converters..... | 712 |
| | Stefan Mendel, Graz University of Technology; Christian Vogel, Christian Doppler Laboratory for Nonlinear Signal Processing | |

| | | |
|--------------|--|------------|
| 15:20 | Analog to Digital Conversion Using a Pulse Width Modulator and an Irregular Sampling Decoder..... | 716 |
| | Luis Hernandez, Enrique Prefasi, Universidad Carlos III de Madrid | |
| 15:40 | High-Efficiency Regulated Charge Pump for Non-Volatile Memories..... | 720 |
| | Alessandro Cabrini, Andrea Fantini, Guido Torelli, University of Pavia | |
| 16:00 | High Efficiency CMOS Charge Pump..... | 724 |
| | Laura Gobbi, Alessandro Cabrini, Guido Torelli, University of Pavia | |

B5L-B COMMUNICATION ALGORITHMS
Time: Tuesday, December 12, 2006, 15:00 - 16:20
Place: Gallieni I
Chair: Herve Lapuyade; *IXL Lab, Bordeaux, France*

| | | |
|--------------|---|------------|
| 15:00 | Reduced Complexity Power Minimization Algorithm for DMT Transmission - Application to Layered Multimedia Services Over DSL | 728 |
| | Charlène Goudemand, Marc Gazalet, François-Xavier Coudoux, Patrick Corlay, Mohamed Gharbi, IEMN | |
| 15:40 | Improving the Security of the SHI Reversible Data Hiding Algorithm | 732 |
| | Siamak Yousefi, Iran University of Science and Technology; Hamid Reza Rabiee, ITRC; Mohammed Ghanbari, Essex University | |
| 16:00 | Teleoperation via Internet with Time-Varying Delay..... | 736 |
| | Ehsan Kamrani, Abas Ramazani, Lorestan University; Fabrice Monteiro, University of Metz | |

B5L-C DIGITAL FILTERS
Time: Tuesday, December 12, 2006, 15:00 - 16:20
Place: Gallieni II
Chair: Duncan Macfarlane; *University of Texas, Dallas, USA*

| | | |
|--------------|--|------------|
| 15:00 | Improved Transient Frequency Response of IIR Filters with Multiple Frequency Initialization | 740 |
| | Jeedella Jeedella, Hussain Al Ahmad, Mohmmad Almualla, Etisalat University College; Jim Noras, University of Bradford | |
| 15:20 | Output Frequencies of A Class of Nonlinear Systems..... | 744 |
| | Xiaofeng Wu, Ziqiang Lang, Stephen Billings, University of Sheffield | |
| 15:40 | ASSUMEs: Heuristic Algorithms for Optimization of Area and Delay in Digital Filter Synthesis | 748 |
| | Levent Aksoy, Istanbul Technical University; Eduardo Costa, UCPel; Paulo Flores, Jose Monteiro, INESC-ID/IST | |
| 16:00 | High Performance Timing Driven Rank Filter..... | 752 |
| | Péter Szántó, Budapest University of Technology and Economics; Gábor Szedő, Xilinx Inc.; Béla Fehér, Budapest University of Technology and Economics | |

| | | |
|--------------|--|------------|
| B5L-D | IMAGE & SPEECH PROCESSING | |
| Time: | Tuesday, December 12, 2006, 15:00 - 16:20 | |
| Place: | Gallieni III | |
| Chairs: | Kunihiro Asada; <i>University of Tokyo, Japan</i> Makoto Ikeda; <i>University of Tokyo, Japan</i> | |
| 15:00 | Camera-Based Digit Recognition System | 756 |
| | David Castells-Rufas, Jordi Carrabina, Universitat Autònoma de Barcelona | |
| 15:20 | A Full-Color QVGA Microdisplay Using Light-Emitting-Polymer on CMOS | 760 |
| | Graeme Kelly, Institute for System Level Integration; Robin Woodburn, Ian Underwood, Dwayne Burns, Roger Monteith, Mark Newsam, Philippa Parmiter, MicroEmissive Displays; Tughrul Arslan, Univeristy of Edinburgh | |
| 15:40 | High-Speed 3-D Measurement System Using Smart Image Sensor and FPGA Based 3-D Engine..... | 764 |
| | Yusuke Yachide, Makoto Ikeda, University of Tokyo; Kunihiro Asada, University of Tokyo | |
| 16:00 | A Micro-Architecture Simulator for Multimedia Stream Processor..... | 768 |
| | Fang-Ju Lin, NCTU; Herming Chiueh, National Chiao Tung University | |

| | | |
|--------------|---|------------|
| B5L-E | SPECIAL SYSTEM – DIGITAL SYSTEMS | |
| Time: | Tuesday, December 12, 2006, 15:00 - 16:20 | |
| Place: | Gallieni A | |
| Chairs: | Dominique Dallet; <i>IXL Lab, Bordeaux, France</i> Guy Gogniat; <i>LESTER, Lorient, France</i> | |
| 15:00 | Intra- and Inter-Processors Memory Size Estimation for Multithreaded MPSoC Modeled in Simulink | 772 |
| | Bilel Belhadj Mohamed, Chiheb Rebai, Adel Ghazel, SUP'COM | |
| 15:20 | Trusted Computing - A New Challenge for Embedded Systems..... | 776 |
| | Romain Vaslin, Guy Gogniat, Jean-Philippe Diguët, Université de Bretagne Sud; Alain Pegatoquet, Texas Instruments | |
| 15:40 | Multi-Bank Memory Allocation for Multimedia Application | 780 |
| | Hanene Ben Fradj, Cécile Belleudy, Michel Auguin, University of Nice Sophia Antipolis; Alain Pegatoquet, Texas Instruments | |
| 16:00 | IP Generation Targeting Multiple Bit-Width Standards | 784 |
| | Bertrand Le Gal, IXL Laboratory; Emmanuel Casseau, R2D2 - IRISA Laboratory | |

| | | |
|--------------|---|------------|
| B5L-F | SPECIAL SESSION - ULTRA WIDE BAND ICS DESIGN | |
| Time: | Tuesday, December 12, 2006, 15:00 - 16:20 | |
| Place: | Gallieni B | |
| Chair: | Jean-Michel Fournier; <i>IMEP, Grenoble, France</i> | |
| 15:00 | Digital Radio Front-End for High Data Rate Impulse UWB System..... | 788 |
| | Dominique Morche, Frederic Hameau, David Lachartre, Gilles Masson, Christopher Mounet, Michael Pelissier, CEA/LETI; Didier Helal, Lydi Smaini, STMicroelectronics; Didier Belot; ST Microelectronics, Crolles | |

| | | |
|--------------|---|------------|
| 15:20 | UWB LNAs Using LC Ladder and Transformers for Input Matching Networks | 792 |
| | Thierry Taris, University of Bordeaux 1; Ouail Elgharniti, Jean Baptiste Begueret, Eric Kerhervé, IXL Laboratory | |
| 15:40 | FM-UWB: A Low-Complexity Constant Envelope LDR UWB Approach | 797 |
| | John Gerrits, John Farserotu, CSEM; John Long, TU Delft | |
| 16:00 | Effect of RF Front-End Parameters on UWB-OFDM Receiver Performances in Presence of Adjacent Channel Interferers..... | 802 |
| | Philippe Lombard, Emilie Ponthus, Emil Novakov, Jean-Michel Fournier, IMEP | |

B6P-G DIGITAL CIRCUITS & SIGNAL PROCESSING

Time: Tuesday, December 12, 2006, 15:00 - 17:00

Place: Poster Area 1

| | | |
|--|--|------------|
| | Two-Dimensional FIR Signal Adapted Filter Banks | 806 |
| | Sheeba V S, Elizabeth Elias, National Institute of Technology, Calicut | |
| | A High Performance VLSI FFT Architecture..... | 810 |
| | Konstantinos Babionitakis, Konstantinos Manolopoulos, Konstantinos Nakos, NKUA; Dionysios Reisis, Nikolaos Vlassopoulos, National and Kapodistrian University of Athens; Vassilios Chouliaras, Loughborough University | |
| | An Efficient HW/SW Implementation of the H.263 Video Coder in FPGA | 814 |
| | Ahmed Ben Atitallah, Patrice Kadionik, IXL-ENSEIRB; Fahmi Ghazzi, LETI-ENIS; Patrice Nouel, IXL-ENSEIRB; Nouri Masmoudi, National Engineering School of Sfax; Hervé Levi, IXL-ENSEIRB | |
| | Ultra Low Voltage CMOS Gates | 818 |
| | Yngvar Berg, Omid Mirmotahari, Per Andreas Norseng, Snorre Aunet, University of Oslo | |
| | SystemC-Defined SIMD Instructions for High Performance SoC Architectures..... | 822 |
| | Vassilios Chouliaras, Konstantia Koutsomyti, Tom Jacobs, Simon Parr, David Mulvaney, Robert Thompson, Loughborough University | |
| | Architecture of an Efficient Area and Flexible Multi-CODEC Processor | 826 |
| | Hee Ju Park, Jeoung Hun Kim, Kyusam Lim, Ji Hwan Park, Korea University | |
| | Oversampled and Noise-Shaped Pulse-Width Modulator for High-Fidelity Digital Audio Amplifier | 830 |
| | Sergio Saponara, Luca Fanucci, Pierangelo Terreni, University of Pisa | |
| | Strategies for Adaptive Nonlinear Noise Reduction Volterra-Wiener Filter Structure Selection | 834 |
| | Pawel Biernacki, University of Technology Wroclaw | |
| | An 11Gb/s CMOS Demultiplexer Using a Redundant Multi-Valued Logic | 838 |
| | Jeong Beom Kim, Sun Hong Ahn, Kangwon National University | |

Implementation of Multiplier Block with Reduced Adder Cost.....842
Somayyeh Rahimian, S. Maryam Mortazavi, S. Mehdi Fakhraie, Omid Shoaei, University
of Tehran

SAD-Based Stereo Matching Circuit for FPGAs846
Stefania Perri, Daniela Colonna, Paolo Zicari, University of Calabria Italy; Pasquale
Corsonello, University of Calabria

B6P-H TELECOMMUNICATION & MULTIMEDIA

Time: Tuesday, December 12, 2006, 15:00 - 17:00

Place: Poster Area 2

Systematic Lossy Error Protection of Video Based on Reduced Spatial Resolution850
Marie Ramon, François-Xavier Coudoux, Marc Gazalet, Mohamed Gharbi, Patrick
Corlay, IEMN

**A Real-Time Control System for Home/Office Appliances Automation, from Mobile
Device Through GPRS Network.....854**
Usman Ali, University Paris 11; Syed Junaid Nawaz, Nazish Jawad, COMSATS Institute
of Information Technology, Abbottabad, CAMPUS

Performance of DSSS Against Repeater Jamming.....858
Hang Wang, Zanj Wang, Jingbo Guo, Tsinghua University

B6P-J SYSTEM ARCHITECTURES & APPLICATIONS

Time: Tuesday, December 12, 2006, 15:00 - 17:00

Place: Poster Area 3

**Committee Machine with Over 95% Classification Accuracy for Combustible Gas
Identification.....862**
Minghua Shi, Amine Bermak, Hong Kong University of Science and Technology

**Analysis of the Thermal Impact of Source-Code Transformations in Embedded
Processors.....866**
Jose Ayala, Candido Mendez, Marisa Lopez-Vallejo, Universidad Politecnica de Madrid

**Hybrid Method for Cereal Grain Identification Using Morphological and Color
Features870**
Mehrez Abdellaoui, ENIM; Ali Douik, Ecole Nationale d'Ingénieurs de Monastir;
Mohamed Annabi, ESSTT

B6P-K SYSTEM INTEGRATION II

Time: Tuesday, December 12, 2006, 15:00 - 17:00

Place: Poster Area 4

**Yield-Driven Redundant Via Insertion Based on Probabilistic Via-Connection
Analysis874**
Jin-Tai Yan, Bo-Yi Chiang, Zhi-Wei Chen, Chung-Hua University

| | |
|---|------------|
| Simulation of SoCs with Embedded Mixed-Signal Cores Using a Verilog High-Speed Virtual Serial Interface | 878 |
| Jan Schat, Philips Semiconductors | |
| Modeling of Feedback Analog Circuits with VHDL..... | 882 |
| Melita Pennisi, Gaetano Palumbo, Rosario Mita, Giuseppe Di Cataldo, University of Catania | |
| 3 Megapixel Camera Signal Processor for Mobile Camera Applications | 886 |
| <i>Kyusam Lim, Hwangyoung So, Sejin Kang, Mtekvision Co., Ltd; Jeoung Hun Kim,</i> | |
| An Implementation of Integrable Low Power Techniques for Modern Cell-Based VLSI Designs | 890 |
| Ming-Chung Lee, NCTU; Herming Chiueh, National Chiao Tung University | |
| Modeling of Operational Amplifier Based on VHDL-AMS | 894 |
| Huabiao Qin, South China University of Technology; Fei Wang, South Chian University of Technology | |
| Effect of Simultaneous Switching Noise on an Analog Filter..... | 898 |
| Erik Backenius, Mark Vesterbacka, Robert Hägglund, Linköping University | |
| A New Dynamic Floating Input D Flip-Flop (DFIDFF) for High Speed and Ultra Low Voltage Divided-by 4/5 Prescaler..... | 902 |
| Jau Ting-Sheng, Industrial Technology Research Institute; Yang Wei-Bin, ITRI; Lo Yu-Lung, National Central University | |
| FPAAs Prototyping of Sigma-Delta Analog Digital Converters | 906 |
| Robert Suszynski, Krzysztof Wawryn, Koszalin University of Technology | |
| Implementation of a Mixed Signal Chip for Multichannel Audio Equalizer with Sigma-delta A/D Conversion..... | 910 |
| Byoung-II Kim, Jin-Yong Hwang, Keun-Pyo Hong, Jae-Sik Lee, Tae-Gyu Chang, Chung-Ang University | |

B6P-L PHOTONICS

Time: Tuesday, December 12, 2006, 15:00 - 17:00
Place: Poster Area 5

| | |
|--|------------|
| Accuracy Improvement by Nonlinearity Reduction in Two-Frequency Laser Heterodyne Interferometer | 914 |
| Shahram Mohammad Nejad, Saeed Olyaei, Iran University of Science and Technology | |
| Optimal Dark Current Reduction in Quantum Well 9 μm GaAs/AlGaAs Infrared Photodetectors with Improved Detectivity | 918 |
| Shahram Mohammad Nejad, Iran University of Science and Technology; Maryam Pourmahyabadi, IUST; Ali Asghar Amidian, ITRC | |

B6P-M NEURAL NETWORKS II

Time: Tuesday, December 12, 2006, 15:00 - 17:00

Place: Poster Area 6

Design and Test of a CMOS MLP Analog Neural Network for Fast on-Board Signal Processing.....922

Laurent Gatet, H el ene Tap-Beteille, Marc Lescure, Daniel Roviras, INP/ENSEEIH; Alain Mallet, CNES

An Analog-Digital Neural Processor for Integrated Sensor Conditioning.....926

Nicolas Medrano, University of Zaragoza; Guillermo Zatorre, Teltronic, S.A.U.; Maria Teresa Sanz, Pedro A. Martinez, Santiago Celma, University of Zaragoza

Exponential Stability for Cellular Neural Networks with Delay.....930

Jinxiang Yang, Southwest University for Nationalities; Shouming Zhong, University of Electronic Science and Technology of China; Xingwen Liu, Southwest University for Nationalities

Using FPGAs to Implement Artificial Neural Networks934

Jos e Mar a Granado-Criado, Miguel  ngel Vega-Rodr guez, Rosa P rez-Utrero, Juan Manuel S nchez-P rez, Juan Antonio G mez-Pulido, University of Extremadura

A LVDS Serial AER Link938

Lourdes Miro-Amarante, Angel Jimenez Fernandez, Alejandro Linares-Barranco, Francisco Gomez-Rodriguez, Rafael Paz Vicente, Gabriel Jimenez Moreno, Anton Civit Balcells, Universidad de Sevilla

FPGA Implementation of Programmable Pulse Mode Neural Network with on Chip Learning for Signature Application.....942

Dorra Sellami Masmoudi, National Engineering School of Sfax; Krid Mohamed, Dammak Alima, ENIS

Design of a Modular and Mixed Neuromimetic ASIC.....946

Jean Tomas, Yannick Bornat, Sylvain Saighi, Timothee L vi, IXL - CNRS 5818; Sylvie Renaud, IXL Laboratory

B7L-A DATA CONVERTERS III

Time: Tuesday, December 12, 2006, 16:40 - 18:20

Place: Auditorium

Chair: Franco Maloberti; *University of Pavia, Italy***16:40 A Continuous-Time Delta-Sigma Modulator for 802.11a/B/G WLAN Implemented with a Hierarchical Bottom-Up Optimization Methodology.....950**

Raf Schoofs, Tom Eeckelaert, Michiel Steyaert, Georges Gielen, Willy Sansen, Katholieke Universiteit Leuven

17:00 A 2--2 Discrete Time Cascaded Sigma-Delta Modulator with NTF Zero Using Interstage Feedback954

Manuel Sanchez-Renedo, Susana Paton, Universidad Carlos III; Luis Hernandez, Universidad Carlos III de Madrid

| | | |
|--------------|--|------------|
| 17:20 | On the Calibration of AD and DA Converters Based on R/betaR Ladder Networks..... | 958 |
| | Carmine Ciofi, Graziella Scandurra, Giuseppe Campobello, Gianluca Cannatà, University of Messina | |
| 17:40 | Continuous-Time Complex Bandpass Delta Sigma Modulator: Key Component for Highly Digitized Receiver | 962 |
| | Nejmeddine Jouida, Chiheb Rebai, Adel Ghazel, SUP'COM; Dominique Dallet, Laboratoire IXL | |
| 18:00 | Scaling Input Signal Swings of Overloaded Integrators in Resonator-Based Sigma- Delta Modulators | 966 |
| | Umut Yazkurt, Bogazici University; Nicolas Beilleau, University of Paris VI; Gunhan Dundar, Bogazici University; Hassan Aboushady, University of Paris VI; Selcuk Talay, Bogazici University; Laurent de Lamarre, University of Paris VI | |

B7L-B TELECOMMUNICATION

Time: Tuesday, December 12, 2006, 16:40 - 18:20
Place: Gallieni I
Chair: Mohamad Obaidat; *Monmouth University, Long Branch, USA*

| | | |
|--------------|---|------------|
| 16:40 | Secured and Seamless Handoff in Wireless Fourth Generation Systems | 970 |
| | F. Zarai, N. Boudriga, Carthage University; Mohammad Obaidat, Monmouth Univeristy | |
| 17:00 | Design and Implementation in FPGA of MIMO Decoder for a 4G Wireless Receiver | 974 |
| | Alberto Jiménez-Pacheco, Ángel Fernández-Herrero, Javier Casajús-Quirós, Universidad Politécnica de Madrid | |
| 17:20 | On the Use of a Performance Indicator for Optimal Pilot Positioning in Multicarrier Systems | 978 |
| | David Bueche, Patrick Corlay, Marc Gazalet, François-Xavier Coudoux, Marc Slachciak, IEMN | |
| 17:40 | Telecommunication Synchronization Development Based on High Level Virtual Prototype | 982 |
| | Celine Guillemot, Laboratoire ICARE; Laurent Andrieux, Laboratoire ICARE and LAAS CNRS | |
| 18:00 | A Low Complexity Simulation Algorithm for TH-UWB MMSE RAKE Receiver in NLOS Channel | 986 |
| | Marina Marjanovic, José Manuel Páez Borrallo, Universidad Politécnica de Madrid | |

B7L-C HIGH SPEED CIRCUITS

Time: Tuesday, December 12, 2006, 16:40 - 18:20
Place: Gallieni II
Chairs: Nathalie Deltimple; *IXL Lab, Bordeaux, France*
Thanos Stouraitis; University of Patras, Greece

| | | |
|--------------|---|------------|
| 16:40 | A 3-Bits DDS Oriented Low Power Consumption 15 GHz Phase Accumulator in a 0.25 um BiCMOS SiGe:C Technology | 991 |
| | Stephane Thuries, Eric Tournier, Jaques Graffeuil, LAAS-CNRS | |

| | | |
|--------------|--|-------------|
| 17:00 | A Digital Frequency Shift Keying Demodulator | 995 |
| | Gerald Arnould, Laboratoire Interfaces Capteurs et Microélectronique (LICM); Fabrice Monteiro, University of Metz; Abbas Dandache, LICM | |
| 17:20 | RF Digital Predistorter for Power Amplifiers of 3G Base Stations | 999 |
| | Anouar Benchahed, CIRTA'COM; Adel Ghazel, SUP'COM; Mohamed Mabrouk, CIRTA'COM; Chiheb Rebai, SUP'COM; M.F. Ghannouchi, Ecole Polytechnique de Montréal | |
| 17:40 | A 20-GHz and 46-GHz, 32x6bit ROM for DDS Application in InP DHBT Technology..... | 1003 |
| | Sanjeev Manandhar, Steven Turner, David Kotecki, University of Maine | |
| 18:00 | 4-Gb/s Low-power PRBS Generator with Wave-pipeline Technique in 0.18-um CMOS | 1007 |
| | Masahiro Sasaki, Makoto Ikeda, University of Tokyo; Kunihiro Asada, University of Tokyo | |

B7L-D UWB & HIGH FREQUENCY LNA
Time: Tuesday, December 12, 2006, 16:40 - 18:20
Place: Gallieni III
Chair: Eric Kerherve; *IXL Lab, Bordeaux, France*

| | | |
|--------------|---|-------------|
| 16:40 | 79 GHz Fully Integrated Fully Differential Si/SiGe HBT Amplifier for Automotive Radar Applications | 1011 |
| | Sebastien Chartier, Bernd Schleicher, Till Feger, Tatyana Purtova, Hermann Schumacher, University of Ulm | |
| 17:00 | A 0.35 um SiGe Low-Noise Amplifier for UWB Receivers with Integrated Interferer Rejection | 1015 |
| | Andrea Bevilacqua, Andrea Maniero, Andrea Gerosa, Andrea Neviani, Università di Padova | |
| 17:20 | A 4mA, 0.25 SiGe, 23GHz BiFET Low Noise Amplifier | 1019 |
| | Thierry Taris, N. Seller, R. Toupe, University of Bordeaux 1; Hervé Lapuyade, Jean Baptiste Begueret, Yann Deval, IXL Laboratory | |
| 17:40 | A Dual Stage GaAs Amplifier for a K-Band Direct Receiver | 1023 |
| | Meik Huber, Stefan von der Mark, Georg Boeck, Technische Universität Berlin | |
| 18:00 | Low Power 3~8-GHz UWB Tuable LNA Design Using SiP Technology | 1026 |
| | Yang Chuan Chen, MediaTek Inc.; Chun-Hsing Li, National Chiao Tung University; J. K. Huang, Chiennan Kuo, Yu Ting Cheng, National Chiao Tung University | |

| | | |
|--------------|---|-------------|
| B7L-E | ADVANCED TECHNOLOGIES (NANO, BAW, ETC) I | |
| Time: | Tuesday, December 12, 2006, 16:40 - 18:20 | |
| Place: | Gallieni A | |
| Chairs: | Stéphane Bila; <i>XLIM Laboratory</i> Mohammed Ismail; <i>Ohio State University</i> | |
| | | |
| 16:40 | Compact Modeling and Applications of CNTFETs for Analog and Digital Circuit Design | 1030 |
| | Fabien Prégaldiny, Jean-Baptiste Kammerer, Christophe Lallement, InESS | |
| | | |
| 17:00 | A Non-Volatile Multi-Level Memory Cell Using Molecular-Gated Nanowire Transistors..... | 1034 |
| | Antoine Jalabert, Fabien Clermidy, CEA-LETI; Amara Amara, ISEP | |
| | | |
| 17:20 | 3D Simulation of Thin-Film Bulk Acoustic Wave Resonators (FBAR) | 1038 |
| | Sylvain Giraud, Stéphane Bila, Michel Aubourg, Dominique Cros, Xlim, Research Institute | |
| | | |
| 17:40 | An Improved Isolation W-CDMA Ladder BAW-SMR Filter | 1042 |
| | Alexandre Shirakawa, Jean-Marie Pham, Pierre Jarry, Eric Kerhervé, IXL Laboratory; Jean-Baptiste David, Fabien Dumont, CEA LETI; Didier Belot, ST Microelectronics, Crolles | |
| | | |
| 18:00 | Intermediate Frequency Lamb Wave Resonators and Filters for RF Receiver Architectures | 1045 |
| | Mathieu Desvergne, CEA/LETI; Yann Deval, IXL Laboratory; Pierre Vincent, CEA-LETI; Jean Baptiste Begueret, IXL Laboratory; Caroline Bernier, CEA-LETI | |

| | | |
|--------------|--|-------------|
| B7L-F | LOGIC CIRCUITS & ARCHITECTURES | |
| Time: | Tuesday, December 12, 2006, 16:40 - 18:20 | |
| Place: | Gallieni B | |
| Chair: | Paul Ampadu; <i>University of Rochester, USA</i> | |
| | | |
| 16:40 | Monostable-Bistable Transition Logic Elements: Threshold Logic Vs. Boolean Logic Comparison..... | 1049 |
| | David Bol, Université catholique de Louvain; José María Quintana, María José Avedillo, Instituto de Microelectrónica de Sevilla; Jean-Didier Legat, Université catholique de Louvain | |
| | | |
| 17:00 | Pre-Conditioning Free Footless DCVSL for High-Performance Datapaths | 1053 |
| | Makoto Ikeda, Diakin Hooi, Kunihiro Asada, University of Tokyo | |
| | | |
| 17:20 | orBDDs Direct Mapping for Structured Logic Circuits | 1057 |
| | Reginaldo Tavares, Universidade Estadual do Rio Grande do Sul; Cristina Meinhardt, Universidade Federal do Rio Grande do Sul; Ricardo Reis, UFRGS | |
| | | |
| 17:40 | Bit Error Rate Analysis for Flip-Flop and Latch Based Interconnect Pipelining | 1061 |
| | Jingye Xu, Masud H. Chowdhury, University of Illinois at Chicago | |
| | | |
| 18:00 | Exact Minimum Logic Factoring via Quantified Boolean Satisfiability..... | 1065 |
| | Hiroaki Yoshida, Makoto Ikeda, Kunihiro Asada, University of Tokyo | |

C1L-A PLENARY TALK – MARC BELLEVILLE

Time: Wednesday, December 13, 2006, 08:30 - 09:20

Place: Auditorium

Evolutions of the Microelectronics Technologies: A Designer Perspective..... No Paper
Marc Belleville

C2L-A ANALOG DESIGN TECHNIQUES

Time: Wednesday, December 13, 2006, 09:30 - 10:50

Place: Auditorium

Chair: Christian Enz; *CSEM, Switzerland***9:30 Designing Analog Circuits with Reduced Biasing Power 1069**
Reza Hashemian, Northern Illinois University**9:50 BiCMOS vs. CMOS Operational Amplifiers for High-Speed Pipelined A/D
Converters 1073**
Cristiano Azzolini, Andrea Boni, University of Parma**10:10 Frequency Response Analysis of Latch Utilized in High-Speed Comparator..... 1077**
Shunsuke Okura, Osaka University; Hajime Shibata, Analog Devices, Inc.; Tetsuro
Okura, Kenji Taniguchi, Osaka Univ.

C2L-B ALGORITHM ARCHITECTURES

Time: Wednesday, December 13, 2006, 09:30 - 10:50

Place: Gallieni I

Chair: Camille Diou; *LICM, Metz, France***9:30 A Systolic Inversion Architecture Based on Modified Extended Euclidean
Algorithm for GF(2^K) Fields 1081**
Apostolos Fournaris, Odysseas Koufopavlou, University of Patras**9:50 Toward a Methodology for Optimizing Algorithm-Architecture Adequacy for
Implementation Reconfigurable System..... 1085**
Ting Liu, Camel Tanougast, Serge Weber, Université Henri Poincaré Nancy I**10:10 Applying Low Power Techniques in AES MixColumn/InvMixColumn
Transformations 1089**
George Selimis, Apostolos Fournaris, Odysseas Koufopavlou, University of Patras**10:30 Lock and Unlock: a Data Management Algorithm for a Security-Aware Cache..... 1093**
Koji Inoue, Kyushu Univ.

C2L-C CALIBRATION METHODS

Time: Wednesday, December 13, 2006, 09:30 - 10:50

Place: Gallieni II

**9:30 An Offset and Gain Calibration Method for Time-Interleaved Analog to Digital
Converters 1097**
Maher Jridi, Dominique Dallet, Guillome Monnerie, Lilian Bossuet, Laboratoire IXL

| | | |
|--------------|---|-------------|
| 9:50 | Leakage Power Minimization of Nanoscale CMOS Circuits via Non-Critical Path Transistor Sizing | 1101 |
| | Bo Fu, Paul Ampadu, University of Rochester | |
| 10:10 | Recursive Least-Squares Lattice Adaptive Algorithm Suitable for Fixed-Point Implementation..... | 1105 |
| | Constantin Paleologu, Andrei Alexandru Enescu, Silviu Ciochina, Politehnica University of Bucharest | |
| 10:30 | Implementation and Synthesis of a Sorting Network..... | 1109 |
| | Navid Zeraatkar, Ali Tavanaie, Reza Talebian, Ferdowsi University of Mashhad; Somayyeh Rahimian, University of Tehran | |

C2L-D IF DELTA SIGMA ADC & FILTERS
Time: Wednesday, December 13, 2006, 09:30 - 10:50
Place: Gallieni III
Chair: Andreia Cathelin; *STMicroelectronics, Grenoble, France*

| | | |
|--------------|---|-------------|
| 9:30 | Design Techniques for Very High Speed Digital Delta-Sigma Modulators Aimed at All-Digital RF Transmitters..... | 1113 |
| | Antoine Frappé, Axel Flament, Bruno Stefanelli, IEMN/ISEN; Raphael Daouphars, LIP6; Andreia Cathelin, STMicroelectronics; Andreas Kaiser, IEMN/ISEN | |
| 9:50 | A Study of High-Frequency Bandpass Delta-Sigma Transmitter Architectures..... | 1117 |
| | Nejdat Demirel, Eric Kerhervé, IXL Laboratory; Renato Negra, Fadhel Ghannouchi, University of Calgary | |
| 10:10 | A Sigma-Delta Fractional- N Synthesizer for GSM Standard Specifications..... | 1121 |
| | Hassene Mnif, Mourad Fakhfakh, Ibtihel Krout, M. Barhoumi, National Engineering School of Sfax; Mourad Loulou, University of Sfax | |
| 10:30 | A Programmable Complex FIR Filter with Integrated MEMS Filter for Front-End Charge Sampling Receiver..... | 1125 |
| | James Wei, Dominique Morche, CEA/LETI; Serge Ramet, STMicroelectronics; Jacques Verdier, INSA de Lyon | |

C2L-E PHOTONIC & OPTOELECTRONIC CIRCUITS
Time: Wednesday, December 13, 2006, 09:30 - 10:50
Place: Gallieni A
Chair: Edoardo Charbon; *EPFL, Lausanne, Switzerland*

| | | |
|-------------|---|-------------|
| 9:30 | Direct Form I Active Optical Filters Realized in an Integrated Photonic Architecture | 1129 |
| | Duncan Macfarlane, Jian Tong, Robert Hunt, Issa Panahi, Kent Wade, University of Texas at Dallas; Gary Evans, Marc Christensen, Southern Methodist University | |
| 9:50 | A 100dB Dynamic Range CMOS Image Sensor with Global Shutter | 1133 |
| | Estelle Labonne, Gilles Sicard, Marc Renaudin, TIMA Laboratory; Pierre-Damien Berger, ATMEL Grenoble | |

10:10 A 1Gb/s 4-Channel Optical Transceiver Chipset for Automotive Wired Networks 1137
Jae Kwan Kwon, Yonsei University; Wonseok Oh, Jongchan Choi, Korea Electronics
Technology Institute; J. -W. Han, B. -Y. Choi, Sung Min Park, Ewha Womans University

10:30 High-Performance Pixelwise Readout Integrated Circuits for Microbolometer 1140
Chi Ho Hwang, Yong Soo Lee, Hee Chul Lee, Korea Advanced Institute of Science and
Technology

C2L-F SENSORS I

Time: Wednesday, December 13, 2006, 09:30 - 10:50

Place: Gallieni B

Chair: Joseph Micallef; *University of Malta, Malta*

9:30 Low-Power 2.4-GHz RF Transceiver for Wireless EEG Module Plug-and-Play 1144
Joao Paulo Carmo, Polytechnic Institute of Braganca; Nuno Dias, Paulo Mateus
Mendes, Carlos Couto, Jose Higino Correia, University of Minho

**9:50 A New PhotoFET for Monolithic Active Pixel Sensors Using CMOS Submicronic
Technology 1148**
Sébastien Heini, Christine Hu-Guo, Marc Winter, Yann Hu, Institut Pluridisciplinaire
Hubert Curien

**10:30 A Comparison Between Centerized and Distributed Agent-Based Evolutionary
Target Tracking System 1152**
Yaser Khalifa, State University of New York; Ehi Okoene, SUNY; Basel Al Murad, Aston
University

C3L-A ANALOG BUILDING BLOCKS III

Time: Wednesday, December 13, 2006, 11:10 - 12:30

Place: Auditorium

Chair: Erik Bruun; *Technical University of Denmark, Denmark*

11:10 A Novel Bootstrapped Switch Design, Applied in a 400 MHz Clocked DS ADC 1156
Koen Cornelissens, K.U.Leuven; Michiel Steyaert, Katholieke Universiteit Leuven

**11:30 Investigation of Timing Jitter in NAND and NOR Gates Induced by Power-Supply
Noise 1160**
Adam Strak, Hannu Tenhunen, KTH - Royal Institute of Technology

**11:50 Track-and-Latch Comparator Design Using Associations of MOS Transistors and
Characterization 1164**
Fernando Paixao Cortes, Alessandro Girardi, Universidade Federal do Rio Grande do
Sul; Sergio Bampi, UFRGS

12:10 A Wide-Range Delay-Locked Loop with a New Lock-Detect Circuit 1168
Amir Ghaffari, Adib Abrishamifar, Iran University of Science and Technology

| | | |
|--------------|--|-------------|
| C3L-B | DIGITAL MODELING | |
| Time: | Wednesday, December 13, 2006, 11:10 - 12:30 | |
| Place: | Gallieni I | |
| Chair: | Fabrice Monteiro; <i>LICM, Metz, France</i> | |
| 11:10 | Power Macromodeling for IP Modules | 1172 |
| | Yaseer A. Durrani, Teresa Riesgo, Universidad Politécnica de Madrid | |
| 11:30 | Acceleration for a Compiled Transaction Level Modeling Simulation..... | 1176 |
| | Mathieu Dubois, El Mostapha Aboulhamid, Université de Montréal; Frédéric Rousseau, Laboratoire TIMA | |
| 11:50 | Temporal and System Level Modifications for High Speed VLSI Implementations of Cryptographic Core | 1180 |
| | George Panagiotakopoulos, Vasilis Thanasoulis, Harris Michail, Athanasios Kakarountas, Costas Goutis, University of Patras | |
| 12:10 | Pole Optimisation of GOB-Volterra Model for Non Linear MISO System | 1184 |
| | Safa Chouchane, Hassani Messaoud, Ecole Nationale d'Ingénieurs de monastir | |

| | | |
|--------------|---|-------------|
| C3L-C | MEMORY | |
| Time: | Wednesday, December 13, 2006, 11:10 - 12:30 | |
| Place: | Gallieni II | |
| 11:10 | Address Generation Techniques for Conflict Free Parallel Memory Accessing in FFT Architectures | 1188 |
| | Dionysios Reisis, Nikolaos Vlassopoulos, National and Kapodistrian University of Athens | |
| 11:30 | Cell Ratio Bounds for Reliable SRAM Operation | 1192 |
| | Qiaoyan Yu, Paul Ampadu, University of Rochester | |
| 11:50 | Leakage Energy Reduction in Banked Content Addressable Memories | 1196 |
| | Pedro Echeverria, Jose Ayala, Marisa Lopez-Vallejo, Universidad Politecnica de Madrid | |
| 12:10 | Switched Polarity Charge Pump for NOR-Type Flash Memories | 1200 |
| | Mohammad Mohammad, Jalal Fahmi, Omar Terkawi, Kuwait University | |

| | | |
|--------------|--|-------------|
| C3L-D | RF SYSTEMS | |
| Time: | Wednesday, December 13, 2006, 11:10 - 12:30 | |
| Place: | Gallieni III | |
| Chair: | Marc Belleville; <i>CEA LETI, Grenoble, France</i> | |
| 11:10 | An RF-ID Receiver Using SAW Filters for Wideband Synchronisation | 1204 |
| | Thomas McCoy, Paul Brennan, Richard Bullock, UCL | |
| 11:30 | A Fully Integrated 2.45-GHz Frequency Synthesizer and FSK Modulator | 1208 |
| | Vincent Cheynet de Beaupré, L2MP - Université de Provence; Lakhdar Zaïd, Wenceslas Rahajandraibe, L2MP; Gilles Bas, STMicroelectronics | |

11:50 A New Simple UWB Monocycle Pulse Generator 1212
Yvan Duroc, Tan-Phu Vuong, INPG/ESISAR; Jose Ewerton Pombo de Farias,
Glauco Fontgalland, UFCG/CEII/DEE; Alexandre Serres, INPG/ESISAR

12:10 A Low-Power High-Rate Modulator for Ultra-Wideband Transmitters 1216
Mehdi Salehi, Malek Ashtar University of Technology; Abdolreza Nabavi, Tarbiat
Modarres University; Nader Ghadimi, Malek Ashtar University of Technology

C3L-E PROCESSORS & CONTROLLERS

Time: Wednesday, December 13, 2006, 11:10 - 12:30

Place: Gallieni A

Chair: Makoto Ikeda; *University of Tokyo, Japan*

**11:10 A Pre-Processing Based Real-Time Address Tracer for Embedded
Microprocessors 1220**
Yuan-Long Jeang, Tzue-Shuang Wey, Kun Shan University; Hung-Yu Wang, Ching-Ta
Chen, National Kaohsiung University of Applied Sciences

11:30 Efficient Post-Processing Module for a Chaos-Based Random Bit Generator 1224
Tommaso Addabbo, Massimo Alioto, Ada Fort, Santina Rocchi, Valerio Vignoli,
University of Siena

**11:50 Hardware-Software Co-design of a Dynamically Reconfigurable FPGA-based
Fuzzy Logic Controller 1228**
Francisco Fons, Mariano Fons, Enrique Canto, Rovira i Virgili University

**12:10 A Programmable Hardware Cellular Automaton : Example of Data Flow
Transformation 1232**
Samuel Charbouillot, Annie Perez, Daniele Fronte, L2MP

C3L-F SENSORS II

Time: Wednesday, December 13, 2006, 11:10 - 12:30

Place: Gallieni B

Chair: Herve Barthelemy; *L2MP, Marseille, France*

**11:10 A Novel Architecture for Remote Interrogation of Wireless Battery-Free Capacitive
Sensors 1236**
Michel Nowak, Nicolas Delorme, CEA-LETI; Gilles Jacquemod, LEAT; François Conseil,
MBDA

**11:30 A New Polysilicon TFT Capacitive Fingerprint Sensor with Advanced Mismatch
Compensation 1240**
Cedric Rechatin, Patrick Audebert, CEA/LETI; Nacer Abouchi, Jean-Marc Galvan,
CPE/Lyon

11:50 A Hardware Library for Sensors/Actuators Interfaces in Sensor Networks 1244
Jorge Portilla, Jose Luis Buron, Universidad Politecnica de Madrid; Angel de Castro,
Universidad Autonoma de Madrid; Teresa Riesgo, Universidad Politecnica de Madrid

12:10 **MAC Protocol for Low-Power Real-Time Wireless Sensing and Actuation** 1248
Jose Afonso, Luis Rocha, Helder Silva, Jose Higino Correia, University of Minho

C4L-A ANALOG BUILDING BLOCKS II

Time: Wednesday, December 13, 2006, 14:00 - 15:40

Place: Auditorium

Chair: Mourad Loulou; *ENIS, Sfax, Tunisia*

14:00 **On Stability of Synchronized Van der Pol Oscillators**..... 1252
Igor Filanovsky, University of Alberta; Chris Verhoeven, TU Delft

14:20 **A 900 MHz Multiphase LC Oscillator with Sinusoidal Outputs in SiGe Technology** 1256
Raúl Regidor, Roberto Esper-Chaín, Félix Tobajas, Octavio Santana, Roberto Sarmiento, Research Institute for Applied Microelectronics (IUMA)

14:40 **Detailed Solution Curves and Bifurcation Boundaries of the Forced Van der Pol Oscillator**..... 1260
Jordi Bonet-Dalmau, Pere Palà-Schönwälder, UPC-Technical University of Catalonia

15:00 **Application of the Inductor Multiplier** 1264
Takeshi Shima, Kanagawa University

15:20 **An Optimized Low Voltage and High Frequency CCII Based Multifunction Filters**..... 1268
Samir Bensalem, Dorra Sellami Masmoudi, Mourad Loulou, Ashwek Ben Saïd, University of Sfax

C4L-B DIGITAL CIRCUITS & SYSTEMS

Time: Wednesday, December 13, 2006, 14:00 - 15:40

Place: Gallieni I

Chair: Ricardo Reis; *UFRGS, Porto Alegre, Brazil*

14:00 **A UML-Based Environnement for System Design Space Exploration**..... 1272
Ludovic Aprville, GET / ENST; Waseem Muhammad, Rabéa Ameer-Boulifa, Sophie Coudert, Renaud Pacalet, ENST

14:20 **An Efficient FPGA Implementation of Gaussian Mixture Models-Based Classifier Using Distributed Arithmetic** 1276
Minghua Shi, Hong Kong University of Science and Technology; Shrutisagar Chandrasekaran, Brunel University, West London; Amine Bermak, Hong Kong University of Science and Technology; Abbes Amira, Brunel University, West London

14:40 **Wave Pipelining Using Self Reset Logic**..... 1280
Miguel Litvin, Samiha Mourad, Santa Clara University

15:00 **A NAND Flash Memory Controller for SD/MMC Flash Memory Card** 1284
Chuan-Sheng Lin, Kuang-Yuan Chen, Yu-Hsian Wang, Prolific Technology; Lan-Rong Dung, National Chiao Tung University

| | | |
|--------------|--|-------------|
| 15:20 | An Efficient Hardware Implementation of a Robust and Low-Complexity ADSRC Timing Synchronization Design | 1288 |
| | Huynh Trong Anh, Jinsang Kim, Won-Kyung Cho, Kyung Hee University; Jongchan Choi, Korea Electronics Technology Institute | |

C4L-C LOW-POWER, LOW-VOLTAGE CIRCUITS

Time: Wednesday, December 13, 2006, 14:00 - 15:40

Place: Gallieni II

Chair: Thierry Taris; *IXL Lab, Bordeaux, France*

| | | |
|--------------|--|-------------|
| 14:00 | A Low Power Sense Amplifier Flip-Flop with Balanced Rise/Fall Delay | 1292 |
| | Rubil Ahmadi, ATI technologies Inc. | |

| | | |
|--------------|---|-------------|
| 14:20 | Influence of Refresh Circuits Connected to Low Power Digital Quasi-Floating Gate Designs | 1296 |
| | Jon Alfredsson, Bengt Oelmann, Mid Sweden University | |

| | | |
|--------------|--|-------------|
| 14:40 | Precharge Node Based Variable Forward Body Bias for Low-Energy LSIs | 1300 |
| | Senthilkumar Jayapal, University of Freiburg - IMTEK; Yiannos Manoli, IMTEK | |

| | | |
|--------------|--|-------------|
| 15:00 | Design of a Flexible Low-Power Modem Chip for Point to Point Radio Link Cellular Backhaul Applications..... | 1304 |
| | Stefano Chinnici, Carmelo Decanis, Ericsson Lab Italy S.p.A. | |

| | | |
|--------------|---|-------------|
| 15:20 | A Design Methodology for High-Speed Low-Power MCML Frequency Dividers | 1308 |
| | Massimo Alioto, University of Siena; Rosario Mita, Gaetano Palumbo, University of Catania | |

C4L-D RF RECEIVER & TRANSMITTER ARCHITECTURES

Time: Wednesday, December 13, 2006, 14:00 - 15:40

Place: Gallieni III

Chair: Yann Deval; *IXL Lab, Bordeaux, France*

| | | |
|--------------|--|-------------|
| 14:00 | Low-Power RF Transceiver for IEEE 802.15.4 (Zigbee) Standard Applications | 1312 |
| | Domenico Zito, Domenico Pepe, Bruno Neri, University of Pisa | |

| | | |
|--------------|---|-------------|
| 14:20 | Wide-Band 0.9 GHz to 4 GHz Four-Port Receiver | 1316 |
| | Haddadi Kamel, Institut d'Electronique, de Microélectronique et Nanotechnologies; Lasri Tuami, Glay David, El Aabbaoui Hassan, Loyez Christophe, Rolland Nathalie, IEMN | |

| | | |
|--------------|--|-------------|
| 14:40 | Automated Design of a WCDMA/WLAN Multi-Standard Receiver | 1320 |
| | Delia Rodríguezellera González, Royal Institute of Technology; Ana Rusu, Royal Institute of Technology Stockholm; Mohammed Ismail, KTH | |

| | | |
|--------------|--|-------------|
| 15:00 | Optimized AIS/DSC Homodyne Receiver Design..... | 1324 |
| | Rim Barrak, Mounira Msehli, Adel Ghazel, SUP'COM; Ammar Kouki, Ecole Supérieure des Technologies | |

15:20 A 3.1 - 10.6 GHz CMOS Direct-Conversion Receiver for UWB Applications 1328
Chung-Yu Wu, NCTU; Yi-Kai Lo, Min-Chiao Chen, Nanoelectronics and Giga-scale
Systems Laboratory

C4L-E NEURAL NETWORKS

Time: Wednesday, December 13, 2006, 14:00 - 15:40

Place: Gallieni A

Chair: Adrijan Baric; *University of Zagreb, Croatia*

14:00 Robust Symmetric Multiplication for Programmable Analog VLSI Array Processing 1332
Carlos Manuel Domínguez Matas, Ricardo Carmona Galán, Francisco Javier Sánchez
Fernández, Ángel Rodríguez Vázquez, Instituto de Microelectrónica de Sevilla-CNM-
CSIC

**14:20 Finding the Number of Clusters in a Dataset Using an Information Theoretic
Hierarchical Algorithm..... 1336**
Mehdi Aghagolzadeh, Hamid Soltanian-Zadeh, Babak Araabi, University of Tehran; Ali
Aghagolzadeh, University of Tabriz

14:40 Artificial Neural Network Optimization for FPGA 1340
Mark Bonnici, Edward Gatt, Joseph Micallef, Ivan Grech, University of Malta

15:00 Simple Analogue VLSI Circuit of a Cortical Neuron 1344
Jayawan Wijekoon, Piotr Dudek, University of Manchester

15:20 Modelling the XOR/XNOR Boolean Functions Complexity Using Neural Network..... 1348
P. W. C. Prasad, Multimedia University; Ashutosh Kumar Singh, University Tun Abdul
Razak; Azam Beg, Ali Assi, United Arab Emirates University

C4L-F SYSTEM INTEGRATION

Time: Wednesday, December 13, 2006, 14:00 - 15:40

Place: Gallieni B

Chair: Francesco Svelto; *University of Pavia, Italy*

14:00 Scalable Model for Multistandard Phase Locked Loop..... 1352
Benjamin Nicolle, Mentor Graphics / Laboratoire d'Electronique Antennes &
Télécommunications; William Tatinian, LEAT; Jean Oudinot, Mentor Graphics; Gilles
Jacquemod, LEAT

14:20 Noise and Jitter in CMOS Digitally Controlled Delay Lines 1356
Monica Figueiredo, Instituto Politecnico de Leiria; Rui Aguiar, Universidade de Aveiro

14:40 Frequency-Path Modeling for Three-Longitudinal-Mode Interferometer 1360
Saeed Olyaei, Shahram Mohammad Nejad, Iran University of Science and Technology

15:00 Area-Driven White Space Distribution for Detailed Floorplan Design 1364
Jin-Tai Yan, Zhi-Wei Chen, Ming-Yuen Wu, Chung-Hua University

15:20 **Dynamic Element Matching for Low-Power Sigma-Delta Modulator with R-C Based Internal DAC** **1368**
Cristina Della Fiore, Franco Maloberti, University of Pavia; Miguel Garcia, Instituto Nacional de Astrofisica Optica y Electronica