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S. Hurtt, A. G. Dentai, J. L. Pleumeekers, A. Mathur, R. Muthiah, C. Joyner, R. P. Schneider, R. Nagarajan, F. A. Kish, and D. F. Welch, Infinera Corporation, Sunnyvale, California, USA
- V.A-2 **A hybrid silicon evanescent photodetector**
H. Park¹, A. W. Fang¹, R. Jones², O. Cohen³, O. Radaý³, M. N. Sysak¹, M. J. Paniccia², and J. E. Bowers¹, ¹University of California Santa Barbara, ECE Department, Santa Barbara, California, USA, ²Intel Corporation, Santa Clara, California, USA and ³Intel Corporation, Jerusalem, ISRAEL
- V.A-3 **High-Frequency Performance of a High-Power Traveling Wave Photodetector with Parallel Optical Feed**
A. Beling¹, H.-G. Bach², G. G. Mekonnen², R. Kunkel², D. Schmidt² and J. C. Campbell¹, ¹Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, Virginia, USA, and ²Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institut, Berlin, GERMANY
- V.A-4 **Single Ultra Violet Photon Detection with 4H-SiC Avalanche Photodiodes**
X. Bai, D. McIntosh, H. Liu, J. Campbell, Electrical and Computer Engineering, University of Virginia, Charlottesville, Virginia, USA
- V.A-5 **The challenges and opportunities for dilute nitride antimonides in photonic devices**
Jim Harris , Stanford University Jim Harris , Stanford University, Stanford, California, USA
- V.A-6 **1.65 μm buffer-free GaSb/AlGaSb quantum-well diode lasers grown on a GaAs substrate operating at room temperature**
M. Mehta, G. Balakrishnan, A. Jallapali, M. N. Kutty, L. R. Dawson, and D. L. Huffaker, Center for High Technology Materials, University of New Mexico, Albuquerque, New Mexico, USA
- V.A-7 **High Temperature CW Operation of Interband Cascade Lasers at $\sim 4.0 \mu\text{m}$**
C. S. Kim, M. Kim, W. W. Bewley, C. L. Canedy, D. C. Larrabee, J. A. Nolde, J. R. Lindle, I. Vurgaftman, and J. R. Meyer, Naval Research Laboratory, Washington District of Columbia, USA
- V.A-8 **Strain-Compensated AlAs-InGaAs Quantum-Cascade Lasers with Emission Wavelength 3–5 μm**
M.P. Semtsiy¹, S. Dressler¹, M. Wienold¹, I. Bayrakli¹, M. Ziegler², K. Kennedy³, R. Hogg³, and W.T. Masselink¹, ¹Humboldt University, Berlin, Germany, ²Max-Born-Institut, Berlin, Germany, and ³University of Sheffield, Sheffield, UK

- V.B-1 **InGaAs CMOS: a “Beyond-the-Roadmap” Logic Technology?**
J. A. del Alamo and D. H. Kim, Massachusetts Institute of Technology, Cambridge, Massachusetts, USA
- V.B-2 **InGaAs and GaAs/InGaAs Channel Enhancement Mode n-MOSFETs With HfO₂ Gate Oxide and a-Si Interface Passivation Layer**
S. Oktyabrsky¹, S. Kovesnikov², V. Tokranov¹, M.I Yakimov¹, R. Kambhampati¹, H. Bakhru¹, F. Zhu², J. Lee³, and W. Tsai², ¹College of Nanoscale Science and Engineering, University at Albany-SUNY, New York, USA, ²Intel Corporation, Santa Clara, California, USA, and ³The University of Texas at Austin, Department of Electrical and Computer Engineering, Austin, Texas, USA
- V.B-3 **Enhancement Mode n-MOSFET with High- κ Dielectric On GaAs Substrate**
K. Rajagopalan², P. Zurcher², J. Abrokwah², R. Droopad², D. A. J. Moran¹, R. J. W. Hill¹, X. Li¹, H. Zhou¹, D. McIntyre¹, S. Thoms¹, I.G. Thayne¹ and M. Passlack², ¹Department of Electronics & Electrical Engineering, University of Glasgow, Glasgow, UK and ²Freescale Semiconductor Inc., Tempe, Arizona, USA

- V.B-4 **High-performance submicron inversion-type enhancement-mode InGaAs MOSFET with maximum drain current of 360 mA/mm and transconductance of 130 mS/mm**
Y. Xuan, Y. Q. Wu, H. C. Lin, T. Shen and P. D. Ye, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA
- V.B-5 **Enhancement-mode In_{0.70}Ga_{0.30}As-channel MOSFETs with ALD Al₂O₃**
Y. Sun, E. W. Kiewra, J. P. De Souza, S. J. Koester, K. E. Fogel, D. K. Sadana, IBM Thomas J. Watson Research Center, Yorktown Heights, New York, USA
- V.B-6 **Performance of Sub-micron Gate Length InAlP Native Oxide GaAs-channel MOSFETs**
J. Zhang, T. H. Kosel, D. C. Hall, and P. Fay, Dept. of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

Session V.C Memory Devices

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- V.C-1 **Hybrid ALD-SiN/Si-nanocrystals/ALD-SiN FinFET device with large P/E window for MLC NAND Flash memory application**
J.-D. Choe¹, S.-H. Lee², Y. J. Ahn², D. Jang², Y.-B. Yoon², J. J. Lee², I. Chung¹, K. Park² and D. Park²,
¹School of Information and Communication Engineering, Sungkyunkwan University, Kyungki-Do, KOREA and ²Technology Development Team 2, Samsung Electronics Co., Yongin-City, Kyungki-Do, KOREA
- V.C-2 **Ge/Si hetero-nanocrystal nonvolatile floating gate memory**
B. Li, Y. Zhu and J. Liu, Quantum Structures Laboratory, Department of Electrical Engineering, University of California, Riverside, California, USA
- V.C-3 **Memory Effects in Metal-Oxide-Semiconductor Capacitors Incorporating Dispersed Highly Mono-disperse One-Nanometer Silicon Nanoparticles**
O. M. Nayfeh¹, D. A. Antoniadis¹, K. Mantey² and M. H. Nayfeh², ¹Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, Massachusetts and ²Department of Physics, University of Illinois at Urbana-Champaign, Urbana, Illinois, USA
- V.C-4 **Modeling of Multi-layer Nanocrystal Memory**
T.-H. Hou, C. Lee, and E. C. Kan, School of Electrical and Computer Engineering, Cornell University, Ithaca, New York, USA
- V.C-6 **Phase-change Memory**
C. Lam, IBM Qimonda Macronix PCRAM Joint Project, IBM T.J. Watson Research Center, Yorktown Heights, New York, USA
- V.C-7 **Novel Cross Point Switch based on Zn_{1-x}Cd_xS memory devices for FPGA**
K. Abe¹, Z. Wang², S. Fujita¹, T. H. Lee² and Y. Nishi², ¹Frontier Research Laboratory, Corporate R&D Center, Toshiba Corporation, JAPAN, and ²Center for Integrated Systems, Stanford University, Stanford, California, USA

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- R.1 **The Future of Nanowire Devices: Top-down or bottom-up?**
Session Organizers: Prabhat Agarwal, NXP, Steven Koester, IBM, and Eric Pop, Univ. Illinois/Urbana Champaign
- R.2 **Why do we need nano for biosensors?**
Session Organizers: Sang-Hyun Oh, University of Minnesota and Janos Voros, ETH Zurich
- R.3 **The THz Bridge**
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Low Cost "Plastic" Solar Cells: A Dream or Reality???

Alan J. Heeger, University of California, Santa Barbara

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- VI.A-1 **The brain and the computer**
K. Boahen, Stanford University, Bioengineering Dept., Stanford, California, USA
- VI.A-2 **Joining Microelectronics and Microionics: Nerve Cells and Brain Tissue on Semiconductor Chips**
P. Fromherz, Department of Membrane and Neurophysics, Max Planck Institute for Biochemistry, Munich, GERMANY
- VI.A-3 **Biolithography: DNA-assisted Manufacturing of Nanodevices for Optical and Electronic Biosensing**
J. Vörös, Laboratory of Biosensors and Bioelectronics, Institute for Biomedical Engineering, Zurich, SWITZERLAND

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- VII.A-1 **Recent Advances in MRAM Technology**
J. M. Slaughter, Freescale Semiconductor, Inc., Chandler, Arizona, USA
- VII.A-2 **Magnetic Sensitivity in Mesoscopic EMR Devices in I-V-I-V Configuration**
T. Boone, L. Folks, J. A. Katine, E. Marinero, N. Smith and B. A. Gurney, Hitachi Global Storage Technologies, San Jose Research Center, San Jose, California, USA
- VII.A-3 **Simulation of Spin Torque Devices with Inelastic Spin flip Scattering**
S. Salahuddin and S. Datta, School of Electrical and Computer Engineering and NSF Network for Computational Nanotechnology, Purdue University, West Lafayette, Indiana, USA
- VII.A-5 **Characterization and Application of Large Magnetoresistance in Organic Semiconductors**
M. Wohlgenannt, G. Veeraraghavan, Y. Sheng, O. Mermer, and T. D. Nguyen, Department of Physics and Astronomy, The University of Iowa, Iowa City, Iowa, USA
- VII.A-6 **Metamaterials - Negative Indices with Positive Benefits?**
M. C. K. Wiltshire, Imaging Sciences Department, Imperial College London, London, UK
- VII.A-7 **High Performance Polycrystalline Diamond Micro Resonators**
N. Sepúlveda¹, J. Lu¹, D. M. Aslam¹, and J. P. Sullivan², ¹Electrical and Computer Engineering, Michigan State University, E. Lansing, Michigan, USA and ²Sandia National Laboratories, Albuquerque, New Mexico, USA

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- VII.B-1 **Aligned Arrays Single Walled Carbon Nanotubes for Thin Film Electronics**
J. A. Rogers, University of Illinois at Urbana/Champaign, Urbana, Illinois, USA
- VII.B-2 **Quantum Capacitance Measurement for SWNT FET with Thin ALD High-k Dielectric**
Y. Lu¹, H. Dai¹ and Y. Nishi², ¹Department of Chemistry and Laboratory for Advanced Materials, Stanford University, Stanford, California, USA and ²Electrical Engineering, Stanford University, Stanford, California, USA

- VII.B-3 **The study of low frequency noise of single-walled carbon nanotube transistors**
S. Kim, D. Chang, Y. Xuan, P. Ye and S. Mohammadi, School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA
- VII.B-4 **Semiconducting Graphene Ribbon Transistor**
Z. Chen, P. Avouris, IBM T. J. Watson Research Center, Yorktown Heights, New York, USA
- VII.B-5 **Performance Limits of Nanocomposite Transistors & Nanobio Sensors: A Bottom-up Perspective**
M. A. Alam, N. Pimparkar, P. Nair, S. Kumar, and J. Murthy, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA
- VII.B-6 **Impact of Process Variation on Nanowire and Nanotube Device Performance**
B. C. Paul^{1,2}, S. Fujita², M. Okajima², T. Lee¹, H.S.P. Wong¹, and Y. Nishi¹, ¹Center for Integrated Systems, Stanford University, Stanford, California, USA and ²Toshiba America Research Inc., San Jose, California, USA
- VII.B-7 **Scaling Behaviors of Graphene Nanoribbon FETs**
Y. Yoon, Y. Ouyang, and J. Guo, Electrical and Computer Engineering, University of Florida, Gainesville, Florida, USA
- VII.B-7 **Role of Electrical and Thermal Contact Resistance in the High-Bias Joule Breakdown of Single-Wall Carbon Nanotube Devices**
E. Pop, Dept. of Electrical and Computer Engineering and Micro and Nanotechnology Lab, University of Illinois, Urbana-Champaign, Urbana, Illinois, USA