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Session 6 – Advances in Programmable Devices

Oak Ballroom, Monday Afternoon, September 17
Chair: Raj Amirtharajah
Co-Chair: Steve Wilton

Programmable devices are everywhere: from consumer products to high-security applications. This session highlights novel architectures, new CAD techniques, and innovative technologies that make these systems possible.

1:30 pm
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3:15 pm - BREAK

Session 7 – Emerging Wireless Applications

Fir Ballroom, Monday Afternoon, September 17
Chair : Stefan Drude
Co-Chair : Earl McCune

Progress in achieving high levels of integration is presented for single chip solutions in satellite TV, WiMax-WiBRO, GPS, and RFID applications, using a variety of process technologies.

1:30 pm
Introduction

7.1 - 1:35 pm 97
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3:15 pm - BREAK

Session 8 – Microsystems for BioMedical Applications

Pine Ballroom, Monday Afternoon, September 17
Chair: Dawn Fitzgerald
Co-Chair : Sudhir Aggarwal

A tutorial on the acquisition of biopotentials is presented followed by three papers on emerging microsystems for biomedical applications. These include circuit innovations in MRI, hearing aid and tactile imaging.

1:30 pm
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8.1 - 1:35 pm 115
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3:15 pm - BREAK

Session 9 – Test, Characterization, and Jitter of High-Speed Serial I/O and Clocks

Cedar Ballroom, Monday Afternoon, September 17
Chair: Jeanne Trinko Mechler
Co-Chair : Gordon Roberts

Characterization, test and jitter measurements are reaching picosecond resolution for high speed serial links and clock networks.

1:30 pm
Introduction

Session 10 – Panel Discussion

Oak Ballroom, Monday Afternoon, September 17
4:00 pm - 5:30 pm

Are Analog Designers Hopeless At Scaling?
Will Digital Designers Eat Their Lunch At 45nm And Below?

Session 11 – Biomedical Sensors

Pine Ballroom, Monday Afternoon, September 17
Chair: Jackie Snyder
Co-Chair : Ken Szajda

This session presents innovative uses of integrated circuits for biomedical applications.

Poster Session

Cascade Ballroom, Monday, September 17
3:30 pm – 8:00 pm
(Authors are at the posters from 5:30 pm – 7:00 pm)

Session 12 – Nyquist A/D Converters

Oak Ballroom, Tuesday Morning, September 18
Chair: George La Rue
Co-Chair : Yusuf Haque

The first four papers present pipelined A/D converters with resolution of 10 to 14 bits and conversion rates below 210 MS/s. These are followed by higher conversion rate circuits up to 4 GS/s.

8:25 am
Introduction

10:10 am - BREAK

Session 13 – Clocking and CDRs

Fir Ballroom, Tuesday Morning, September 18
Chair : Jafar Savoj
Co-Chair: Kimo Tam

This session explores modern clocking techniques with an emphasis on digital enhancement along with new CDR implementations.

8:25 am
Introduction

10:10 am - BREAK

Session 14 – Power Management Techniques

Pine Ballroom, Tuesday Morning, September 18
Chair: Steve Garverick
Co-Chair: Makoto Takamiya

This session addresses issues in power management, including ac-dc and dc-dc converters, regulators, controllers, timers, and low-power drivers.

8:25 am
Introduction

10:10 am - BREAK

Session 15 – CMOS Scaling and Technology Implications

Cedar Ballroom, Tuesday Morning, September 18
Chair: David Sunderland
Co-Chair: Jordan Lai

This session of invited papers addresses important issues related to maintaining Moore's Law scaling beyond 45nm, focusing on device technology, package technology, reliability and physical analysis.

8:25 am
Introduction

15.3 - 9:45 am **417**
High-K/Metal Gate Technology: A New Horizon (INVITED PAPER), *M. Khare, IBM*

10:10 am - BREAK

15.4 - 10:25 am **421**
Revolutionary NanoSilicon Ancillary Technologies for Ultimate-Performance Gigascale Systems (INVITED PAPER), *M. Bakir, B. Dang and J. Meindl, Georgia Institute of Technology*

15.5 - 11:15 am **429**
Reverse Engineering in the Semiconductor Industry (INVITED PAPER), *R. Torrance and D. James, Chipworks, Inc.*

Session 16 – Signal and Data Processing

Oak Ballroom, Tuesday Afternoon, September 18
Chair: Charles Thomas
Co-Chair: Ram Krishnamurthy

This session explores new signal and data processing integrated circuits for a diverse reange of applications including medical devices, video processing and high speed communications.

2:00 pm
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16.1 - 2:05 pm **437**
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16.2 - 2:55 pm **443**
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16.3 - 3:20 pm **447**
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3:45 pm - BREAK

16.4 - 4:00 pm **451**
A 0.25µm 0.92mW per Mb/s Viterbi Decoder Featuring Resonant Clocking for Ultra-Low-Power 54Mb/s WLAN Communication, *F. Carbognani, S. Haene, M. Arrigo, C. Pagnamenta, F. Buergin, N. Felber, H. Kaeslin and W. Fichtner, ETH Zurich*

16.5 - 4:25 pm **455**
A High-Throughput Maximum a posteriori Probability Detector, *R. Ratnayake, G.-Y. Wei, Harvard University, A. Kavcic, University of Hawaii*

16.6 - 4:50 pm **459**
A 3.3-Gbps Bit-Serial Block-Interlaced Min-Sum LDPC Decoder in 0.13µm CMOS, *A. Darabiha, A. Chan Carusone and F. Kschischang, University of Toronto*

Session 17 – Wideband Techniques

Fir Ballroom, Tuesday Afternoon, September 18

Chair: Tony Chan Carusone
Co-Chair: Ed Van Tuijl

This session focuses on the design of high-speed wireline circuits for data connectivity up to 100 Gb/s. Novel architectures and methodologies are presented.

2:00 pm
Introduction

17.1 - 2:05 pm **463**
A Heterodyne Phase Locked Loop with GHz Acquisition Range for Coherent Locking of Semiconductor Lasers in 0.13µm CMOS, *F. Aflatouni, O. Momeni and H. Hashemi, USC*

17.2 - 2:30 pm **467**
A Synthesis-based Bandwidth Enhancing Technique for CML Buffers/Amplifiers, *D. Pi, B.-K. Chun and P. Heydari, University of California*

17.3 - 2:55 pm **471**
Towards a sub-2.5V, 100-Gb/s Serial Transceiver (INVITED PAPER), *S. Voinigescu, R. Aroca, S. Nicolson, T. Chalvatzis, University of Toronto, P. Chevalier, P. Garcia, C. Garnier and B. Sautreuil, STMicroelectronics, T. Dickson, IBM*

3:45 pm - BREAK

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17.5 - 4:50 pm **487**
Time-Variant Characterization and Compensation of Wideband Circuits, *A. Amirkhany, M. Horowitz, Stanford University, A. Abbasfar, J. Savoj, Rambus, Inc.*

17.6 - 5:15 pm **491**
High-Voltage-Tolerant I/O Circuit Design for USB 2.0-Compliant Applications, *M.-J. Kim, T.H. Lee, Stanford University, H. Icking, H. Gossner, Infineon Technology*

Session 18 – Compact Modeling for Analog and RF

Pine Ballroom, Tuesday Afternoon, September 18
Chair: Rob Jones
Co-Chair: Hong-Ha Vuong

This session presents advanced compact models and modeling/synthesis approaches to address analog and RF applications.

2:00 pm
Introduction

18.1 - 2:05 pm **495**
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Mismatch Characterization of Ring Oscillators, *A. Balankutty, T.-C. Chih, C.-Y. Chen and P. Kinget, Columbia University*

18.6 - 4:50 pm **519**
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Session 19 – Front-Ends and Synthesizers for Communication Applications

Cedar Ballroom, Tuesday Afternoon, September 18

Chair: Ranjit Gharpurey
Co-Chair: Rick Carley

This session begins with presentations on four receiver front ends, covers two frequency synthesizers, and finishes with a high efficiency CMOS cellular power amplifier.

2:00 pm
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19.1 - 2:05 pm **527**
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19.3 - 2:55 pm **535**
A Current-Equalized Distributed Receiver Front-End for UWB Direct Conversion Receivers, *A. Safarian, L. Zhou and P. Heydari, University of California Irvine*

19.4 - 3:20 pm **539**
A 65μW, 1.9 GHz RF to Digital Baseband Wakeup Receiver for Wireless Sensor Nodes, *N. Pletcher, S. Gambini and J. Rabaey, University of California, Berkeley*

3:45 pm - BREAK

19.5 - 4:00 pm **543**
A 4GHz Low Complexity ADPLL-based Frequency Synthesizer in 90nm CMOS, *J. Zhuang, Q. Du and T. Kwasniewski, Carelton University*

19.6 - 4:25 pm **547**
A 4.2 GHz PLL Frequency Synthesizer with an Adaptively Tuned Coarse Loop, *T. Wu, Rambus Inc., P. Hanumolu, K. Mayaram and U.-K. Moon, Oregon State University*

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Cascade Ballroom, Tuesday Afternoon, September 18
5:30 pm – 7:30 pm
(Authors are at the posters from 5:30 pm – 7:00 pm)

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A 2.4GHz Efficiency-Enhanced Rectifier for Wireless Telemetry, *K.-H. Chen, J.-H. Lu and S.-I. Liu, National Taiwan University*

TP-02 **559**
Comparative Studies of Common Control Schemes for ReferenceTtracking and Application of End-point Prediction, *Y. Wu and P. K. T. Mok, Hong Kong University of Science and Technology*

TP-03 **563**
An Energy Management Circuit for Self-Powered Ubiquitous Sensor Modules, *J. Pan and Y. Inoue, Waseda University*

TP-04 **567**
An Ultra-Low-Power Power Management IC for Wireless Sensor Nodes, *M. Seeman, S. Sanders and J. Rabaey, University of California Berkeley*

TP-05 **571**
A Low Standby Power Flip-flop with Reduced Circuit and Control Complexity, *L. Clark, M. Kabir and J. Knudsen, Arizona State University*

TP-06 **575**
A 610-MHz FIR Filter Using Rotary Clock Technique, *Z. Yu and X. Liu, North Carolina State University*

TP-07 **579**
A 186Mvertices/s 161mW Floating-Point Vertex Processor for Mobile Graphics Systems, *C.-H. Yu, K. Chung, D. Kim and L.-S. Kim, KAIST*

TP-08 **583**
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TP-09 **587**
Addressing Parametric Impact of Systematic Pattern Variations in Digital IC Design, *P.-H. Wang, B. Lee, G. Han, UMC, R. Rouse, P. Hurat and N. Verghese, Clear Shape Technologies*

TP-10 **591**
Design Considerations and Benefits of Three-Dimensional Ternary Content Addressable Memory, *E. C. Oh and P. Franzon, North Carolina State University*

TP-11 **595**
A 37 ppm/degC Temperature Compensated CMOS ASIC with ±16 V Supply Protection for Capacitive Microaccelerometers, *H. Ko, S.-J. Paik, B. Choi, D.-I. Cho, Seoul National University, and A. Lee, T. Ahn, SML Electronics*

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TP-14 **607**
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Session 20 – Analog Techniques

Oak Ballroom, Wednesday Morning, September 19
Chair: Don Thelen
Co-Chair : Dennis Fischette

This session presents analog circuit design techniques used in frequency selective filters, image sensors, and temperature and process compensated oscillators.

8:25 am
Introduction

10:10 am - BREAK

Session 21 –High Performance Processors and Digital Techniques

Fir Ballroom, Wednesday Morning, September 19
Chair: Aurangzeb Khan
Co-Chair: Henry Chang

This session examines processor architectures, design methods, and implementations in 90nm and 65nm. Additional digital techniques are explored in the areas of low power, reliability and emulation-based verification.

8:25 am
Introduction

21.1 - 8:30 am **711**
Cell Broadband Engine Processor Design Methodology (INVITED PAPER), *O. Takahashi, E. Behnen, S. Cottier, P. Coulman, S. Dhong, B. Flachs, P. Hofstee, C. Johnson and S. Posluszny, IBM*

21.2 - 9:20 am **717**
Implementation of the 65nm Cell Broadband Engine, *M. Riley, B. Flachs, S. Dhong, G. Gervais, S. Weitzel, M. Wang, D. Boerstler, M. Bolliger, J. Keaty, J. Pille, R. Berry,and O. Takahashi, IBM, Y. Nishino, Sony Computer Entertainment, T. Uchino, Toshiba America*

21.3 - 9:45 am **721**
Compact Fault Recovering Flip-Flop with Adjusting Clock Timing Triggered by Error Detection, *S. Yasuda and S. Fujita, Toshiba Corporation*

10:10 am - BREAK

21.4 - 10:25 am **725**
A 2GHz, 7W (max) 64b Power™ Microprocessor Core, *D. Murray, J. Burnette, B. Campbell, M. Chung, B. Fernandes, S. Ghosh, R. Goel, G. Hess, H. Huang, Z. Huang, N. Javarappa, P. Kanapathipilai, F. Klass, F. Liu, A. Mehta, Y. Modukuru, N. Nerurkar, A. Radhakrishnan, S. Santhanam, J. Sugisawa, S. Sundar, H. J. Tam, R. Wen E. Wu, J.-C. Yeh, J. Yong, and Z. Zambare, PA Semi, Inc.*

21.5 - 10:50 am **729**
Power-Efficient Dual-Supply 64kB L1 Caches in a 65nm CMOS Technology, *B. Campbell, J. Burnette, N. Javarappa and V. von Kaenel, PA Semi, Inc.*

21.6 - 11:15 am **733**
Process-Tolerant Low-Power Adaptive Pipeline under Scaled-Vdd, *S. Ghosh, P. Batra, K. Kim and K. Roy, Purdue University*

21.7 - 11:40 am **737**
ASIC Design and Verification in an FPGA Environment, *D. Markovic, C. Chang, B. Richards, H. So, B. Nikolic and R. Brodersen, University of California Berkeley*

Session 22 – mm-Wave Systems and Building-Blocks

Pine Ballroom, Wednesday Morning, September 19
Chair: Cicero Vaucher
Co-Chair: John Rogers

This session will present advances in mm-Wave transmitters and receivers. In addition the design of on-chip programmable phase shifters and mm-wave power amplifiers will be addressed.

8:25 am
Introduction

22.1 - 8:30 am **741**
mm-Wave Silicon ICs: Challenges and Opportunities (INVITED PAPER), *A. Hajimiri, California Institute of Technolgy*

22.2 - 9:20 am **749**
65-nm CMOS, W-Band Receivers for Imaging Applications, *K. Tang, M. Khanpour, S. Voinigescu, University of Toronto, P. Garcia, C. Garnier, STMicroelectronics*

22.3 - 9:45 am **753**
A 4-Channel 24-27 GHz UWB Phased Array Transmitter in 0.13µm CMOS for Vehicular Radar, *H. Krishnaswamy and H. Hashemi, University of Southern California*

10:10 am - BREAK

22.4 - 10:25 am **757**
A CMOS 22-29GHz Receiver Front-End for UWB Automotive Pulse-Radars, *V. Jain, P. Heydari, University of California Irvine and S. Sundararaman, Avago Technologies*

22.5 - 10:50 am **761**
An X- and Ku-Band 8-Element Linear Phased Array Receiver, *K.-J. Koh and G. M. Rebeiz, University of California, San Diego*

22.6 - 11:15 am **765**
A 30-40 GHz 1:16 Internally Matched SiGe Active Power Divider for Phased Array Transmitters, *J. May and G. Rebeiz, University of California, San Diego*

22.7 - 11:40 am **769**
A 60 GHz Power Amplifier in 90nm CMOS Technology, *B. Heydari, M. Bohsali, E. Adabi and A. Niknejad, University of California Berkeley*

Session 23 – Methodology and Design for Process Variability Mitigation

Cedar Ballroom, Wednesday Morning, September 19
Chair: Philippe Jansen
Co-Chair: Hamid Mahmoodi

This session addresses different aspects and approaches to mitigate process variability for yield enhancement for nano-scale CMOS technologies. The discussed topics include yield estimation, design/process interaction, and design for yield.

8:25 am
Introduction

23.1 - 8:30 am **773**
At Tape-out: Can System Yield in Terms of Timing/Energy Specifications Be Predicted? (INVITED PAPER), *A. Papanikolaou, M. Miranda, P. Marchal, B. Dierickx and F. Catthoor, IMEC*

23.2 - 8:55 am **779**
Process/Product Interactions in a Concurrent Design Environment (INVITED PAPER), *L. Bair, Advanced Micro Devices*

23.3 - 9:20 am **783**
Dynamic Supply Noise Measurement with All Digital Gated Oscillator for Evaluating Decoupling Capacitance Effect, *Y. Ogasahara, M. Hashimoto and T. Onoye, Osaka University*

23.4 - 9:45 am **787**
An Embedded 8-bit RISC Controller for Yield Enhancement of the 90-nm PRAM, *H. Kim, J. Yoo, H.-J. Yoo, KAIST, and K. Sohn, Samsung*

10:10 am - BREAK

Session 24 – Advanced Memories

Cedar Ballroom, Wednesday Morning, September 19
Chair : Kenji Noda
Co-Chair: Sreedhar Natarajan

This session covers SRAM alternatives, and describes the evolution of electronically-programmed fuses to enable redundancy.

10:20 am
Introduction

24.1 - 10:25 am **791**
A 180 Kbit Embeddable MRAM Memory Module, *J. J. Nahas, T. Andre, B. Garni, C. Subramanian, H. Lin, S.M. Alam, K. Papworth and W. L. Martino, Jr., Freescale Semiconductor*

24.2 - 10:50 am **795**
A 1.0GHz multi-banked embedded DRAM in 65nm CMOS featuring concurrent refresh and hierarchical BIST, *D. Anand, J. Covino, J. Dreibelbis, J. Fifield, K. Gorman, M. Jacunski, J. Paparelli, G. Pomichter, D. Pontius, M. Roberge and S. Sliva, IBM*

24.3 - 11:15 am **799**
Electrically Programmable Fuse (eFUSE): From Memory Redundancy to Autonomic Chips (INVITED PAPER), *N. Robson, J. Safran, C. Kothandaraman, A. Cestero, X. Chen, R. Rajeevakumar, A. Leslie, D. Moy, T. Kirihata and S. Iyer, IBM*

Session 25 – Advanced Oscillator Concepts

Oak Ballroom, Wednesday Afternoon, September 19
Chair: Trudy Stetzler
Co-Chair: Nobuyuki Itoh

Oscillators form the fundamental building blocks of all wireless transceivers. Oscillators also play an important role in power efficient frequency dividers. The papers in this session examine the basic trade-offs in oscillator performance and novel low phase noise topologies.

1:30 pm
Introduction

25.1 - 1:35 pm **805**
Advanced Design Techniques for Integrated Voltage Controlled LC Oscillators (INVITED PAPER), *P. Kinget, B. Soltanian, S. Xu, S.-A. Yu and F. Zhang, Columbia University*

25.2 - 2:25 pm **813**
A 0.5-V 16GHz-20GHz Differential Injection-Locked Divider in 0.18-µm CMOS Process, *H. Zheng and H. Luong, The Hong Kong University of Science and Technology*

25.3 - 2:50 pm **817**
A 1V 4GHz-and-10GHz Transformer-Based Dual-Band Quadrature VCO in 0.18µm CMOS, *S. Rong and H. C. Luong, The Hong Kong University of Science and Technology*

Session 26 – Imagers and MEMS

Fir Ballroom, Wednesday Afternoon, September 19
Chair: Sang-Soo Lee
Co-Chair: Makoto Nagata

This session presents CMOS image sensors for DNA microarrays, electrochemical and fluorescence detection, as well as a high frame rate imager and a MEMs-based system for in-vivo neural imaging.

1:30 pm
Introduction

26.1 - 1:35 pm **821**
A CMOS Image Sensor for DNA Microarrays, *S. Parikh, G. Gulak and P. Chow, The University of Toronto*

26.2 - 2:00 pm **825**
Active CMOS Array for Electrochemical Sensing of Biomolecules, *P. Levine, P. Gong, K. Shepard, Columbia University, and R. Levicky, Polytechnic University*

26.3 - 2:25 pm **829**
A CMOS Array Sensor for Sub-800-ps Time-Resolved Fluorescence Detection, *T.-C. Huang, K. Shepard, P. Gong, Columbia University, and R. Levicky, Polytechnic University*

26.4 - 2:50 pm **833**
A High-Speed CMOS Image Sensor with On-chip Parallel Image Compression Circuits, *Y. Nishikawa, S. Kawahito, M. Furuta, Shizuoka University, and T. Tamura, Photron Ltd.*

26.5 - 3:15 pm **837**
Integration of CMOS and MEMS Technologies in the Development of a Neural Imaging and Interface Device: Showcase of an Emerging Bioimaging Technique, *D. Ng, T. Mizuno, T. Tokuda, M. Nunoshita, H. Tamura, Y. Ishikawa, S. Shiosaka and J. Ohta, Nara Institute of Science and Technology*

Session 27 – Substrate Noise Modeling; Behavioral Models

Pine Ballroom, Wednesday Afternoon, September 19
Chair: Laurence Nagel
Co-Chair: Gennady Gildenblat

Recent substrate noise models are the subject of the first part of the session. The second part includes applications of behavioral modeling to advanced integrated circuit design.

1:30 pm
Introduction

27.1 - 1:35 pm **841**
Physical Model for Power Supply Noise and Chip/Package Co-Design in Gigascale Systems with the Consideration of Hot Spots, *G. Huang, D. Sekar, A. Naeemi, J. Meindl, Georgia Institute of Technology, K. Shakeri, Cypress Semiconductor*

27.2 - 2:00 pm **845**
Simulation and Modeling of Substrate Noise Generation from Synchronous and Asynchronous Digital Logic Circuits, *C. Hanken, J. Le, T. Fiez and K. Mayaram, Oregon State University*

27.3 - 2:25 pm **849**
Chip-Level Substrate Noise Analysis with Emphasis of Vertical Impurity Profile for Isolation, *D. Kosaka, M. Nagata, Kobe University, Y. Murasaka, A. Iwata, A-R-Tec*

27.4 - 2:50 pm **853**
Automated Extraction of Model Parameters for Noise Coupling Analysis in Silicon Substrates, *B. Peterson, K. Mayaram and T. Fiez, Oregon State University*

27.5 - 3:15 pm **857**
Modeling and Simulation of Noise in Closed-Loop All-Digital PLLs using Verilog-A, *W. Fergusson, R. Patel and W. Bereza, Altera Corp.*

3:40m - BREAK

27.6 - 3:50 pm **861**
Time-Domain Modeling of a Phase-Domain All-Digital Phase-Locked Loop for RF Applications, *I. Syllaios, P. Balsara, University of Texas, and R. Staszewski, Texas Instruments*

27.7 - 4:15 pm **865**
Accurate Modeling of RF Circuit Blocks: Weakly-Nonlinear Narrowband LNAs, *J. Croon, D. Leenaerts and D. Klaassen, NXP Semiconductors*

27.8 - 4:40 pm **869**
Analytical Eye-diagram Model for On-chip Distortionless Transmission Lines and Its Application to Design Space Exploration, *M. Hashimoto, J. Siriporn, Osaka University, A. Tsuchiya, Kyoto University, H. Zhu and C.-K. Cheng, University of California, San Diego*