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8:30 am Keynote Presentation
Dr. Bill Krenik, Chief Technical Officer for Texas Instruments' Wireless Terminals Business Unit

Session 2 –3D and SiP

Oak Ballroom, Monday Morning, September 17

Chair: Rakesh Patel
Co-Chair : Ann Rincon

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Pine Ballroom, Monday Morning, September 17

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Cedar Ballroom, Monday Morning, September 17

Chair: Jennifer Lloyd
Co-Chair: Un-Ku Moon

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Oak Ballroom, Monday Afternoon, September 17
 Chair: Raj Amirtharajah
 Co-Chair: Steve Wilton

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 Chair: Stefan Drude
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Pine Ballroom, Monday Afternoon, September 17
 Chair: Dawn Fitzgerald
 Co-Chair: Sudhir Aggarwal

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Cedar Ballroom, Monday Afternoon, September 17
 Chair: Jeanne Trinko Mechler
 Co-Chair: Gordon Roberts

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Will Digital Designers Eat Their Lunch At 45nm And Below?

Session 11 – Biomedical Sensors

Pine Ballroom, Monday Afternoon, September 17
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Co-Chair : Ken Szajda

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Session 13 – Clocking and CDRs

Fir Ballroom, Tuesday Morning, September 18

Chair : Jafar Savoj

Co-Chair: Kimo Tam

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Session 14 – Power Management Techniques

Pine Ballroom, Tuesday Morning, September 18

Chair: Steve Garverick

Co-Chair: Makoto Takamiya

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Session 15 – CMOS Scaling and Technology Implications

Cedar Ballroom, Tuesday Morning, September 18

Chair: David Sunderland

Co-Chair: Jordan Lai

This session of invited papers addresses important issues related to maintaining Moore's Law scaling beyond 45nm, focusing on device technology, package technology, reliability and physical analysis.

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Chair: Charles Thomas

Co-Chair: Ram Krishnamurthy

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Fir Ballroom, Tuesday Afternoon, September 18

Chair: Tony Chan Carusone

Co-Chair: Ed Van Tuijl

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A Heterodyne Phase Locked Loop with GHz Acquisition Range for Coherent Locking of Semiconductor Lasers in 0.13 μ m CMOS, F. Aflatouni, O. Momeni and H. Hashemi, USC

17.2 - 2:30 pm 467
A Synthesis-based Bandwidth Enhancing Technique for CML Buffers/Amplifiers, D. Pi, B.-K. Chun and P. Heydari, University of California

17.3 - 2:55 pm 471
Towards a sub-2.5V, 100-Gb/s Serial Transceiver (INVITED PAPER), S. Voinescu, R. Aroca, S. Nicolson, T. Chalvatzis, University of Toronto, P. Chevalier, P. Garcia, C. Gamier and B. Sautreuil, STMicroelectronics, T. Dickson, IBM

3:45 pm - BREAK

17.4 - 4:00 pm 479
Future Microprocessor Interfaces: Analysis, Design and Optimization (INVITED PAPER), B. Casper, G. Balamurugan, J. Jaussi, J. Kennedy, M. Mansuri, F. O'Mahony and R. Mooney, Intel Corporation

17.5 - 4:50 pm 487
Time-Variant Characterization and Compensation of Wideband Circuits, A. Amirkhany, M. Horowitz, Stanford University, A. Abbasfar, J. Savoj, Rambus, Inc.

17.6 - 5:15 pm 491
High-Voltage-Tolerant I/O Circuit Design for USB 2.0-Compliant Applications, M.-J. Kim, T.H. Lee, Stanford University, H. Icking, H. Gossner, Infineon Technology

Session 18 – Compact Modeling for Analog and RF

Pine Ballroom, Tuesday Afternoon, September 18

Chair: Rob Jones

Co-Chair: Hong-Ha Vuong

This session presents advanced compact models and modeling/synthesis approaches to address analog and RF applications.

2:00 pm
Introduction

18.1 - 2:05 pm 495
PSP-Based Scalable MOS Varactor Model (INVITED PAPER), J. Victory, Z. Yan, J. Cordovez, Jazz Semiconductor, Z. Zhu, Q. Zhou, W. Wu, G. Gildenblat, Arizona State University, C. McAndrew, Freescale Semiconductor, F. Anderson, IBM, J. Paasschens, NXP Semiconductors, R. van Langevelde, Philips Research, P. Kolev, Qualcomm, R. Cheme, Intersil Corp. and C. Yao, Analog Devices

18.2 - 2:55 pm 503
An Accurate Scalable Compact Model for the Substrate Resistance of RF MOSFETs, B. Parvais, M. Dehan, A. Mercha, S. Decoutere, IMEC, S. Hu, Shanghai IC R&D Center

18.3 - 3:20 pm 507
Synthesis of Optimal On-Chip Baluns, S. Kapur, D. Long, R. Frye, Integrand Software, Y.-C. Chen, M.-H. Cho, H.-W. Chang, J.-H. Ou and B. Hung, UMC

3:45 pm - BREAK

18.4 - 4:00 pm 511
An Integrated Modeling Paradigm of Circuit Reliability for 65nm CMOS Technology, W. Wang, R. Vattikonda, Y. Cao, Arizona State University and V. Reddy, A. Krishnan, S. Krishnan, Texas Instruments

18.5 - 4:25 pm 515
Mismatch Characterization of Ring Oscillators, A. Balankutty, T.-C. Chih, C.-Y. Chen and P. Kinget, Columbia University

18.6 - 4:50 pm 519
The Advanced Compact MOSFET (ACM) Model for Circuit Analysis and Design (INVITED PAPER), C. Galup-Montoro, M. Schneider, O. Siebel, Federal University of Santa Catarina, A. Cunha, Federal University of Bahia, F. Sousa, Federal University of Rio Grande do Norte, and H. Klimach, Federal University of Rio Grande do Sul

Session 19 – Front-Ends and Synthesizers for Communication Applications

Cedar Ballroom, Tuesday Afternoon, September 18

Chair: Ranjit Gharpurey
Co-Chair: Rick Carley

This session begins with presentations on four receiver front ends, covers two frequency synthesizers, and finishes with a high efficiency CMOS cellular power amplifier.

2:00 pm
Introduction

19.1 - 2:05 pm 527
A 3.5mW 900MHz Down-converter with Multiband Feedback and Device Transconductance Reuse, J. Han and R. Gharpurey, University of Texas Austin

19.2 - 2:30 pm 531
A Highly Linear Broadband Variable Gain LNA for TV Applications, D. Manstretta, Universita' degli Studi di Pavia, and L. Dauphinee, Broadcom Corp.

19.3 - 2:55 pm 535
A Current-Equalized Distributed Receiver Front-End for UWB Direct Conversion Receivers, A. Safarian, L. Zhou and P. Heydari, University of California Irvine

19.4 - 3:20 pm 539
A 65 μ W, 1.9 GHz RF to Digital Baseband Wakeup Receiver for Wireless Sensor Nodes, N. Pletcher, S. Gambini and J. Rabaey, University of California, Berkeley

3:45 pm - BREAK

19.5 - 4:00 pm 543
A 4GHz Low Complexity ADPLL-based Frequency Synthesizer in 90nm CMOS, J. Zhuang, Q. Du and T. Kwasniewski, Carleton University

19.6 - 4:25 pm 547
A 4.2 GHz PLL Frequency Synthesizer with an Adaptively Tuned Coarse Loop, T. Wu, Rambus Inc., P. Hanumolu, K. Mayaram and U.-K. Moon, Oregon State University

19.7 - 4:50 pm 551
A 1.7-GHz 31dBm differential CMOS Class-E Power Amplifier with 58% PAE, R. Brama, L. Larcher, A. Mazzanti, Universita di Modena e Reggio Emilia and F. Svelto, Universita di Pavia

Poster Session

Cascade Ballroom, Tuesday Afternoon, September 18
5:30 pm – 7:30 pm
(Authors are at the posters from 5:30 pm – 7:00 pm)

TP-01 555
A 2.4GHz Efficiency-Enhanced Rectifier for Wireless Telemetry, K.-H. Chen, J.-H. Lu and S.-I. Liu, National Taiwan University

TP-02 559
Comparative Studies of Common Control Schemes for Reference Tracking and Application of End-point Prediction, Y. Wu and P. K. T. Mok, Hong Kong University of Science and Technology

TP-03 563
An Energy Management Circuit for Self-Powered Ubiquitous Sensor Modules, J. Pan and Y. Inoue, Waseda University

TP-04 567
An Ultra-Low-Power Power Management IC for Wireless Sensor Nodes, M. Seeman, S. Sanders and J. Rabaey, University of California Berkeley

TP-05 571
A Low Standby Power Flip-flop with Reduced Circuit and Control Complexity, L. Clark, M. Kabir and J. Knudsen, Arizona State University

TP-06 575
A 610-MHz FIR Filter Using Rotary Clock Technique, Z. Yu and X. Liu, North Carolina State University

TP-07 579
A 186Mvertices/s 161mW Floating-Point Vertex Processor for Mobile Graphics Systems, C.-H. Yu, K. Chung, D. Kim and L.-S. Kim, KAIST

TP-08 583
A 0.8-1.2GHz Single-Phase Resonant-Clocked FIR Filter with Level-Sensitive Latches, V. Sathe, J. Kao and M. Papaefthymiou, University of Michigan

TP-09 587
Addressing Parametric Impact of Systematic Pattern Variations in Digital IC Design, P.-H. Wang, B. Lee, G. Han, UMC, R. Rouse, P. Hurat and N. Verghese, Clear Shape Technologies

TP-10 591
Design Considerations and Benefits of Three-Dimensional Ternary Content Addressable Memory, E. C. Oh and P. Franzon, North Carolina State University

TP-11 595
A 37 ppm/degC Temperature Compensated CMOS ASIC with ± 16 V Supply Protection for Capacitive Microaccelerometers, H. Ko, S.-J. Paik, B. Choi, D.-I. Cho, Seoul National University, and A. Lee, T. Ahn, SML Electronics

TP-12 599
A 500 MHz Low Phase-Noise A1N-on-Silicon Reference Oscillator, H. M. Lavasani, R. Abdolvand and F. Ayazi, Georgia Institute of Technology

TP-13 603
1.1 TMACS/mW Load-Balanced Resonant Charge-Recycling Array Processor, R. Karakiewicz, R. Genov, University of Toronto and G. Cauwenberghs, University of California San Diego

TP-14 607
Optimization of SC Sigma Delta Modulators based on Worst-Case-Aware Pareto-Optimal Fronts, J. Zou, H. Graeb, D. Mueller and U. Schlichtmann, Techn. Univ. Muenchen

TP-15	611
Obtaining Frequency Sensitivities to Variations Analytically from Parameterized Nonlinear Oscillator Phase Macromodels , Z. Wang and J. Roychowdhury, University of Minnesota	
TP-16	615
Modeling and Validation of Silicon Contour-Based Extraction and Simulation of Non-Uniform Devices , T. Devoivre, STMicroelectronics, R. Rouse, N. Verghese and P. Hurat, Clear Shape Technologies	
TP-17	619
Standard Cell and Custom Circuit Optimization using Dummy Diffusions through STI Width Stress Effect Utilization , R. O. Topaloglu, University of California	
TP-18	623
FinFET SRAM: Optimizing Silicon Fin Thickness and Fin Ratio to Improve Stability at iso Area , D. Lekshmanan, A. Bansal and K. Roy, Purdue University	
TP-19	627
A Comprehensive Phase-Transfer Model for Delay-Locked Loops , J. Bumham, Stanford University, G.Y. Wei, Harvard University, C.-K. K. Yang, UCLA, and H. Hindi, PARC	
TP-20	631
Efficient Frequency-Domain Simulation of Massive Clock Meshes Using Parallel Harmonic Balance , W. Dong, P. Li and X. Ye, Texas A&M University	
TP-21	635
Low-Voltage Multi-Mode G_m-C Channel Selection Filter for Mobile Applications , T.-Y. Lo and C.-C. Hung, National Chiao Tung University	
TP-22	639
Multi-Mode Modulator and Frequency Demodulator Circuits for Gb/s Data Rate 60 GHz Wireless Transceivers , A. Valdes-Garcia, S. Reynolds and T. Beukema, IBM TJ Watson	
TP-23	643
CMOS Low Noise Amplifier with Capacitive Feedback Matching , E. Adabi and A. Niknejad, University of California Berkeley	
TP-24	647
A 750Mb/s 12pJ/b 6-to-10GHz Digital UWB Transmitter , V. Kulkarni, M. Muqsith, H. Ishikuro and T. Kuroda, Keio University	
TP-25	651
A 3.1-8.0 GHz MB-OFDM UWB Transceiver in 0.18μm CMOS , H. Zheng, S. Lou, D. Lu, C. Shen, T. Chan and H. Luong, The Hong Kong University of Science and Technology	
TP-26	655
A -90dBm Sensitivity 0.13μm CMOS Bluetooth Transceiver Operating in Wide Temperature Range , K. Agawa, H. Majima, H. Kobayashi, M. Koizumi, S. Ishizuka, T. Nagano, M. Arai, Y. Shimizu, G. Urakawa, N. Itoh, M. Hamada and N. Otsuka, Toshiba Corporation	
TP-27	659
On IIP2 Improvement by Injecting DC Offset at the Mixer in a Wireless Receiver , I. Elahi and K. Muhammad, Texas Instruments	
TP-28	663
ECO chip: Energy Consumption Zeroize Chip with a 953MHz High-Sensitivity Radio Wave Detector for Standby Mode Applications , T. Umeda and S. Otaka, Toshiba R&D Center	
TP-29	667
On the Transient Behavior of Injection Locked LC Oscillators , N. Lanka, S. Patnaik and R. Harjani, University of Minnesota	

TP-30	671
A Wideband CMOS Linear Digital Phase Rotator , H. Wang and A. Hajimiri, California Institute of Technology	

TP-31	675
Low-Power CMOS Energy Detection Transceiver for UWB Impulse Radio System , T.-A. Phan, V. Krizhanovskii, S.G. Lee, Information and Communications University	

Session 20 – Analog Techniques

Oak Ballroom, Wednesday Morning, September 19

Chair: Don Thelen

Co-Chair : Dennis Fischette

This session presents analog circuit design techniques used in frequency selective filters, image sensors, and temperature and process compensated oscillators.

8:25 am
Introduction

20.1 - 8:30 am	679
An 80MHz Noise Optimized Continuous-Time Bandpass Filter in 0.25 μm BiCMOS , A. Kumar and P. Allen, Georgia Institute of Technology	

20.2 - 8:55 am	683
A Low Power 44-300 MHz Programmable Active-RC Filter in 0.18μm CMOS , T. Laxminidhi, V. Prasadu and S. Pavan, Indian Institute of Technology-Madras	

20.3 - 9:20 am	687
A Q-enhanced Transformer Coupling Dynamic Dual-Mode 5GHz Bandpass NB / Interference Rejection UWB Filter , B. Pham and A. Dinh, University of Saskatchewan	

20.4 - 9:45 am	691
A Process and Temperature Compensated Two-Stage Ring Oscillator , K. Lakshmikummar, V. Mukundagiri and S. Gierkink, Conexant Systems	

10:10 am - BREAK

20.5 - 10:25 am	695
Signal Processing Architectures for Low-Noise High-Resolution CMOS Image Sensors (INVITED PAPER) , S. Kawahito, Shizuoka University	

20.6 - 10:50 am	703
A 1.8 mm², 11 mA, 23.2 dB-NF, discrete-time filter for GSM/WCDMA/WLAN using retiming technique , T. Sano, T. Maruyama, I. Yasui, H. Sato and T. Shimizu, Renesas Technology	

20.7 - 11:15 am	707
An Equalized Ultra-Wideband Channel-Select Filter with a Discrete-Time Charge-Domain Band-Pass IIR Filter , A. Yoshizawa and S. Iida, Sony Corporation	

Session 21 –High Performance Processors and Digital Techniques

Fir Ballroom, Wednesday Morning, September 19

Chair: Aurangzeb Khan

Co-Chair: Henry Chang

This session examines processor architectures, design methods, and implementations in 90nm and 65nm. Additional digital techniques are explored in the areas of low power, reliability and emulation-based verification.

8:25 am Introduction	
21.1 - 8:30 am Cell Broadband Engine Processor Design Methodology (INVITED PAPER), O. Takahashi, E. Behnen, S. Cottier, P. Coulman, S. Dhong, B. Flachs, P. Hofstee, C. Johnson and S. Posluszny, IBM	711
21.2 - 9:20 am Implementation of the 65nm Cell Broadband Engine, M. Riley, B. Flachs, S. Dhong, G. Gervais, S. Weitzel, M. Wang, D. Boerstler, M. Bolliger, J. Keaty, J. Pille, R. Berry, and O. Takahashi, IBM, Y. Nishino, Sony Computer Entertainment, T. Uchino, Toshiba America	717
21.3 - 9:45 am Compact Fault Recovering Flip-Flop with Adjusting Clock Timing Triggered by Error Detection, S. Yasuda and S. Fujita, Toshiba Corporation	721

10:10 am - BREAK

21.4 - 10:25 am A 2GHz, 7W (max) 64b Power™ Microprocessor Core, D. Murray, J. Burnette, B. Campbell, M. Chung, B. Femandes, S. Ghosh, R. Goel, G. Hess, H. Huang, Z. Huang, N. Javarappa, P. Kanapathipilai, F. Klass, F. Liu, A. Mehta, Y. Modukuru, N. Nerurkar, A. Radhakrishnan, S. Santhanam, J. Sugisawa, S. Sundar, H. J. Tam, R. Wen E. Wu, J.-C. Yeh, J. Yong, and Z. Zambare, PA Semi, Inc.	725
21.5 - 10:50 am Power-Efficient Dual-Supply 64kB L1 Caches in a 65nm CMOS Technology, B. Campbell, J. Burnette, N. Javarappa and V. von Kaenel, PA Semi, Inc.	729
21.6 - 11:15 am Process-Tolerant Low-Power Adaptive Pipeline under Scaled-Vdd, S. Ghosh, P. Batra, K. Kim and K. Roy, Purdue University	733
21.7 - 11:40 am ASIC Design and Verification in an FPGA Environment, D. Markovic, C. Chang, B. Richards, H. So, B. Nikolic and R. Brodersen, University of California Berkeley	737

Session 22 – mm-Wave Systems and Building-Blocks

Pine Ballroom, Wednesday Morning, September 19

Chair: Cicero Vaucher

Co-Chair: John Rogers

This session will present advances in mm-Wave transmitters and receivers. In addition the design of on-chip programmable phase shifters and mm-wave power amplifiers will be addressed.

8:25 am
Introduction

22.1 - 8:30 am mm-Wave Silicon ICs: Challenges and Opportunities (INVITED PAPER), A. Hajimiri, California Institute of Technology	741
22.2 - 9:20 am 65-nm CMOS, W-Band Receivers for Imaging Applications, K. Tang, M. Khanpour, S. Voinigescu, University of Toronto, P. Garcia, C. Gamier, STMicroelectronics	749
22.3 - 9:45 am A 4-Channel 24-27 GHz UWB Phased Array Transmitter in 0.13µm CMOS for Vehicular Radar, H. Krishnaswamy and H. Hashemi, University of Southern California	753

10:10 am - BREAK

22.4 - 10:25 am A CMOS 22-29GHz Receiver Front-End for UWB Automotive Pulse-Radars, V. Jain, P. Heydari, University of California Irvine and S. Sundararaman, Avago Technologies	757
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22.5 - 10:50 am An X- and Ku-Band 8-Element Linear Phased Array Receiver, K.-J. Koh and G. M. Rebeiz, University of California, San Diego	761
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22.6 - 11:15 am A 30-40 GHz 1:16 Internally Matched SiGe Active Power Divider for Phased Array Transmitters, J. May and G. Rebeiz, University of California, San Diego	765
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22.7 - 11:40 am A 60 GHz Power Amplifier in 90nm CMOS Technology, B. Heydari, M. Bohsali, E. Adabi and A. Niknejad, University of California Berkeley	769
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Session 23 – Methodology and Design for Process Variability Mitigation

Cedar Ballroom, Wednesday Morning, September 19

Chair: Philippe Jansen

Co-Chair: Hamid Mahmoodi

This session addresses different aspects and approaches to mitigate process variability for yield enhancement for nano-scale CMOS technologies. The discussed topics include yield estimation, design/process interaction, and design for yield.

8:25 am
Introduction

23.1 - 8:30 am At Tape-out: Can System Yield in Terms of Timing/Energy Specifications Be Predicted? (INVITED PAPER), A. Papanikolaou, M. Miranda, P. Marchal, B. Dierickx and F. Catthoor, IMEC	773
23.2 - 8:55 am Process/Product Interactions in a Concurrent Design Environment (INVITED PAPER), L. Bair, Advanced Micro Devices	779

23.3 - 9:20 am Dynamic Supply Noise Measurement with All Digital Gated Oscillator for Evaluating Decoupling Capacitance Effect, Y. Ogasahara, M. Hashimoto and T. Onoye, Osaka University	783
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23.4 - 9:45 am An Embedded 8-bit RISC Controller for Yield Enhancement of the 90-nm PRAM, H. Kim, J. Yoo, H.-J. Yoo, KAIST, and K. Sohn, Samsung	787
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10:10 am - BREAK

Session 24 – Advanced Memories

Cedar Ballroom, Wednesday Morning, September 19

Chair: Kenji Noda

Co-Chair: Sreedhar Natarajan

This session covers SRAM alternatives, and describes the evolution of electronically-programmed fuses to enable redundancy.

10:20 am
Introduction

24.1 - 10:25 am A 180 Kbit Embeddable MRAM Memory Module, J. J. Nahas, T. Andre, B. Gami, C. Subramanian, H. Lin, S.M. Alam, K. Papworth and W. L. Martino, Jr., Freescale Semiconductor	791
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24.2 - 10:50 am 795
A 1.0GHz multi-banked embedded DRAM in 65nm CMOS featuring concurrent refresh and hierarchical BIST, D. Anand, J. Covino, J. Dreibelbis, J. Fifield, K. Gorman, M. Jacunski, J. Paparelli, G. Pomichter, D. Pontius, M. Roberge and S. Sliva, IBM

24.3 - 11:15 am 799
Electrically Programmable Fuse (eFUSE): From Memory Redundancy to Autonomic Chips (INVITED PAPER), N. Robson, J. Safran, C. Kothandaraman, A. Cestero, X. Chen, R. Rajeevakumar, A. Leslie, D. Moy, T. Kihata and S. Iyer, IBM

Session 25 – Advanced Oscillator Concepts

Oak Ballroom, Wednesday Afternoon, September 19

Chair: Trudy Stetzler

Co-Chair: Nobuyuki Itoh

Oscillators form the fundamental building blocks of all wireless transceivers. Oscillators also play an important role in power efficient frequency dividers. The papers in this session examine the basic trade-offs in oscillator performance and novel low phase noise topologies.

1:30 pm
Introduction

25.1 - 1:35 pm 805
Advanced Design Techniques for Integrated Voltage Controlled LC Oscillators (INVITED PAPER), P. Kinget, B. Soltanian, S. Xu, S.-A. Yu and F. Zhang, Columbia University

25.2 - 2:25 pm 813
A 0.5-V 16GHz-20GHz Differential Injection-Locked Divider in 0.18- μ m CMOS Process, H. Zheng and H. Luong, The Hong Kong University of Science and Technology

25.3 - 2:50 pm 817
A 1V 4GHz-and-10GHz Transformer-Based Dual-Band Quadrature VCO in 0.18 μ m CMOS, S. Rong and H. C. Luong, The Hong Kong University of Science and Technology

Session 26 – Imagers and MEMS

Fir Ballroom, Wednesday Afternoon, September 19

Chair: Sang-Soo Lee

Co-Chair: Makoto Nagata

This session presents CMOS image sensors for DNA microarrays, electrochemical and fluorescence detection, as well as a high frame rate imager and a MEMS-based system for in-vivo neural imaging.

1:30 pm
Introduction

26.1 - 1:35 pm 821
A CMOS Image Sensor for DNA Microarrays, S. Parikh, G. Gulak and P. Chow, The University of Toronto

26.2 - 2:00 pm 825
Active CMOS Array for Electrochemical Sensing of Biomolecules, P. Levine, P. Gong, K. Shepard, Columbia University, and R. Levicky, Polytechnic University

26.3 - 2:25 pm 829
A CMOS Array Sensor for Sub-800-ps Time-Resolved Fluorescence Detection, T.-C. Huang, K. Shepard, P. Gong, Columbia University, and R. Levicky, Polytechnic University

26.4 - 2:50 pm 833
A High-Speed CMOS Image Sensor with On-chip Parallel Image Compression Circuits, Y. Nishikawa, S. Kawahito, M. Furuta, Shizuoka University, and T. Tamura, Photron Ltd.

26.5 - 3:15 pm 837
Integration of CMOS and MEMS Technologies in the Development of a Neural Imaging and Interface Device: Showcase of an Emerging Bioimaging Technique, D. Ng, T. Mizuno, T. Tokuda, M. Nunoshita, H. Tamura, Y. Ishikawa, S. Shiosaka and J. Ohta, Nara Institute of Science and Technology

Session 27 – Substrate Noise Modeling; Behavioral Models

Pine Ballroom, Wednesday Afternoon, September 19

Chair: Laurence Nagel

Co-Chair: Gennady Gildenblat

Recent substrate noise models are the subject of the first part of the session. The second part includes applications of behavioral modeling to advanced integrated circuit design.

1:30 pm
Introduction

27.1 - 1:35 pm 841
Physical Model for Power Supply Noise and Chip/Package Co-Design in Gigascale Systems with the Consideration of Hot Spots, G. Huang, D. Sekar, A. Naeemi, J. Meindl, Georgia Institute of Technology, K. Shakeri, Cypress Semiconductor

27.2 - 2:00 pm 845
Simulation and Modeling of Substrate Noise Generation from Synchronous and Asynchronous Digital Logic Circuits, C. Hanken, J. Le, T. Fiez and K. Mayaram, Oregon State University

27.3 - 2:25 pm 849
Chip-Level Substrate Noise Analysis with Emphasis of Vertical Impurity Profile for Isolation, D. Kosaka, M. Nagata, Kobe University, Y. Murasaka, A. Iwata, A-R-Tec

27.4 - 2:50 pm 853
Automated Extraction of Model Parameters for Noise Coupling Analysis in Silicon Substrates, B. Peterson, K. Mayaram and T. Fiez, Oregon State University

27.5 - 3:15 pm 857
Modeling and Simulation of Noise in Closed-Loop All-Digital PLLs using Verilog-A, W. Fergusson, R. Patel and W. Bereza, Altera Corp.

3:40m - BREAK

27.6 - 3:50 pm 861
Time-Domain Modeling of a Phase-Domain All-Digital Phase-Locked Loop for RF Applications, I. Syllaios, P. Balsara, University of Texas, and R. Staszewski, Texas Instruments

27.7 - 4:15 pm 865
Accurate Modeling of RF Circuit Blocks: Weakly-Nonlinear Narrowband LNAs, J. Croon, D. Leenaerts and D. Klaassen, NXP Semiconductors

27.8 - 4:40 pm 869
Analytical Eye-diagram Model for On-chip Distortionless Transmission Lines and Its Application to Design Space Exploration, M. Hashimoto, J. Siripom, Osaka University, A. Tsuchiya, Kyoto University, H. Zhu and C.-K. Cheng, University of California, San Diego