

2007 IFIP International Conference on Very Large Scale Integration

**Atlanta, GA
15-17 October 2007**



IEEE Catalog Number: CFP07LSI-PRT
ISBN 10: 1-4244-1709-0
ISBN 13: 978-1-4244-1709-4

Contents

<i>Message from the General and Program Chairs</i>	iii
<i>Committees</i>	iv
<i>Technical Program Committee</i>	v
<i>Additional Reviewers</i>	vi
<i>Conference Overview</i>	vii
<i>Conference Venue</i>	viii
<i>Keynote Speakers</i>	ix
<i>Programme-At-A-Glance</i>	xiii
<i>Technical Program</i>	xvii

Session 1: Analog Circuit Design

Power Invariant Secure IC Design Methodology Using Reduced Complementary Dynamic and Differential Logic <i>Vijay Sundaresan, Srividhya Rammohan and Ranga Vemuri</i>	1
Neuromorphic Building Blocks for Adaptable Cortical Feature Maps <i>C. M. Markan and Priti Gupta</i>	7
An Analog Programmable Multi-Dimensional Radial Basis Function Based Classifier <i>Sheng-Yu Peng, Paul E. Hasler and David Anderson</i>	13

Session 2: CAD Tools

ReCPU: A Parallel and Pipelined Architecture for Regular Expression Matching <i>Marco Paolieri, Ivano Bonesana and Marco D. Santambrogio</i>	19
Use of Gray Decoding for Implementation of Symmetric Functions <i>Osnat Keren, Ilya Levin and Radomir S. Stankovic</i>	25
Parametric Structure-Preserving Model Order Reduction <i>Jorge Fernandez Villena, Wil H. A. Schilders and L. Miguel Silveira</i>	31

Session 3: Modeling and Simulation

Hierarchical Statistical Analysis of Performance Variation for Continuous-Time Delta-Sigma Modulators <i>Hua Tang</i>	37
--	----

First Order Quasi-Static SoI MOSFET Channel Capacitance Model <i>Sameer Sharma and L. G. Johnson</i>	42
Regression Based Circuit Matrix Models for Accurate Performance Estimation of Analog Circuits <i>Almitra Pradhan and Ranga Vemuri</i>	48
Session 4: Reconfigurable Systems	
A Software-Supported Methodology for Designing High-Performance 3D FPGA Architectures <i>Kostas Siozios, Kostas Sotiriadis, Vassilis F. Pavlidis and Dimitrios Soudris</i>	54
Estimating Design Time for System Circuits <i>Cyrus Bazeghi, Francisco J. Mesa-Martínez, Brian Greskamp, Josep Torrellas and Jose Renau</i>	60
Transparent Acceleration of Data Dependent Instructions for General Purpose Processors <i>Antonio Carlos Schneider Beck and Luigi Carro</i>	66
Session 5: Communication	
VLSI Models of Network-on-Chip Interconnect <i>Dimitrios N. Serpanos and Wayne Wolf</i>	72
Statistical Analysis of Systematic and Random Variability of Flip-Flop Race Immunity in 130 nm and 90 nm CMOS Technologies <i>Gustavo Neuberger, Fernanda Kastensmidt, Ricardo Reis, Gilson Wirth, Ralf Brederlow and Christian Pacha</i>	78
AC-Coupling Strategy for High-Speed Transceivers of 10 Gbps and Beyond <i>Yikui (Jen) Dong, Steve Howard, Freeman Zhong, Scott Lowrie, Ken Paradis, Jan Kolnik and Jeff Burleson</i>	84
Session 6: High-Level Synthesis	
SWORD: A SAT Like Prover Using Word Level Information <i>Robert Wille, Görschwin Fey, Daniel Große, Stephan Eggarsglüß and Rolf Drechsler</i>	88
Obtaining Delay Distribution of Dynamic Logic Circuits by Error Propagation at the Electrical Level <i>Lucas Brusamarello, Roberto da Silva, Gilson I. Wirth and Ricardo A. L. Reis</i>	94
Minimizing Wire Delays by Net-Topology Aware Binding During Floorplan-Driven High Level Synthesis <i>Vyas Krishnan and Srinivas Katkoori</i>	99
Session 7: New Devices	
A High-Driving Class-AB Buffer Amplifier with a New Pseudo Source Follower <i>Chih-Wen Lu, Yen-Chih Shen and Meng-Lieh Sheu</i>	105
A New Analytical Approach of the Impact of Jitter on Continuous Time Delta Sigma Converters <i>Julien Goulier, Eric Andre and Marc Renaudin</i>	110
Transistor Level Automatic Layout Generator for Non-Complementary CMOS Cells <i>Adriel Ziesemer, Cristiano Lazzari and Ricardo Reis</i>	116

Session 8 (Special Session 1): Reconfigurable and Hybrid System

Computing and Design for Software and Silicon Manufacturing <i>Davide Pandini, Giuseppe Desoli and Alessandro Cremonesi</i>	122
An Adaptive Genetic Algorithm for Dynamically Reconfigurable Modules Allocation <i>Vincenzo Rana, Chiara Sandionigi, Marco Santambrogio and Donatella Sciuto</i>	128
New Tool Support and Architectures in Adaptive Reconfigurable Computing <i>Jürgen Becker, Adam Donlin and Michael Hübner</i>	134

Session 9: Architecture and Compiler

Rate-Based Scheduling Policy for QoS Flows in Networks on Chip <i>Aline Mello, Ney Calazans and Fernando Moraes</i>	140
Parallelized Radix-2 Scalable Montgomery Multiplier <i>Nan Jiang and David Harris</i>	146
An Efficient Heterogeneous Reconfigurable Functional Unit for an Adaptive Dynamic Extensible Processor <i>Arash Mehdizadeh, Behnam Ghavami, Morteza Saheb Zamani, Hossein Pedram and Farhad Mehdipour</i>	151

Session 10 (Special Session 2): Architecture Design Principles

Simulation of Hybrid Computer Architectures: Simulators, Methodologies and Recommendations <i>Pranav Vaidya and Jaehwan John Lee</i>	157
New Parallel Programming Techniques for Hardware Design <i>Satnam Singh</i>	163
Efficient DSP Algorithm Development for FPGA and ASIC Technologies <i>Shiv Balakrishnan and Chris Eddington</i>	168

Session 11: Physical Design and Test

Incremental Placement for Structured ASICs Using the Transportation Problem <i>Andrew C. Ling, Deshanand P. Singh and Stephen D. Brown</i>	172
Test Data Compression and TAM Design <i>Julien Dalmaso, Marie-Lise Flottes and Bruno Rouzeyre</i>	178
Dynamic Gates with Hysteresis and Configurable Noise Tolerance <i>Krishna Santhanam and Kenneth S. Stevens</i>	184

Session 12: Signal and Image Processing

A Low-Power Deblocking Filter Architecture for H.264 Advanced Video Coding <i>Jaemoon Kim, Sangkown Na and Chong-Min Kyung</i>	190
The Hazard-Free Superscalar Pipeline Fast Fourier Transform Algorithm and Architecture <i>Bassam Jamil Mohd, Adnan Aziz and Earl E. Swartzlander Jr.</i>	194

An Efficient H.264 Intra Frame Coder System Design <i>Ilker Hamzaoglu, Ozgur Tasdizen and Esra Sahin</i>	200
---	-----

Session 13: Verification and Validation

Qualification of Behavioral Level Design Validation for AMS & RF SoCs <i>Yves Joannon, Vincent Berouille, Chantal Robach, Smail Tedjini and Jean-Louis Carbonero</i>	206
Evaluating Memory Sharing Data Size and TCP Connections in the Performance of a Reconfigurable Hardware-Based Architecture for TCP/IP Stack <i>Jean Carlo Hamerski, Everton Reckziegel and Fernanda Lima Kastensmidt</i>	212
Impact of Hardware Emulation on the Verification Quality Improvement <i>Youssef Serrestou, Vincent Berouille and Chantal Robach</i>	218

Session 14: Estimation and Evaluation

Fast Estimation of Software Energy Consumption Using IPI(Inter-Prefetch Interval) Energy Model <i>Jungsoo Kim, Kyungsu Kang, Heejun Shim, Woong Hwangbo and Chong-Min Kyung</i>	224
Power Optimization for Conditional Task Graphs in DVS Enabled Multiprocessor Systems <i>Parth Malani, Prakash Mukre and Qinru Qiu</i>	230
A Minimum-Latency Block-Serial Architecture of a Decoder for IEEE 802.11n LDPC Codes <i>Massimo Rovini, Giuseppe Gentile, Francesco Rossi and Luca Fanucci</i>	236

Session 15: New Devices for Mixed Signal

Full Custom Design of a Three-Stage Amplifier with 5500 MHz.pF/mW Performance in 0.18 μ m CMOS <i>Run Chen, Liyuan Liu, Dongmei Li and Zhihua Wang</i>	242
A 128 dB Dynamic Range 1 kHz Bandwidth Stereo ADC with 114 dB THD <i>YuQing Yang, Terry Sculley and Jacob Abraham</i>	248

Session 16: Low Power Design

A Bit-Sliced, Scalable and Unified Montgomery Multiplier Architecture for RSA and ECC <i>M. Sudhakar, R. V. Kamala and M. B. Srinivas</i>	252
Low Power On-Chip Thermal Sensors Based on Wiresan <i>Basab Datta and Wayne P. Burleson</i>	258
A Low-Power CAM Using a 12-Transistor Design Cell <i>Saleh Abdel-Hafeez, Shadi M. Harb and William R. Eisenstadt</i>	264

Session: Poster

Improvement of Dual Rail Logic as a Countermeasure Against DPA <i>A. Razafindraibe, M. Robert and P. Maurine</i>	270
---	-----

A VHDL Based Approach for Fast and Accurate Energy Consumption Estimations <i>César A. M. Marcon, Sérgio Johann Filho and Fabiano P. Hessel</i>	276
Circuit Prospects of DGFET: Variable Gain Differential Amplifier and a Schmitt Trigger with Adjustable Hysteresis <i>Srimoyee Sen, Urmimala Roy, Chaitanya Kshirsagar, Navakanta Bhat and Chandan Kumar Sarkar</i>	280
High Speed SOC Design for Blowfish Cryptographic Algorithm <i>Brian Cody, Justin Madigan, Spencer MacDonald and Kenneth W. Hsu</i>	284
Implementing Cellular Automata Modeled Applications on Network-on-Chip Platforms <i>N. Zompakis, L. Papadopoulos, G. Sirakoulis and D. Soudris</i>	288
Optimum IR Drop Models for Estimation of Metal Resource Requirements for Power Distribution Network <i>Rishi Bhooshan and Bindu P. Rao</i>	292
Impact of Task Migration in NoC-Based MPSoCs for Soft Real-Time Applications <i>Eduardo Wenzel Brião, Daniel Barcelos, Fabio Wronski and Flávio Rech Wanger</i>	296
A Flexible Design Flow for a Low Power RFID Tag <i>José C. S. Palma, César Marcon, Fabiano Hessel, Eduardo Bezerra, Guilherme Rohde, Luciano Azevedo, Carlos Reif and Carolina Metzler</i>	300
Co-Synthesis of Custom On-Chip Bus and Memory for MPSoC Architectures <i>Sujan Pandey, Christian Genz and Rolf Drechsler</i>	304
An HDTV H.264 Deblocking Filter in FPGA with RGB Video Output <i>Vagner S. Rosa, Altamiro A. Susin and Sergio Bampi</i>	308
Efficient Timing Closure with a Transistor Level Design Flow <i>Cristiano Lazzari, Cristiano Santos, Adriel Ziesemer, Lorena Anghel and Ricardo Reis</i>	312
Hybrid Multiplierless FIR Filter Architecture Based on NEDA <i>J. Luis Tecpanecatl-Xihuitl, Ruth M. Aguilar-Ponce and Magdy Bayoumi</i>	316
A Genetic Algorithm Based Heuristic Technique for Power Constrained Test Scheduling in Core-Based SOCs <i>Chandan Giri, Soumojit Sarkar and Santanu Chattopadhyay</i>	320
<i>Author Index</i>	325