



36th International Symposium on
Multiple-Valued Logic

Singapore
17-20 May 2006



Image courtesy of Singapore Tourism Board



Sponsored by
IEEE Computer Society
Nanyang Technological University
Singapore Tourism Board

Product Number E2532

ISBN 0-7695-2532-6

ISSN 0195-623X

Table of Contents

36th International Symposium on Multiple-Valued Logic – ISMVL 2006

Message from the Symposium Chairs.....	viii
Message from the Program Chair.....	ix
Organizing Committee.....	x
List of Reviewers.....	xi

Session 1: Invited Address

Design Methods for Multiple-Valued Input Address Generators.....	1
<i>T. Sasa</i> o	

Session 2: Circuits I

Algorithm Level Interpretation of Fast Adder Structures in Binary and Multiple-Valued Logic.....	2
<i>N. Homma, T. Aoki, and T. Iguchi</i>	

On Designs of Radix Converters using Arithmetic Decompositions.....	3
<i>Y. Iguchi, T. Sasa</i> o, and <i>M. Matsuura</i>	

New Data Encoding Method with a Multiple-Valued Logic for Low Power Asynchronous Circuit Design.....	4
<i>E. J. Choi, J. H. Lee, and K. R. Cho</i>	

Highly Reliable Multiple-Valued Circuit Based on Dual-Rail Differential Logic.....	5
<i>A. Mochizuki and T. Hanyu</i>	

Evaluation of Multiple-Valued Packet Multiplexing Scheme for Network-on-Chip Architecture.....	6
<i>H. M. Munirul, T. Hasegawa, and M. Kameyama</i>	

Session 3: Algebra and Logic

On the Range of Algebraic Functions on Lattices. A Preliminary Report.....	7
<i>S. Rudeanu and D. Simovici</i>	

Upper and Lower Bounds on the Number of Disjunctive Forms.....	8
<i>H. Tatsumi, M. Miyakawa, and M. Mukaidono</i>	

Completeness of a Hypersequent Calculus for Some First-Order Gödel Logic with Delta.....	9
<i>M. Baaz, N. Preining, and R. Zach</i>	

Assumption Based Multiple-Valued Semantics for Extended Logic Programs.....	10
<i>D. Stamate</i>	

Session 4: Circuits II

Implementation of Multiple-Valued CAM Functions with LUT Cascades.....	11
<i>T. Sasao and J. Butler</i>	
The New Architecture for Radix-4 Chinese Abacus.....	12
<i>S.-C. Yi, K.-T. Lee, J.-J. Chen, C.-H. Lin, C.-C. Wang, C.-F. Hsieh, C.-Y. Lu</i>	
Fine-Grain Cell Design for Multiple-Valued Reconfigurable VLSI Using a Single Differential-Pair Circuit.....	13
<i>H. M. Munirul and M. Kameyama</i>	
Design of a Microprocessor Datapath Using Four-Valued Differential-Pair Circuits.....	14
<i>A. Mochizuki, T. Kitamura, H. Shirahama, and T. Hanyu</i>	
A Quaternary Half-Adder Using Current Mode Operation with Bipolar Transistors.....	15
<i>C. R. Mingoto</i>	

Session 5: Invited Address

Signal Processing Algorithms and Multiple-Valued Logic Design Methods.....	16
<i>J. Astola</i>	

Session 6: Circuits III

Switch Block Architecture for Multi-Context FPGAs Using Hybrid Multiple-Valued/Binary Context Switching Signals.....	17
<i>Y. Nakatani, M. Hariyama, and M. Kameyama</i>	
A Novel Balanced Ternary Adder Using Recharged Semi-Floating Gate Devices.....	18
<i>H. Gundersen and Y. Berg</i>	
A High-Density Ternary Content-Addressable Memory Using Single-Electron Transistors.....	19
<i>K. Degawa, T. Aoki, T. Higuchi, H. Inokawa, K. Nishiguchi, and Y. Takahashi</i>	
A Feedback-Signal Shaping Technique for Multi-Level Continuous-Time Delta-Sigma Modulators with Clock-Jitter.....	20
<i>M. Tanihata and T. Waho</i>	

Session 7: Algebra and Clones

Commuting Hyperoperations.....	21
<i>J. Pantović and G. Vojvodić</i>	
Theoretical Basis of Commutation Theory for Partial Clones.....	22
<i>L. Haddad, H. Machida, and I. Rosenberg</i>	
Associativity Test in Hypergrupoids <i>I. Rosenberg, M. Miyakawa, and H. Tatsumi</i>	23
Some Observations on Minimal Clones.....	24
<i>H. Machida and M. Pinsker</i>	

Session 8: Systems and Satisfiability

Efficiency and Multiple-Valued Encoding in SAT-Based ATPG..... <i>G. Fey, J. Shi, and R. Drechsler</i>	25
Towards Solving Many-Valued MaxSAT..... <i>J. Argelich, X. Domingo, F. Manya, and J. Planes</i>	26
Random Multiple-Valued Networks: Theory and Applications..... <i>E. Dubrova</i>	27

Session 9: Decision Diagrams and Decision Trees

Representation of Elementary Functions using Decision Diagrams..... <i>T. Sasao and S. Nagayama</i>	28
Embedding and Assembling Technique for Spatial Computing Structure Design using Decision Trees and Diagrams..... <i>S. Yanushkevich, O. R. Boulanov, and V. Shmerko</i>	29
QMDD: A Decision Diagram Structure for Reversible and Quantum Circuits..... <i>D. Miller and M. Thornton</i>	30
Arithmetic-Haar Spectral Transform Decision Diagrams..... <i>B. J. Falkowski and S. Yan</i>	31

Session 10: Quantum Logic and Spectral Techniques

Multi-Valued Quantum Logic..... <i>Michael Katz</i>	32
A Quantum CAD Accelerator Based on Grover's Algorithm for Finding the Minimum Fixed Polarity Reed-Muller Form..... <i>L. Li, M. Thornton, and M. Perkowski</i>	33
Generation and Relation of Quaternary and Binary Linearly Independent Transforms..... <i>B. J. Falkowski and C. Fu</i>	34
Properties of Matrix-Valued Spectral Coefficients with the Fourier Transform on a Non-Abelian Group..... <i>C. Moraga, R. Stanković, and J. Astola</i>	35
<i>Author Index</i>	36