

# **2007 50<sup>th</sup> Midwest Symposium on Circuits and Systems**

**Montreal, QC, Canada  
5-8 August 2007**

**Pages 1-410**



**IEEE Catalog Number:**  
**ISBN 10:**  
**ISBN 13:**

**CFP07MID-PRT**  
**1-4244-1175-0**  
**978-1-4244-1175-7**

# Table of Contents

<b>A Programmable Clock Generator HDL Softcore .....</b>	<b>1</b>
<i>H. Eisenreich, C. Mayr, S. Henker, M. Wickert, and R. Schüffny</i>	
<b>Variation Aware Extracted Timing Model.....</b>	<b>5</b>
<i>Ratnakar Goyal, Naresh Kumar, Harindranath Parameswaran</i>	
<b>Metastability Tolerant Mesochronous Synchronization .....</b>	<b>9</b>
<i>Syed Rafay Hasan, Yvon Savaria</i>	
<b>High Speed Current-Mode Signalling for Interconnects Considering Transmission line and Crosstalk Effects .....</b>	<b>13</b>
<i>Mohammad Moghaddam Tabrizi, Nasser Masoumi, Mahsa Deilami</i>	
<b>A Tapered Partitioning Method for "Delay Energy product" Optimization in Global Interconnects.....</b>	<b>17</b>
<i>Mahdiyeh Mehran, Nasser Masoumi</i>	
<b>Low-Voltage, Low-Power Rail-to-Rail two stage Op-amp with Dynamic Biasing and no Miller compensation.....</b>	<b>21</b>
<i>Jaime Ramírez-Angulo, A. J. Lopez-Martin, Annajirao Garimella, Lalitha M. Kalyani-Garimella and R.G. Carvajal</i>	
<b>Low-Power and Robust On-Chip Thermal Sensing Using Differential Ring Oscillators .....</b>	<b>25</b>
<i>Basab Datta and Wayne Burlison</i>	
<b>Low-distortion, emitter-coupled, differential voltage-to-current converters .....</b>	<b>29</b>
<i>M. Mathew, K. Hayatleh, B.L. Hart and F.J. Lidgely</i>	
<b>Electrically Evoked Compound Action Potential (ECAP) Stimulus-Artifact (SA) Blanking Low-Power Low-Noise CMOS Amplifier.....</b>	<b>33</b>
<i>Dean Wheatley, Torsten Lehmann</i>	
<b>Versatile Multidecade CMOS Voltage Controlled Oscillator with Accurate Amplitude and PWM Control .....</b>	<b>37</b>
<i>Annajirao Garimella, Lalitha M Kalyani-Garimella, Randy Romero, Jaime Ramírez-Angulo, Ramon G. Carvajal, Antonio J. Lopez-Martin</i>	
<b>Design of Mth-band Filters for Image Interpolation Application .....</b>	<b>41</b>
<i>Chao Wu, Wei-Ping Zhu, and M.N.S. Swamy</i>	
<b>Design of a Radix-4 Booth Multiplier with Neighborhood Dependent Approach for Video Processing Applications.....</b>	<b>45</b>
<i>Hau T. Ngo and Vijayan K. Asari</i>	
<b>A Piecewise Polynomial Canonical Representing Function and its Application to Image Edge Processing .....</b>	<b>49</b>
<i>Hideaki Okazaki, Tomo Shidara, Yoichi Okubo</i>	
<b>A CMOS Imager with On-pixel Gray-Scale Erosion.....</b>	<b>53</b>
<i>Duha Jabakhanji, Maitham Shams</i>	
<b>Evolvable Reconfigurable Hardware Framework for Edge Detection .....</b>	<b>57</b>
<i>Nader I. Rafla</i>	
<b>CMOS Integrated System for Magnetic Field Monitoring and Gradient Measurement in MRI Environment.....</b>	<b>61</b>
<i>Vincent Frick, Joris Pascal, Luc Hebrard, Jean-Philippe Blondie, Jacques Felblinger</i>	
<b>Detection of Epileptic Seizures in Stereo-EEG using Frequency-Weighted Energy.....</b>	<b>65</b>
<i>Rajeev Yadav, Rajeev Agarwal and M. N. S. Swamy</i>	
<b>A High Efficiency Full-Wave Rectifier in Standard CMOS Technology.....</b>	<b>69</b>
<i>Gaurav Bawa, Uei-Ming Jow and Maysam Ghovanloo</i>	
<b>Fully-Pipelined CORDIC Implementation of Subspace-Based Speech Enhancement .....</b>	<b>73</b>
<i>Pavel Sinha, M.N.S. Swamy, P.K. Meher</i>	

# Table of Contents

<b>A New Wavelet Function for Audio and Speech Processing</b> .....	77
<i>Alfredo Mantilla-Caeiros , Mariko Nakano-Miyatake, Hector Perez-Meana</i>	
<b>A Formant Frequency Estimation Algorithm for Speech Signals with Low Signal-to-Noise Ratio</b> .....	81
<i>S.A. Fattah, W.-P. Zhu, and M.O. Ahmad</i>	
<b>Rational Dither Modulation in Audio Signals</b> .....	85
<i>Jose Juan Garcia Hernandez, Mariko Nakano Miyatake and Hector Perez Meana</i>	
<b>Unique In-Fiber Photonic Crystal Sensor</b> .....	89
<i>Beiu R.-M., Stanescu C-tin.D., Beiu V.</i>	
<b>Burst-Mode Clock and Data Recovery with FEC and Fast Phase Acquisition for Burst-Error Correction in GPONs</b> .....	93
<i>Bhavin J. Shastri, Julien Faucher Ming Zeng, and David V. Plant</i>	
<b>All-Optical Swapping of Spectral Amplitude Labels Using Cross-Gain Modulation in Hybrid Semiconductor Fiber Ring Lasers</b> .....	97
<i>Varghese Baby, Christian Habib, and Lawrence R. Chen</i>	
<b>Scaling rule of optically differential reconfigurable gate array VLSIs</b> .....	101
<i>Minoru Watanabe, Takenori Shiki and Fuminori Kobayashi</i>	
<b>A 100MS/s recycling 2-step ADC embedding Programmable Gain Amplification for DVB Satellite</b> .....	105
<i>He-Gong Wei, Chon-Kit Lai , Seng-Pan U and R.P. Martins</i>	
<b>A Nanowatt Successive Approximation ADC with a Calibrated Capacitor Array for Biomedical Applications</b> .....	109
<i>Karim Abdelhalim, Leonard MacEachern, Samy Mahmoud</i>	
<b>A Comprehensive Calibration Scheme for a 14-b 50 MSPS Pipeline ADC for multi-mode Wireless Receivers</b> .....	113
<i>Bahar Jalali</i>	
<b>A Prototype Implementation of a Two-Channel Frequency-Translating Hybrid ADC</b> .....	117
<i>Shahzad Jalali Mazlouman, Samad Sheikhaei and Shahriar Mirabbasi</i>	
<b>Second-Order .SAD Modulator with Novel Feedforward Architecture</b> .....	121
<i>Hao San, Hajime Konagaya, Feng Xu, Atsushi Motozawa, Haruo Kobayashi, Kazumasa Ando, Hiroshi Yoshida and Chieto Murayama</i>	
<b>A CMOS 3.4 mW 200 MHz Continuous-Time Delta-Sigma Modulator with 61.5 dB Dynamic Range and 5 MHz Bandwidth for Ultrasound Application</b> .....	125
<i>Pengyu Song, Kei-Tee Tiew, Yvonne Lam, Liang Mong Koh</i>	
<b>A 10-MHz Low-Power Always Valid Sample-and- Hold Circuit With Low-Droop Rate</b> .....	129
<i>Adnan Harb and Ali Assi</i>	
<b>Low Power Sigma Delta Modulator with Dynamic Biasing for Audio Applications</b> .....	132
<i>Hsin-Liang Chen, Yi-Sheng Lee, and Jen-Shiun Chiang</i>	
<b>Realization of a GIC Using Hybrid Current Conveyor/Operational Amplifier Circuits</b> .....	136
<i>Brent Maundy, Stephan Gift and Peter Aronhime</i>	
<b>A CMOS 650 MHz Seventh-order Current-Mode 0.05° Equiripple Linear Phase Filter</b> .....	140
<i>Xi Zhu, Yichuang Sun, and James Moritz</i>	
<b>Improved Low Voltage All Cascode Mirror Current Source Using the DC Level Shifter</b> .....	144
<i>Mohammad Sadegh Eslampanah Sendi, Iman Rezanejad Gatabi</i>	
<b>A Programmable Input-Pulse Dependent Chaotic Oscillator</b> .....	146
<i>Hamid Nejati, Tamer Ragheb, Amir Hosseini, and Yehia Massoud</i>	

# Table of Contents

<b>A CMOS High-Frequency and Low-Voltage Tunable Positive Transconductor with a Improved Linearization Technique .....</b>	<b>150</b>
<i>J. M. García del Pozo, P. A. Martínez , A. Otín, N. Medrano</i>	
<b>Temperature Insensitive Current Reference Circuit using Standard CMOS Devices .....</b>	<b>154</b>
<i>Takeshi Shima</i>	
<b>A CMOS Based Microfluidic Detector: Design, Calibration and Experimental Results .....</b>	<b>158</b>
<i>E. Ghafar-Zadeh, M. Sawan, M. Hajj-Hassan, M.A. Miled</i>	
<b>Precise bifurcation in an autonomous circuit with op amp based nonlinear resistors which op amps are out of normal operating conditions .....</b>	<b>162</b>
<i>Hideaki Okazaki, Kohei Hashimoto, Hideo Nakano</i>	
<b>An Undersampled Duty Cycle Jitter BIST Circuit.....</b>	<b>166</b>
<i>Zeljko Zilic</i>	
<b>New Low Power Current Memory Circuits .....</b>	<b>170</b>
<i>Jaime Ramírez-Angulo and Paul Vizcaino</i>	
<b>Implementation of Accurate Blind Real Time Interference Suppression.....</b>	<b>174</b>
<i>Jose Luis Ruiz-Chavira and Jaime Ramirez-Angulo, Christopher M. Brislawn</i>	
<b>Accurate Design of Two-Phase Voltage Doublers based on a Compact Mathematical Model .....</b>	<b>178</b>
<i>Albert Saiz-Vela, Pere Miribel-Català, Jordi Colomer, Manel Puig-Vidal, and Josep Samitier</i>	
<b>3.2-Gb/s 1024-b Rate-1/2 LDPC Decoder Chip Using a Flooding-Type Update-Schedule Algorithm.....</b>	<b>182</b>
<i>Naoya Onizawa, Tomokazu Ikeda and Takahiro Hanyu, Vincent C. Gaudet</i>	
<b>On Amplitude and Operating Point Control of a Voltage-Controlled Crystal Oscillator.....</b>	<b>186</b>
<i>Todd Wey</i>	
<b>Testing of LUT Delay Aliasing Faults in SRAM Based FPGAs Using Half-Frequencies .....</b>	<b>190</b>
<i>M.Y.Niamat, Dileep Koleti, M. Alam</i>	
<b>A Built In Self Test Scheme for Automatic Interconnect Fault Diagnosis in Multiple and Single FPGA Systems .....</b>	<b>194</b>
<i>M.Y. Niamat, Arunjit Sahni, M.M. Jamali</i>	
<b>A Retargetable Embedded Code Scheduler for SoC Design Space Exploration under Real-Time Constraints .....</b>	<b>198</b>
<i>Jose Otavio Carlomagno Filho, Luiz Fernando Penkal Santos, Luiz C. V. Santos</i>	
<b>Seamless Design Space Exploration for Automotive Systems.....</b>	<b>202</b>
<i>William Fornaciari, Mauro V. Angiolillo, Roberto Farina</i>	
<b>Automatically-Retargetable Model-Driven Tools for Embedded Code Inspection in SoCs .....</b>	<b>206</b>
<i>Max R. de O. Schultz, Alexandre K. I. Mendonça, Felipe G. Carvalho, Olinto J. V. Furtado, Luiz C. V. Santos</i>	
<b>Timing Specification in Transaction Level Modeling of Hardware/Software Systems .....</b>	<b>210</b>
<i>A. Tsikhanovich, E. M. Aboulhamid, G. Bois</i>	
<b>A Low-Voltage Class-AB CMOS Variable Gain Amplifier .....</b>	<b>214</b>
<i>Phanumas Khumsat, Piamsuk Anantaseth, Pasin Isarasena</i>	
<b>A 1.8 V - 400 MHz Programmable Gain Amplifier in 0.35 <math>\mu</math>m CMOS .....</b>	<b>218</b>
<i>B. Calvo, S. Celma, J. P. Alegre and M. T. Sanz</i>	
<b>A 0.35<math>\mu</math>m CMOS 1.8V Low-Power 175MHz Variable Gain Amplifier .....</b>	<b>222</b>
<i>J. P. Alegre, S. Celma, B. Calvo and J. M. García del Pozo</i>	
<b>A Robust Multi-application Automatic Gain Control Chip.....</b>	<b>226</b>
<i>Ndubuisi Ekekwe, Ralph Etienne-Cummings</i>	

# Table of Contents

<b>Design of Amplifiers with High Gain Accuracy and High Linearity</b> .....	230
<i>R. Wu, F.J. Lidgely and K. Hayatleh</i>	
<b>1.25 Gb/s Variable Transimpedance Amplifier in Digital CMOS Process</b> .....	234
<i>M.T. Sanz, J.M. García del Pozo, S. Celma, A. Sarmiento</i>	
<b>Efficient Feature Representation Employing PCA and VQ in the Transform Domain for Facial Recognition</b> .....	238
<i>Moataz M. Abdelwahab, Wasfy B. Mikhael</i>	
<b>Masked Nearly-Orthogonal Wavelet-Based Image Compression and its Application to Medical Imaging</b> .....	242
<i>Lakshmi Sugavaneswaran, M. N. S. Swamy, and Chunyan Wang</i>	
<b>On the Modeling of the Wavelet Image Coefficients using a Symmetric Generalized Hyperbolic PDF</b> .....	246
<i>M. I. H. Bhuiyan, M. Omair Ahmad, and M. N. S. Swamy</i>	
<b>Automated Formal Synthesis of Wallace Tree Multipliers</b> .....	250
<i>Osman Hasan, Skander Kort</i>	
<b>Fast Redundant Binary Partial Product Generators for Booth Multiplication</b> .....	254
<i>Bijoy Jose and Damu Radhakrishnan</i>	
<b>Hardware Reciprocation using Degree-3 Polynomials but Only 1 Complete Multiplication</b> .....	258
<i>Arnaud Tisserand</i>	
<b>Floating-Point Division and Square Root using a Taylor-Series Expansion Algorithm</b> .....	262
<i>Taek-Jun Kwon, Jeff Sondeen, Jeff Draper</i>	
<b>Pipelining High-Radix SRT Division Algorithms</b> .....	266
<i>Saurabh Upadhyay and James E. Stine</i>	
<b>Cache Leakage: A Leakage Aware Cache Simulator</b> .....	270
<i>Lushan Liu , Manjari Agarwal , Praveen Elakkumanan , Ramalingam Sridhar</i>	
<b>Equalization of Volterra Systems Using a Multilinear SVD Based Pseudo pth Order Inverse</b> .....	274
<i>Ernest Seagraves, Bruce Walcott, and David Feinauer</i>	
<b>Constructing Memory-Polynomial Models from Frequency-dependent AM/AM and AM/PM Measurements</b> .....	278
<i>Peter Singerl, and Gernot Kubin</i>	
<b>Implementation Models for Analog-to-Information Conversion via Random Sampling</b> .....	282
<i>Tamer Ragheb, Sami Kirolos, Jason Laska, Anna Gilbert, Martin Strauss, Richard Baraniuk, Yehia Massoud</i>	
<b>Architecture of a Configurable Centered Discrete Fractional Fourier Transform Processor</b> .....	286
<i>Pavel Sinha, Saibal Sarkar, Amitabha Sinha, Dhruba Basu</i>	
<b>A Chip Semiblind Receiver for STBC Downlink MC-CDMA Systems without Cyclic Prefix</b> .....	290
<i>Samphan Phrompichai, Peerapol Yuvapoositanon</i>	
<b>Application of Neural Networks for Linear/Nonlinear Microwave Modeling</b> .....	294
<i>Lei Zhang, Kui Bo, and Q. J. Zhang</i>	
<b>Neural Network based Universal Tone Detector</b> .....	298
<i>D. Sträußnigg, D. Schwingshackl and M. Schaller</i>	
<b>Rough-Winner-Take-All Self-Organizing Neural Network for Hardware Oriented Vector Quantization Algorithm</b> .....	302
<i>Hakaru Tomukoh, Takanori Koga, Keiichi Horio, Takeshi Yamakawa</i>	
<b>A Graphical Transform for Subexpression Elimination Using Genetic Algorithms</b> .....	306
<i>T. Williams, M. Ahmadi, W.C. Miller</i>	

# Table of Contents

<b>Separation of Complex Signals with Known Source Distributions in Time-Varying Channels using Optimum Complex Block Adaptive ICA.....</b>	<b>310</b>
<i>Raghuram Ranganathan, Thomas T Yang, Wasfy B Mikhael</i>	
<b>Continuous wavelet transform based source separation.....</b>	<b>314</b>
<i>Lee-Pierre Belley, Marcel Gabrea, Christian Gargour</i>	
<b>Estimating the Error Bound in QOBE Vowel Classification.....</b>	<b>318</b>
<i>Timothy Kraus, Gihan I. Mandour, Dale Joachim</i>	
<b>VAD INNES: A Voice Activity Detector For Noisy Industrial Environments.....</b>	<b>322</b>
<i>Julie Séris, Christian Gargour and Frédéric Laville</i>	
<b>A Simplified Method for Online Secondary Path Modeling in Multichannel ANC Systems.....</b>	<b>326</b>
<i>Muhammad Tahir Akhtar, Masahide Abe, Masayuki Kawamata, and Muhammad Tufail</i>	
<b>A Robust Pitch Detection Algorithm for Speech Signals in a Practical Noisy Environment.....</b>	<b>330</b>
<i>C. Shahnaz, W. -P. Zhu, and M. O. Ahmad</i>	
<b>Multitarget Tracking (MTT) in 3-D using 2-D Particle Filters with Single Passive Sensor.....</b>	<b>334</b>
<i>Jinseok Lee, Shung Han Cho, Xi Deng, Sangjin Hong and We-Duke Cho</i>	
<b>Speech Enhancement Based Noise PSD Estimator to Remove Cosine Shaped Residual Noise.....</b>	<b>338</b>
<i>A. Trabelsi, F.R. Boyer, and Y. Savaria</i>	
<b>A 1 GHz Decimation Filter for Sigma-Delta ADC.....</b>	<b>342</b>
<i>Yong Lian, Ying Wei, and Rajasekaran Chandrasekaran</i>	
<b>Time-Division Multiplexing Architecture for Hybrid Filter Bank A/D converters.....</b>	<b>346</b>
<i>Davud Asemani, Jacques Oksman</i>	
<b>FFT Filter Bank-Based CFAR Detection Schemes.....</b>	<b>350</b>
<i>Robert Inkol, Sichun Wang, Sreeraman Rajan</i>	
<b>Adaptive Filters Realized with Nano-scale VLSI Circuit Technology.....</b>	<b>354</b>
<i>C. Radhakrishnan and W. K. Jenkins, D. J. Krusienski</i>	
<b>Image Coding Based on Regular Cosine-Modulated Filter Banks.....</b>	<b>358</b>
<i>Toshiyuki Uto, Katsuhiko Ichihara, Masaaki Ikehara, and Kenji Ohue</i>	
<b>Efficient Time-Varying Loudness Estimation via the Hopping Goertzel DFT.....</b>	<b>362</b>
<i>Ryan J. Cassidy, Julius O. Smith</i>	
<b>A Novel Simultaneous Input and Output Matching Method for GPS CMOS Switched Low Noise Amplifier.....</b>	<b>364</b>
<i>Xuezhen Wang, Han-Chi Hsieh, Noshir Dubash, Gregg Zanfino, Armando Mendoza, and Douglas Schucker</i>	
<b>A Low Noise 13 GHz Power Efficient 16/17 Prescaler with Rail to Rail Output Amplitude.....</b>	<b>368</b>
<i>Evan Eschenko, Kamran Entesari</i>	
<b>A 3.1-4.8 GHz New CMOS Mixer Topology for IEEE 802.15.3a UWB Standard Receivers.....</b>	<b>372</b>
<i>Skandar Douss, Mourad Loulou, Farid Touati</i>	
<b>Microstrip Equivalent Parasitics Modeling of RFIC Interconnects.....</b>	<b>376</b>
<i>Jayanta Mukherjee, Young-Gi Kim, Inwon Suh, Patrick Roblin, Yao-Chian Lin, Wan Rone Liou, M Shojaei Baghini</i>	
<b>A Technique to Improve Noise Figure and Conversion Gain of CMOS Mixers.....</b>	<b>379</b>
<i>GH. Zareh Fatin, M. Savadi Oskoei, Z. D. Koozeh Kanani</i>	
<b>Beating the Power Limit of LC Oscillators.....</b>	<b>383</b>
<i>Zhongtao Fu, Anand Pappu and Alyssa Apsel</i>	
<b>Comparison Study of 3.5 GHz Class-F Power Amplifiers.....</b>	<b>387</b>
<i>Fuding Ge, Hongjiang Song</i>	

# Table of Contents

<b>Automated Design of Radio-Frequency Single-Ended Switched Capacitor Arrays using Genetic Algorithms</b> .....	391
<i>Luis Mendes,, E. J. Solteiro Pires, João Caldinhas Vaz,, Maria João Rosário,</i>	
<b>A 24GHz Multi-Phase PLL for Optical Communication</b> .....	395
<i>Yifei Luo, Kuan Zhou</i>	
<b>A 3.5 GHz CMOS Doherty Power Amplifier with Integrated Diode Linearizer Targeted for WiMax Applications</b> .....	399
<i>Xian Cui, Patrick Roblin, Jongsoo Lee, Young Gi Kim</i>	
<b>Sinusoidal and Relaxation Oscillations in Emitter-Coupled Multivibrators</b> .....	403
<i>I. M. Filanovsky, C. J. M. Verhoeven</i>	
<b>Synchronization of Two LC- Oscillators Using Nonlinear Models</b> .....	407
<i>I. M. Filanovsky, C. J. M. Verhoeven</i>	
<b>Low Noise Multi-band Voltage Controlled Oscillator Using MEMS Technology</b> .....	411
<i>Shumin Zhang, Wansheng Su, Mona E. Zaghoul</i>	
<b>A capacitively-coupled 5GHz CMOS LC oscillator with bias tuning capability</b> .....	416
<i>Sofia Vatti and Christos Papavassiliou</i>	
<b>Frequency of Oscillation of a Cross-Coupled CMOS VCO with Resistor Tail Biasing</b> .....	420
<i>Sinisa Milicevic and Leonard MacEachern</i>	
<b>Power-efficient FSM mapping in FPGAs through SEMB dormancy control</b> .....	424
<i>Arun Janarthanan, Anurag Tiwari, Karen A. Tomko</i>	
<b>A High-Frequency Very Low-Power Low-Pass Filter with a Wide Bandwidth and Gain Tuning Range</b> .....	428
<i>M. Savadi Oskoei, N. Masoumi, and M. Kamarei</i>	
<b>DDCC Based All-Pass Filters Using Minimum Number of Passive Elements</b> .....	432
<i>Bilgin Metin Oguzhan Cicekoglu, Kirat Pal</i>	
<b>A Hybrid Fine/Coarse Auto-Tuning Scheme for Digitally Programmable VHF Gm-C Filters</b> .....	436
<i>A. Otin, S. Celma, C. Aldea and M. T. Sanz</i>	
<b>3-phase Active-RC Tow-Thomas Biquad Complex Filter</b> .....	440
<i>Junya Matsuno, Hiroki Sato, Akira Hyogo, Keitaro Sikine</i>	
<b>Analytical Synthesis of Low-Sensitivity Voltage-Mode Odd-Nth-Order OTA-C Elliptic Filter Structure with the Minimum Number of Components</b> .....	444
<i>Chun-Ming Chang</i>	
<b>Generalized CFA Filter Topology Based on Gain Blocks</b> .....	448
<i>Brent Maundy, Stephan Gift and Peter Aronhime</i>	
<b>Reduction of EMI through Switching Frequency Dithering</b> .....	452
<i>Abbas A. Fardoun, Ali Assi, Esam H. Ismail</i>	
<b>A S. Based DC-DC Converter with Supply Noise Suppression</b> .....	456
<i>Kyle Schulmeyer, Chintan Trehan, and Kwong S. Chao</i>	
<b>Single-Inductor Dual-Output (SIDO) DC-DC Converters for Minimized Cross Regulation and High Efficiency in SoC Supplying Systems</b> .....	460
<i>Ming-Hsin Huang, Hong-Wei Huang, Jiun-Yan Peng, Tzung-Ling Tsai, Min-Chin Lee, Ching-Sung Wang, and Ke-Horng Chen</i>	
<b>Power MOSFET Array in LDO Regulator Compensation</b> .....	464
<i>Yung-Hsin Lin, Kuo-Lin Zheng, Ke-Horng Chen</i>	
<b>Interface Circuits between Adiabatic and Standard CMOS Circuits</b> .....	468
<i>Jianping Hu, Ling Wang, and Huiying Dong</i>	

# Table of Contents

<b>Low-Voltage Universal Capacitive Threshold Logic Gate and its Application in m-out-of-n Functions .....</b>	<b>472</b>
<i>Annajirao Garimella, Lalitha M. Kalyani-Garimella, Jaime Ramirez-Angulo, R.G. Carvajal and A. J. Lopez-Martin</i>	
<b>Timing-Driven Decomposition of a Fast Barrel Shifter .....</b>	<b>476</b>
<i>Sabyasachi Das, Sunil P. Khatri</i>	
<b>Improved Write Margin for 90nm SOI-7T-SRAM by Look-Ahead Dynamic Threshold Voltage Control .....</b>	<b>480</b>
<i>Masaaki Iijima, Kayoko Seto, Masahiro Numa, Akira Tada, Takashi Ipposhi</i>	
<b>Minimization of Frequency-Weighted I2-Sensitivity for State-Space Digital Filters Subject to I2-Scaling Constraints .....</b>	<b>484</b>
<i>Takao Hinamoto, Yukihiro Shibata, and Masayoshi Nakamoto</i>	
<b>Non-Uniform Bandwidth 3D Cone Filter Bank .....</b>	<b>488</b>
<i>Santosh Singh and D. Antony Louis Piriyakumar</i>	
<b>Design of Two-Dimensional Digital Filters Having Monotonic Amplitude-Frequency Responses Using Darlington-type Gyrator Networks.....</b>	<b>492</b>
<i>Muhammad Tariqus Salam, Venkat Ramachandran</i>	
<b>Real-Time, Low Cost Embedded De-noising of Motor Position Control Signals.....</b>	<b>496</b>
<i>Sami Khorbotly, Joan E. Carletta</i>	
<b>Experimental comparison of coupling effects on the performance of quadrature CMOS LC and RC oscillators.....</b>	<b>500</b>
<i>A. Allam, I. M. Filanovsky, Luís Bica Oliveira and Jorge R. Fernandes</i>	
<b>Optimizing MOSFET Channel Width for Low Phase Noise in LC Oscillators .....</b>	<b>504</b>
<i>Jayanta Mukherjee</i>	
<b>Implementation of MEMS-SAW device on RF Circuits for Wireless Applications .....</b>	<b>508</b>
<i>Amal Zaki, Hsu-Cheng Ou, Mona Zaghoul, Hamed Elsimary</i>	
<b>WCDMA/WIMAX Dual-Band Bandpass Filter Design Using Frequency Transformation and Circuit Conversion.....</b>	<b>512</b>
<i>Fahim Hassam, Slim Boumaiza</i>	
<b>Novel and simple table-based HBT large-signal model .....</b>	<b>516</b>
<i>Louay Degachi, Fadhel M. Ghannouchi</i>	
<b>A Two Port Network Model of CNT-FET for RF Characterization.....</b>	<b>520</b>
<i>Y. Xu and A. Srivastava</i>	
<b>Challenges for embedded software development.....</b>	<b>524</b>
<i>Michael V. Woodward, Pieter J. Mosterman</i>	
<b>Synthesis of physically heterogeneous systems on chip .....</b>	<b>528</b>
<i>Ian O'Connor, Hervé Charlery</i>	
<b>Exploring Different Methods for 2DR-tree Binary Search on a FPGA.....</b>	<b>532</b>
<i>J. E. Rice, J. Schultz, W. Osborn</i>	
<b>Hardware Optimization for a Reconfigurable Polyphase-FFT Design Using Common Sub-Expression Elimination .....</b>	<b>536</b>
<i>H. Ho and V. Szwarc, T. Kwasniewski</i>	
<b>Flatness-Based Control of an Electrostatic Torsional Micro-Mirror with Voltage Feedback.....</b>	<b>540</b>
<i>C.-G. Agudelo, G. Zhu, M. Packirisamy, and L. Saydy</i>	
<b>Nonlinear Closed-Loop Control of an Electrostatic Torsional Micro-Mirror by Means of Differential Actuation .....</b>	<b>544</b>
<i>C.-G. Agudelo, G. Zhu, and L. Saydy</i>	



# Table of Contents

<b>SiP Power Management Unit with Embedded Temperature Sensor Powered by Piezoelectric Vibration Energy Harvesting</b> .....	548
<i>Jordi Colomer, Pere Miribel, Albert Saiz-Vela, Jordi Brufau, Jordi Maña, Manel Puig-Vidal, Josep Samitier</i>	
<b>Smart Boost Converter for Battery Charging from Discontinuous Voltage Power Source in Underwater Environment</b> .....	552
<i>Umberto M. Cella, Alessandro Gandelli, Riccardo E. Zich</i>	
<b>Challenge on Compact Size DC-DC Buck Converters with High-Speed Current Sensor and On-Chip Inductors</b> .....	556
<i>Shih-Min Chen, Chun-Yu Hsieh, Ke-Horng Chen</i>	
<b>Design Methodology of a Hybrid Micro-Scale Fuel Cell-Thin-Film Lithium Ion Source</b> .....	560
<i>Min Chen, Justin P. Vogt, and Gabriel A. Rincón-Mora</i>	
<b>Hybrid Algorithms for Power System Unit Commitment</b> .....	564
<i>Lawrence Jenkins</i>	
<b>Performance of SiC Schottky Diodes</b> .....	568
<i>Veda Prakash Galigekere, Marian K. Kazimierczuk</i>	
<b>Time-multiplexed Systolic-array Processors for Realtime 2D IIR Beam Plane-wave Filters</b> .....	572
<i>H.L.P. Arjuna Madanayake, Leonard T. Bruton</i>	
<b>Cascadable ASIC Prototype for Real Time Time-Frequency Analysis</b> .....	576
<i>Ludovic Noury, Habib Mehrez, Francois Durbin, Andre Tissot</i>	
<b>Modeling of Temperature Effects on Nano-CMOS Devices with the Predictive Technologies</b> .....	580
<i>Ranjith Kumar and Volkan Kursun</i>	
<b>Temperature-Adaptive Body-Bias and Supply Voltage Scaling for Enhanced Energy Efficiency in Nano-CMOS Circuits</b> .....	584
<i>Ranjith Kumar and Volkan Kursun</i>	
<b>Adaptive Digital Linearization of a DRP based EDGE Transmitter for Cellular Handsets</b> .....	588
<i>Khurram Waheed, Seydou N. Ba</i>	
<b>An Efficient Variable Gain Homotopy Method Using the SPICE-Oriented Approach</b> .....	592
<i>Wataru Kuroki, Kiyotaka Yamamura, and Shingo Furuki</i>	
<b>A Model-Based Technique for Efficient Evaluation of Noise Robustness</b> .....	596
<i>Sami Kirolos, Mosin Mondal, Kartik Mohanram, and Yehia Massoud</i>	
<b>A Hybrid Approach For Analog Design Optimisation</b> .....	600
<i>L. Labrak, T. Tixier, Y. Fellah and N. Abouchi</i>	
<b>Efficient Volterra Series based Sensitivity Analysis of Mildly Nonlinear Circuits</b> .....	604
<i>Guoji Zhu, Ajoy Opal</i>	
<b>Constraint-Based Verification of Delta-Sigma Modulators using Interval Analysis</b> .....	608
<i>Ghiath Al Sammane, Mohamed H. Zaki, Sofi`ene Tahar and Guy Bois</i>	
<b>Optimal Synthesis of Delta-Sigma Modulator Topologies Considering SNR Variation</b> .....	612
<i>Hua Tang, Matthew M. Webb</i>	
<b>Electronic Circuit Design Using Multiobjective Optimization</b> .....	616
<i>Jan M'ichal, and Josef Dobe</i>	
<b>A Fully Integrated CMOS Transmitter Design for IR-UWB Communication Systems</b> .....	620
<i>Yanjie Wang, Sai M. Kilambi, Kris Iniewski and Vincent Gaudet</i>	
<b>8 GHz High Conversion Gain Darlington Mixer</b> .....	624
<i>Jongsoo Lee, Patrick Roblin, and Steven Bibyk, Chang-Woo Kim, Young-Gi Kim, Hyo-Dal Park</i>	

# Table of Contents

<b>On the Theoretical Limits of Noise-Gain-Mismatch Tradeoff in the Design of Multi-Stage Cascaded Transistor Amplifiers .....</b>	<b>628</b>
<i>Enrico F. Calandra, Bruno Di Maio, and Daniele Lupo</i>	
<b>A Low Power, Good Gain Flatness SiGe Low Noise Amplifier for 3.1-10.6GHz Ultra Wide Band Radio.....</b>	<b>632</b>
<i>Shih-Chih Chen, Ruey-Lue Wang, Cheng-Lung Tsai, Jui-Hao Shang, Chien-Hsuan Liu</i>	
<b>Subsurface Measurement Needs for Ecological, Hydrological and Agricultural Applications .....</b>	<b>636</b>
<i>Scott B. Jones, Krishna Shenai</i>	
<b>Data Fusion in Defense and National Security: Ubiquitous and Indispensable .....</b>	<b>640</b>
<i>Pranab K. Banerjee</i>	
<b>uSOL: A Programming Language for Sensor Networks .....</b>	<b>644</b>
<i>Ramesh Bharadwaj, Anupama Biswas, Jerry James, Supratik Mukhopadhyay</i>	
<b>Circuit Implementation of FitzHugh-Nagumo Neuron Model Using Field Programmable Analog Arrays .....</b>	<b>648</b>
<i>Jun Zhao, Yong-Bin Kim</i>	
<b>A Methodology for Evaluation Time Approximation.....</b>	<b>652</b>
<i>Prasad P. W. C, Azam Beg</i>	
<b>Fault Tolerance of Feed-Forward Artificial Neural Network Architectures Targeting Nano-Scale Implementations .....</b>	<b>655</b>
<i>Mehmet Vural, Ayhan Özgür, Alexandre Schmid, Yusuf Leblebici</i>	
<b>A Relocation Method for Circuit Modifications .....</b>	<b>659</b>
<i>Kunihiko Yanagibashi, Yasuhiro Takashima, Yuichi Nakamura</i>	
<b>The Analysis of Power-related Characteristics of FSM Benchmarks .....</b>	<b>663</b>
<i>Cao Cao, Bengt Oelmann</i>	
<b>Equalization in FPGA-based realization of a multicarrier modem core .....</b>	<b>667</b>
<i>Galia Marinova,, Vassil Guliashki,, Maurice Bellanger</i>	
<b>CAM Enhanced Super Parallel SIMD Processor with High-Speed Pattern Matching Capability .....</b>	<b>671</b>
<i>Takeshi Kumaki, Yutaka Kono, Masakatsu Ishizaki, Masaharu Tagami, Tetsushi Koide, Hans Jurgen Mattausch, Takayuki Gyohten, Hideyuki Noda, Yasuto Kuroda, Katsumi Dosaka, Kazutami Arimoto and Kazunori Saito</i>	
<b>Observations on Error Detection in H.264 .....</b>	<b>675</b>
<i>David Levine, William E. Lynch, Tho Le-Ngoc</i>	
<b>An Automated Technique for Image Noise Identification Using a Simple Pattern Classification Approach .....</b>	<b>679</b>
<i>Yixin Chen, Manohar Das</i>	
<b>Face Recognition for Target Detection on PCA Features with Outlier Information.....</b>	<b>683</b>
<i>Yen-Lun Chen and Yuan F. Zheng</i>	
<b>Large-Scale Tabular-Form Hardware Architecture for Q-Learning for Delays.....</b>	<b>687</b>
<i>Zhenzhen Liu, Itamar Elhanany</i>	
<b>A Low Power IC to Enable Optical Communications in a Robotic Swarm .....</b>	<b>691</b>
<i>O. Alonso, R. Casanova, A. Samy, A. Arbat, J.Canals, A. Diéguez , J. Samitier</i>	
<b>1 mW Low Power SoC for a mm3-sized Microrobot.....</b>	<b>695</b>
<i>R. Casanova, A. Dieguez, A. Arbat, O. Alonso, J. Canals, A. Samy, J. Samitier</i>	
<b>Fuzzy Control of a Carom Player.....</b>	<b>699</b>
<i>Ochoa-Luna Cristóbal, Alejos-Palomares Rubén, Vázquez-González José Luis, Navarro-Martínez Juan Antonio, Díaz-Méndez Alejandro</i>	
<b>A Parallel Architecture for Temporal Difference Learning with Eligibility Traces.....</b>	<b>708</b>
<i>J. Turnmire and I. Elhanany</i>	

# Table of Contents

<b>Fast Adder Design in Dynamic Logic</b> .....	711
<i>Victor Navarro-Botello, Juan A. Montiel-Nelson, Saeid Nooshabadi</i>	
<b>A Standby-Power-Free TCAM Based on TMR Logic</b> .....	715
<i>Kei Kimura and Takahiro Hanyu</i>	
<b>On Estimation and Optimization of Leakage Power in CMOS Multipliers</b> .....	719
<i>D. Kudithipudi, P. Nair and E. John</i>	
<b>Fundamental Concepts of Power and Energy Measurement with the Computer-Aided-Design Tools</b> .....	723
<i>Ranjith Kumar, Zhiyu Liu, and Volkan Kursun</i>	
<b>FPGA Gaussian Random Number Generator Based on Quintic Hermite Interpolation Inversion</b> .....	727
<i>Pedro Echeverria, Marisa Lopez-Vallejo</i>	
<b>Advanced Microarchitecture Simulator for Design, Verification and Synthesis</b> .....	731
<i>Aswin Ramachandran and Louis G. Johnson</i>	
<b>64-bit Pipeline Conditional Carry Adder with MTCMOS TSPC Logic</b> .....	735
<i>Shun-Wen Cheng</i>	
<b>Class AB Low-Voltage CMOS Voltage Follower</b> .....	739
<i>Ivan Padilla-Cantoya, Jesus Ezequiel Molinar-Solis, Gladis O. Ducoudary</i>	
<b>Low Energy MTCMOS with Sleep Transistor Charge Recycling</b> .....	743
<i>Zhiyu Liu and Volkan Kursun</i>	
<b>Dual-Polarity Floating Battery for Class AB Output Stages with Accurate Quiescent Current Control</b> .....	747
<i>Ivan Padilla-Cantoya</i>	
<b>A Delay Line with Highly Linear Thermal Sensitivity for Smart Temperature Sensor</b> .....	751
<i>Nguyen Thanh Trung, Kwansu Shon, Soo-Won Kim</i>	
<b>Architecture of Virus Evolutionary Genetic Algorithm for Car Navigation System</b> .....	755
<i>Masaya Yoshikawa, Hidekazu Terai</i>	
<b>Laplace Transform Approach to Analysis and Synthesis of Bessel Type Linear Time-Varying Systems</b> .....	759
<i>Nima Bayan, Shervin Erfani</i>	
<b>Alternative algorithm for low voltage operation of incremental ADCs</b> .....	764
<i>Carlos A. De La Cruz-Blas, A. Lopez-Martín and A. Carlosena</i>	
<b>A 0.9-V 10-bit 100-MSample/s Pipelined ADC Using Switched-RC and Opamp Sharing Techniques</b> .....	768
<i>Sedigheh Hashemi and Omid Shoaie</i>	
<b>A Continuous-Time Reduced-Sample-Rate .S-Pipeline ADC for Broadband Wireless Applications</b> .....	772
<i>Fuding Ge, Bahar Jalali-Farahani, Hongjiang Song, Mohammed Ismail</i>	
<b>A Digitally-Enhanced 2-0 ADC</b> .....	776
<i>Pukar Malla, Hasnain Lakdawala, Kevin Kornegay, K. Soumyanath</i>	
<b>New Energy Recovery CMOS XNOR/XOR Gates</b> .....	780
<i>Y. Xu and A. Srivastava</i>	
<b>Reducing Power in Memory Decoders by Means of Selective Precharge Schemes</b> .....	784
<i>Michael A. Turi and José G. Delgado-Frias</i>	
<b>Low-Power Bufferless Resonant Clock Distribution Networks</b> .....	788
<i>Behzad Mesgarzadeh, Martin Hansson and Atila Alvandpour</i>	
<b>Two-Phase Clocking Combined with Sleep Transistors Reduces Active Leakage in Low-Frequency Portable Applications</b> .....	792
<i>Flavio Carbognani, Felix Buergin, Norbert Felber, Hubert Kaeslin and Wolfgang Fichtner</i>	
<b>Leakage Aware Full Adder Cell</b> .....	796
<i>Dalia A.F. El-Dib and Hamed Elsimary, M.I. Elmasry</i>	

# Table of Contents

<b>Probabilistic Leakage Power Estimation of Partially-Depleted Silicon-On-Insulator (SOI) Gates .....</b>	<b>800</b>
<i>Kyung Ki Kim, and Yong-Bin Kim</i>	
<b>Hierarchical Implementation and Performance Analysis of Verilog-AMS Model of BSIM3v3.3 Transistor .....</b>	<b>804</b>
<i>Srinivasan Raghuraman, Carla Purdy</i>	
<b>A Novel Wide-Band 5.3 GHz ESD protected Input and Output Matched Low Noise Amplifier .....</b>	<b>808</b>
<i>Roghayeh Salmeh, Brent Maundy and Ronald Johnston</i>	
<b>Noise Figure Optimization of Wide-Band Inductively-Degenerated CMOS LNAs.....</b>	<b>812</b>
<i>Leonid Belostotski, , James W. Haslett</i>	
<b>Low Power Interference-Robust UWB Low Noise Amplifier in 0.18-<math>\mu</math>m CMOS Technology .....</b>	<b>816</b>
<i>Ahmed A. Youssef and James W. Haslett</i>	
<b>CMOS Mixer Enhanced for Multi-Standard Receivers.....</b>	<b>820</b>
<i>M.B. Vahidfar, O.Shoei, M.R.Hassanzadeh</i>	
<b>A Systematic System Level Design Methodology for Dual Band CMOS RF Receivers .....</b>	<b>824</b>
<i>Mohamed El-Nozahi, Kamran Entesari, and Edgar Sanchez-Sinencio</i>	
<b>Using Neural Net Architectures in Analog Circuits.....</b>	<b>828</b>
<i>Martin A. Brooke</i>	
<b>Parasitic-Aware Physical Design Optimization of Deep Sub-Micron Analog Circuits .....</b>	<b>832</b>
<i>Henry Chan and Zeljko Zilic</i>	
<b>Comparison of Two Techniques for Attenuation of Narrow-Band Interference in Spread-Spectrum Communication Systems .....</b>	<b>836</b>
<i>Michael A. Soderstrand, W. Kenneth Jenkins</i>	
<b>A New Method for Designing FIR/IIR Digital Correction Filters for Time- Interleaved Analog-to-Digital Converter Using Second Order Cone Programming.....</b>	<b>840</b>
<i>S. C. Chan, S. H. Zhao and Y. C. Lim</i>	
<b>Desensitized Halfband Interpolation Filters.....</b>	<b>844</b>
<i>Alan N. Willson</i>	
<b>Low Voltage Electrophoresis on a CMOS Chip.....</b>	<b>848</b>
<i>Heather A. Wake, Martin A. Brooke</i>	
<b>An Efficient Framework for High-Level Power Exploration .....</b>	<b>852</b>
<i>Felipe Klein, Guido Araujo, Rodolfo Azevedo, Roberto Leao, Luiz C. V. dos Santos</i>	
<b>Design-Specific Supply and Threshold Voltage Optimization in Nanometer Era .....</b>	<b>856</b>
<i>Kian Haghdad and Mohab Anis</i>	
<b>Performance Degeneration of CMOS RF Power Cells after Hot-Carrier and Load Mismatch Stresses .....</b>	<b>860</b>
<i>Chien-Hsuan Liu, Ruey-Lue Wang, Yan-Kuin Su, Chih-Ho Tu, Ying-Zong Juang</i>	
<b>Minimum Leakage Vector Pattern Estimation .....</b>	<b>864</b>
<i>V.Chinta and D.Kudithipudi</i>	
<b>Efficient Simulation of Jitter Tolerance for All-Digital Data Recovery Circuits.....</b>	<b>868</b>
<i>S. I. Ahmed, Tad A. Kwasniewski</i>	
<b>A 1.8GHz CMOS Continuous-Time Band-Pass Delta- Sigma Modulator for RF Receivers.....</b>	<b>872</b>
<i>Ali Naderi, Mohamad Sawan, Yvon Savaria</i>	
<b>DISCO - A Toolbox for the Discrete-Time Simulation of Continuous-Time Sigma-Delta Modulators Using MATLABTM .....</b>	<b>876</b>
<i>Alexander Buhmann, Matthias Keller, Michael Maurer, Maurits Ortmanns, and Yiannos Manoli</i>	

# Table of Contents

<b>An Unscented Kalman Filter for the Estimation of Circuit Nonidealities with Implicit Decimation in Continuous-Time Multibit Sigma-Delta Modulators .....</b>	<b>880</b>
<i>Alexander Buhmann, Matthias Keller, Maurits Ortmanns, and Yiannos Manoli</i>	
<b>Predicting Processor Performance with a Machine Learnt Model .....</b>	<b>884</b>
<i>Azam Beg</i>	
<b>Reducing Misprediction Penalty in the Branch Target Buffer.....</b>	<b>888</b>
<i>Sherine AbdelHak, Abhijit Sil, Yi Wang, Nian-Feng Tzeng, Magdy Bayoumi</i>	
<b>Spread Spectrum Clock Generator for reducing Electro- Magnetic Interference (EMI) Noise in LCD Driver IC .....</b>	<b>892</b>
<i>Jaehong Ko, Seungjung Lee, Doyoon Kim, Kijoon Kim, Kye-Eon Chang</i>	
<b>Standard Cell based Pseudo-Random Clock Generator for Statistical Random Sampling of Digital Signals.....</b>	<b>896</b>
<i>Rashed Zafar Bhatti, Keith M. Chugg, Jeff Draper</i>	
<b>Data Strobe Timing of DDR2 using a Statistical Random Sampling Technique .....</b>	<b>900</b>
<i>Rashed Zafar Bhatti, Monty Denneau, Jeff Draper</i>	
<b>Precise Free-Running Period Synthesizer (FRPS) with Process and Temperature Compensation .....</b>	<b>904</b>
<i>Bill Pontikakis†, François-R. Boyer, Yvon Savaria, Hung Tien Bui</i>	
<b>Large-Scale Timing-Driven Rectilinear Steiner Tree Construction in Presence of Obstacles.....</b>	<b>908</b>
<i>Hsin-Hsiung Huang, Tung-Fu Chiu, Yu-Cheng Lin, Tsai-Ming Hsieh</i>	
<b>Solution Space Reduction of Sequence Pairs using Model Placement .....</b>	<b>912</b>
<i>Yuuki Yano and Mineo Kaneko</i>	
<b>An Advanced Placement Method for SoC Floorplanning based on ACO Algorithm.....</b>	<b>916</b>
<i>Rong Luo and Peng Sun</i>	
<b>A Comparison of ILP based Global Routing Models for VLSI ASIC Design .....</b>	<b>919</b>
<i>Zhen Yang, Shawki Areibi, Anthony Vannelli</i>	
<b>Single-Channel Communication Scheme Based on Dual Synchronization of Chaos.....</b>	<b>923</b>
<i>Cheng Shen, Zhiguo Shi</i>	
<b>A Spatial Extrapolation Based Blind DOA Estimation Algorithm For Closely Spaced Sources.....</b>	<b>927</b>
<i>Feng Wan, Wei-Ping Zhu and M. N. S. Swamy</i>	
<b>Energy Efficient PWAM Transmitter Design .....</b>	<b>931</b>
<i>Rui Tang, Kyung Ki Kim, and Yong-Bin Kim</i>	
<b>A low-power 10-Gb/s 0.13-<math>\mu</math>m CMOS Transmitter for OC-192/STM-64 Applications .....</b>	<b>935</b>
<i>Jae Hoon Shim, Sangjin Byun, Jyung Chan Lee, Kwangjoon Kim, and Cheon Soo Kim</i>	
<b>Fixed Pattern Noise Correction for Wide Dynamic Range Linear-Logarithmic Pixels .....</b>	<b>939</b>
<i>Bhaskar Choubey and Steve Collins</i>	
<b>Design Considerations in MEMS Parallel Plate Variable Capacitors .....</b>	<b>943</b>
<i>Amro M. Elshurafa and Ezz I. El-Masry</i>	
<b>A Comparison of FPGA and DSP Development Environments and Performance for Acoustic Array Processing .....</b>	<b>947</b>
<i>Russ Duren, Jeremy Stevenson and Mike Thompson</i>	
<b>Rapid Optimization Of FRM Digital Filters Over CSD Multiplier Coefficient Space Using A Diversity Controlled Genetic Algorithm .....</b>	<b>951</b>
<i>Sai Mohan Kilambi and Behrouz Nowrouzian</i>	
<b>A High-Quality Mixed-Signal Audio Codec in 65-nm CMOS .....</b>	<b>955</b>
<i>Rolf Becker, Niels Haandbaek</i>	

# Table of Contents

<b>A Reliable Static-Logic-Based 16:1 Binary-Tree Multiplexer in 0.18<math>\mu</math>m CMOS .....</b>	<b>959</b>
<i>Kwansu Shon, N.T. Trung, and Soo-Won Kim, Jae-Tack Yoo</i>	
<b>Digital and mixed-signal integrated circuits for an RFID telemetry system .....</b>	<b>963</b>
<i>Christopher A. Isert, Michael C. McCoy, Douglas Jackson, and John Naber</i>	
<b>Digital Predistorter Architecture with Small Signal Gain Control for Highly Nonlinear RF Power Amplifiers .....</b>	<b>967</b>
<i>Oualid Hammi, Slim Boumaiza, and Fadhel M. Ghannouchi, Bill Vassilakis</i>	
<b>FPGA Design and Implementation of Direct Matrix Inversion Based on Steepest Descent Method.....</b>	<b>971</b>
<i>Elie H. Sarraf, Messaoud Ahmed-Ouameur, and Daniel Massicotte</i>	
<b>Data Traffic Analysis in Wireless Fusion Network with Multiple Sensors.....</b>	<b>975</b>
<i>Jinseok Lee, Sangkil Jung, Yuntai Kyong, Xi Deng, Sangjin Hong and We-Duke Cho</i>	
<b>Passive Sensor Based Dynamic Object Association Method in Wireless Sensor Networks .....</b>	<b>979</b>
<i>Shung Han Cho, Jinseok Lee, Xi Deng, Sangjin Hong and We-Duke Cho</i>	
<b>Design and Implementation of an Adaptive Multiuser Detector for Multirate WCDMA Systems.....</b>	<b>983</b>
<i>Quoc-Thai Ho and Daniel Massicotte</i>	
<b>Novel PSK Enumeration for Efficient VLSI Implementation of MIMO Detection.....</b>	<b>987</b>
<i>Sudip Mondal, Sandeep Krishnegowda, Khaled N Salama and Tong Zhang</i>	
<b>Design and Analysis of a 6-stage Tunable MZI PLC for BPSK Generation .....</b>	<b>991</b>
<i>A. Jain, I. A. Kostko, L. R. Chen, B. Xia, P. Dumais, C. L. Callender</i>	
<b>Experimental Setup for the Measurement of Local Temperature in Electronic Component during the Steady and Transient State .....</b>	<b>995</b>
<i>Sonia Dhokkar, Patrick Iagonotte, André Piteau</i>	
<b>Design of Optical Range Third-Order Chebychev Low-Pass Filter Using Plasmonic Nanostrip Waveguides.....</b>	<b>999</b>
<i>Amir Hosseini, Hamid Nejati, and Yehia Massoud</i>	
<b>Impedance Formulation of Single Oscillating Nanospheres at Optical Frequencies.....</b>	<b>1003</b>
<i>Mehboob Alam, Amir Hosseini, and Yehia Massoud</i>	
<b>Metal-Insulator-Metal Based Two-Dimensional Triangular Lattice Photonic Band-Gap Structure .....</b>	<b>1007</b>
<i>Amir Hosseini, Hamid Nejati, and Yehia Massoud</i>	
<b>Multi-core Image Processing System using Network on Chip Interconnect .....</b>	<b>1011</b>
<i>Jonathan Joshi, Kedar Karandikar, Sharad Bade, Mandar Bodke, Rohan Adyanthaya, Balkrishan Ahirwal</i>	
<b>A Novel Clock Deskew Method by Linear Programming .....</b>	<b>1015</b>
<i>Yuko Hashizume, Yasuhiro Takashima, Yuichi Nakamura</i>	
<b>High-Level Optimization for Low Power Consumption on Microprocessor-Based Systems .....</b>	<b>1019</b>
<i>David A. Ortiz, Nayda G. Santiago</i>	
<b>A Hardware/Software Cooperative Approach for Reducing Memory Traffic in Application-specific Instruction Set Processors.....</b>	<b>1023</b>
<i>Yunsi Fei, Hai D. Lin, Xuan Guan</i>	
<b>Low-Power and Low-Complexity Architecture for H.264/AVC video decoder.....</b>	<b>1027</b>
<i>Li-Hsun Chen and Oscar T.-C. Chen</i>	
<b>A Low-Power Adiabatic Content-Addressable Memory.....</b>	<b>1031</b>
<i>Sheng Zhang, Jianping Hu, and Dong Zhou</i>	
<b>A 0.5V High Speed DRAM Charge Transfer Sense Amplifier .....</b>	<b>1035</b>
<i>Hwang-Cherng Chow and Chaung-Lin Hsieh</i>	

# Table of Contents

<b>Adaptive SRAM Design for Dynamic Voltage Scaling VLSI Systems .....</b>	<b>1039</b>
<i>Sami Kirolos and Yehia Massoud</i>	
<b>Large Temperature Coefficient PTAT Current Reference using Weak Inversion CMOS FET Resistor .....</b>	<b>1043</b>
<i>Seunghwan Baek, Hyungtae Kim, Changhwee Choi, Seungkwon Lee and Kye_eon Chang</i>	
<b>Rapid Algorithm Verification for Cooperative Analog-Digital Imaging Systems .....</b>	<b>1047</b>
<i>Teahyung Lee, Leung Kin Chiu, David V. Anderson, Ryan Robucci, and Paul Hasler</i>	
<b>Fast Estimation of Interconnects Delay in RLC Trees Using Neural Network.....</b>	<b>1051</b>
<i>Fahimeh Alsadat Hoseini, Nasser Masoumi</i>	
<b>Delay and Slew Analysis of VLSI Interconnects using Difference Model Approach.....</b>	<b>1055</b>
<i>J.V.R.Ravindra, M.B.Srinivas</i>	
<b>Analysis of Current-to-Data Dependency in Asynchronous Cryptographic Circuits .....</b>	<b>1058</b>
<i>Radu Muresan and Stefano Gregori</i>	
<b>General Purpose Serial Processor for Delta Sigma ADC Digital Filter .....</b>	<b>1062</b>
<i>Xin Cai and Martin A. Brooke</i>	
<b>An IEEE 802.11a Baseband Receiver Implementation on an Application Specific Processor .....</b>	<b>1066</b>
<i>S. Eberli , A. Burg , T. Bösch, and W. Fichtner</i>	
<b>Designing CMOS Hardware Processor for Vehicle Tracking .....</b>	<b>1070</b>
<i>Hua Tang, Taek Mu Kwon, Yi Zheng, Hairong Chang</i>	
<b>A Low Power CMOS CORDIC Processor Design for Wireless Telecommunication.....</b>	<b>1074</b>
<i>Young Bok Kim, Yong-Bin Kim, James T. Doyle</i>	
<b>Compression and Encryption of Self-test Programs for Wireless Sensor Network Nodes .....</b>	<b>1078</b>
<i>Bojan Mihajlovic, Željko Žilic, Katarzyna Radecka</i>	
<b>High Frequency Channel Noise Measurement and Characterization in Deep Submicron MOSFETs.....</b>	<b>1082</b>
<i>A. Allam, I. M. Filanovsky</i>	
<b>Delay Faults in Dual-Rail, Self-Reset Wave-Pipelined Circuits .....</b>	<b>1086</b>
<i>Amjed Al-Mousa, Samiha Mourad</i>	
<b>High-Precision Delay Testing of Virtex-4 FPGA Designs .....</b>	<b>1090</b>
<i>Jack Smith, Tian Xia</i>	
<b>Systematic Approach to the Synthesis of Continuous-Time Cascaded Sigma-Delta Modulators .....</b>	<b>1094</b>
<i>Matthias Keller, Alexander Buhmann, Maurits Ortmanns, Yiannos Manoli</i>	
<b>A 1.8 V 64 MHz Delta-Sigma Modulator for Wideband and Multi-Standard Applications.....</b>	<b>1098</b>
<i>Y. Y. Du, Kei-Tee Tiew</i>	
<b>A Low-Distortion Two-path Fourth-order Bandpass Delta-Sigma Modulator Using Horizontal Opamp Sharing.....</b>	<b>1102</b>
<i>Naoya Waki, Hiroki Sato, Akira Hyogo, and Keitaro Sekine</i>	
<b>Fast Decoding Algorithm for First Order DC-Input Sigma-Delta Modulators .....</b>	<b>1106</b>
<i>E. Ghafar-Zadeh, M. Sawan,, M.A. Miled</i>	
<b>A Frequency Counter Based Analog-to-Digital Converter for a RFID Telemetry System.....</b>	<b>1110</b>
<i>Michael Calvin McCoy, Christopher Isert, Douglas Jackson, John Naber</i>	
<b>Integrated Test Scheduling, Wrapper Design, and TAM Assignment for Hierarchical SOC .....</b>	<b>1114</b>
<i>Haidar M. Harmanani and Rana Farah</i>	
<b>On A Web-Graph-Based Micronetwork Architecture for SoCs .....</b>	<b>1118</b>
<i>Ling Wang, Shouye Piao, Yingtao Jiang, Juyeon Jo, Lihong Zhang</i>	
<b>Analysis of Subthreshold Leakage Reduction in CMOS Digital Circuits.....</b>	<b>1122</b>
<i>Boray S. Deepaksubramanyan, Adrian Nuñez</i>	

# Table of Contents

<b>Dual Diode-Vth Reduced Power Gating Structure for Better Leakage Reduction .....</b>	<b>1127</b>
<i>Pervez Khaled, Jingye Xu, Masud H. Chowdhury</i>	
<b>An Efficient Stochastic Integral Equation Method for Modeling the Influence of Conductor Surface Roughness on Interconnect Ohmic Loss.....</b>	<b>1131</b>
<i>Quan Chen and Ngai Wong</i>	
<b>A Finite Element-Domain Decomposition Coupled Resistance Extraction Method with Virtual Terminal Insertion.....</b>	<b>1135</b>
<i>Bo Yang and Hiroshi Murata</i>	
<b>Model-Order Reduction of Frequency-Dependent Interconnects based on Integrated Congruence Transform.....</b>	<b>1139</b>
<i>Changzhong Chen, Michel Nakhla and Ram Achar, Emad Gad</i>	
<b>Feasible Assignment of Wire-Bonding Power Pads in Hierarchical Power Quad-Grids for Signal Integrity .....</b>	<b>1143</b>
<i>Jin-Tai Yan, Zhi-Wei Chen and Chun-Yu Kuo</i>	
<b>A 212 Mb/s Chip for 4 × 4 16-QAM V-BLAST Decoder .....</b>	<b>1147</b>
<i>Fariborz Sobhanmanesh and Saeid Nooshabadi, Kiseon Kim</i>	
<b>Low-Noise CMOS Active Transformer Voltage-Controlled Oscillators .....</b>	<b>1151</b>
<i>A. Tang, F. Yuan, and E. Law</i>	
<b>A <math>\Delta\Sigma</math> Modulator Based Frequency Hopping Approach.....</b>	<b>1155</b>
<i>Innes Cathcart, Haizheng Guo and Robert Sobot, Shawn Stapleton</i>	
<b>A New Parallel Link Interface with Current-Mode Incremental Signaling and Per-Pin Skew Compensation.....</b>	<b>1159</b>
<i>An Hu and Fei Yuan</i>	
<b>Design Trade-offs for Load/Store Buffers in Embedded Processing Environments.....</b>	<b>1163</b>
<i>Young Hoon Kang, Jeffrey Draper</i>	
<b>ASIC Design for the Efficient Computation of Line Spectral Frequencies Using Chebyshev Polynomial Series .....</b>	<b>1167</b>
<i>David L. Reynolds, Linda M. Head, Ravi P. Ramachandran</i>	
<b>Partially-Parallel Irregular LDPC Decoder based on Improved Message Passing Schedule .....</b>	<b>1171</b>
<i>Xing Li, Kazunori Shimizu, Zhen Qiu, Takeshi Ikenaga, Satoshi Goto</i>	
<b>Sinusoidal RF DACs for Undersampled LC Bandpass Modulators .....</b>	<b>1175</b>
<i>Nicolas Beilleau, Cyrius Ouffoue and Hassan Aboushady</i>	
<b>A Charge Steering Type Digital Analog Converter .....</b>	<b>1179</b>
<i>Junko Ikari and Shinji Nakamura, Yasuo Nagazumi</i>	
<b>Automatic Generation of ModelSim-Matlab Interface for RTL Debugging and Verification .....</b>	<b>1183</b>
<i>Brian Gestner and David V. Anderson</i>	
<b>METASIS: A Meta Heuristic Based Logic Optimizer.....</b>	<b>1187</b>
<i>Gyan Ranjan, Pankaj Kumar, Prosenjit Gupta</i>	
<b>A New Scheduling Algorithm for Processor-Based Logic Emulation Systems .....</b>	<b>1191</b>
<i>Amir Yazdanshenas and Mohammed A. S. Khalid</i>	
<b>Partitioning Exploration for Automated Mapping of Discrete Cosine Transforms onto Distributed Hardware Architectures.....</b>	<b>1195</b>
<i>Rafael A. Arce-Nazario, Manuel Jimenez, and Domingo Rodriguez</i>	
<b>0.18<math>\mu</math>m CMOS 9mW Current-Mode FLF Linear Phase Filter with Gain Boost.....</b>	<b>1199</b>
<i>Xi Zhu, Yichuang Sun, and James Moritz</i>	
<b>A New Bang-Bang Phase/Frequency Detector for Fast Locking of Phase-Locked Loops.....</b>	<b>1203</b>
<i>Jiwang Li and Fei Yuan</i>	



# Table of Contents

<b>Pulse Coupled Oscillator Synchronization for Low Power UWB Wireless Transceivers .....</b>	<b>1206</b>
<i>Xiao Y. Wang and Alyssa B. Apsel</i>	
<b>CMOS Active Transformer Current-Mode Phase-Locked Loops .....</b>	<b>1210</b>
<i>D. DiClemente, F. Yuan, and A. Tang</i>	
<b>Design and Implementation of an All-Analog Fast- Fourier Transform Processor.....</b>	<b>1214</b>
<i>Keith Boyle, Pat Mercier, Nima Sadeghi, Vincent Gaudet, Christian Schlegel, Chris Winstead, Manohar Kashyap</i>	
<b>Acoustic Target Localization in Sensor Networks with FUZZYART.....</b>	<b>1218</b>
<i>Zaher Merhi, Mohamed Elgamel, Magdy Bayoumi</i>	
<b>Nontraditional Signal Processing Techniques Employing Linear Transforms.....</b>	<b>1222</b>
<i>Wasfy B. Mikhael, Pradeep Ragothaman, and Moataz M. Abdelwahab</i>	
<b>From (Integrated) Circuits to Systems of Systems on Chip in Five Decades How did and will (IC) Test Technology keep up? .....</b>	<b>1224</b>
<i>André Ivanov</i>	
<b>Low-Power Integrated CMOS RF Transceiver Circuits for Short-Range Applications .....</b>	<b>1226</b>
<i>M. Jamal Deen, Munir M. El-Desouki, Hamed M. Jafari and Saman Asgaran</i>	
<b>A New Direction in Integrated Circuit Technology .....</b>	<b>1232</b>
<i>Akira Matsuzawa</i>	