

# **2007 IEEE Workshop on Signal Propagation on Interconnects**

**Ruta di Camogli, Italy  
13-16 May 2007**



**IEEE Catalog Number:** CFP07SPI-PRT  
**ISBN 10:** 1-4244-1223-4  
**ISBN 13:** 978-1-4244-1223-5

# Table of Contents

## Keynote Speech I

### ***Designing for Energy Efficient Mobile Platforms***

- T. R. Arabi, A. Muhtaroglu, G. Taylor\*  
Mobile Platform Architecture Development, \*Logic Technology Development  
Intel Corporation, USA ..... 1

## Session I – On-Chip Interconnects I

### ***Effect of Noise on Timing or Data-Pattern Dependent Delay Variation***

### ***When Transmission-Line Effects are Taken Into Account for On-Chip Wiring***

- A. Deutsch, H. H. Smith\*, C. Vakirtzis\*, J. Kozhaya\*\*, L. M. Greenberg\*  
IBM T. J. Watson Research Center, USA, \*IBM Systems and Technology Group, Poughkeepsie, NY,  
\*\*IBM Systems and Technology Group, Burlington, VT ..... 7

### ***Spice-Accurate SystemC Macromodels of Noisy On-Chip Communication Channels***

- N. Terrassan, D. Bertozzi, A. Bogliolo\*  
University of Ferrara, Italy, \*University of Urbino, Italy ..... 11

### ***Equalization of Interconnect Propagation Delay with Negative Group Delay Active Circuits***

- B. Ravelo, A. Pérennec, M. Le Roy  
LEST, France ..... 15

## Session II – On-Chip Interconnects II

### ***Silicon-chip Single and Coupled Coplanar Transmission Line Measurements and Model Verification up to 50GHz***

- D. Goren, S. Shlafman, B. Sheinman, W. Woods\*, J. Rascoe\*  
IBM Haifa Research Labs, Israel, \*IBM Burlington Design Enablement, USA ..... 21

### ***Comparison of the benefits, from SiO<sub>2</sub> to ultralow-K dielectric and air spacing introduction, in term of interconnects performances, for the future high speed IC's in a multicoupled lines system***

- F. Ponchel, J.F. Legier, E. Paleczny, C. Seguinot, D. Deschacht\*  
IEMN, France, \*LIRMM, France ..... 25

### ***Comparison Between Metallic Carbon Nanotube and Copper Future VLSI Nano-interconnects***

- A. Maffucci, G. Miano\*, F. Villone  
University of Cassino, Italy, \*University of Napoli "Federico II", Italy ..... 29

## Session 3 – Transmission Lines and High-Speed Channels I

### ***Effect of Uncertainties in the Cross-Sectional Parameters on the Wideband Electrical Properties of Coplanar Waveguides***

J. Leinhos, U. Arz  
PTB, Germany ..... 35

### ***Interconnect Length Impact Investigation by Measurements***

M. Sotman, A. Kostinsky, G. Zobin  
Intel, Israel ..... 39

## Session 4 – Macromodeling by Vector Fitting

### ***Broadband Macromodeling of Sampled Frequency Data Using z-domain Vector-Fitting Method***

Y. S. Mekonnen, J. E. Schutt-Ainé  
University of Illinois at Urbana-Champaign, USA ..... 45

### ***Rational Modeling of Multiport Systems by Modal Vector Fitting***

B. Gustavsen, C. Heitz<sup>\*</sup>  
SINTEF, Norway, \*Institut für Datenanalyse und Prozessdesign, Switzerland ..... 49

### ***Macromodeling of Transfer Functions with Higher-Order Pole Multiplicities***

D. Deschrijver, T. Dhaene, Y. Rolain<sup>\*</sup>  
University of Antwerp, Belgium, \*Vrije Universiteit Brussels, Belgium ..... 53

### ***Well-conditioned Adaptive Interpolation by a Gaussian-Modulated Pole Kernel with Applications to Vector Fitting***

L. Knockaert, D. De Zutter  
Ghent University, Belgium ..... 57

## Keynote Speech II

### ***Future mobile device interconnections***

M. Voutilainen  
Nokia, Finland ..... 63

## Session 5 – Linear Macromodeling I

### ***Model Order Reduction of Large Multiport Interconnect Structures using Waveform Relaxation Techniques***

N. Nakhla , M. Nakhla, R. Achar  
Carleton University, Canada ..... 69

## ***Fast Passivity Enforcement of Rational Macromodels by Perturbation of Residue Matrix Eigenvalues***

B. Gustavsen  
SINTEF, Norway ..... 71

## ***On relative error minimization in passivity enforcement schemes***

S. Grivet-Talocia, A. Ubolli  
Politecnico di Torino, Italy ..... 75

## **Session 6 – Linear Macromodeling II**

### ***Stable model order reduction method using Kautz functions: application to VLSI circuits***

M. Telescu, P. Bréhonnet, N. Tanguy, P. Vilbé  
LEST, France ..... 81

### ***Removing Redundancy in Interconnect Simulation using Domain Decomposition Techniques***

V. Ambalavanar, A. Jerome, P. Gunupudi  
Carleton University, Canada ..... 85

### ***Fast Automatic Order Estimation of Rational Macromodels for Signal Integrity Analysis***

N. Stevens, D. Deschrijver\*, T. Dhaene\*  
Agilent Technologies, USA, \*University of Antwerp, Belgium ..... 89

## **Session 7 – Transmission Lines and High-Speed Channels II**

### ***Frequency domain analysis of transmission zeroes on high-speed interconnects in the presence of an orthogonal metal grid underlayer***

Y. Quéré, T. Le Gouguec, P.M. Martin, D. Le Berre, F. Huret  
LEST, France ..... 95

### ***Determination of Transmission Line Parameters in Time- and Frequency Domain for Product Related Packaging Structures***

T.M. Winkel, A. Deutsch\*, G.A. Katopis\*\*, G. V. Kopcsay\*, W. D. Dyckman\*\*, B.J. Chamberlin\*\*,  
C. W. Surovic\*, H. Liu\*\*, C. Baks\*  
IBM Entwicklungs GmbH, Böblingen, Germany, \*IBM T J Watson Research Center, USA,  
\*\*IBM System and Technology Group, USA ..... 99

### ***Signal Propagation Over Perforated Reference Planes***

L. Shan, M. Ritter, A. Haridass, R. Weekly, D. Becker, E. Klink  
IBM T J Watson Research Center, USA ..... 103

## Session 8 – Interconnect Characterization

### ***Characterization of Electromagnetic Leakages throughout the Connector Shell***

Y. Bouri, L. Koné\*, J. Razafiarivelo, D. Baudry\*\*, S. Baranowski\*, B. Démoulin\*  
FCI, Corporate Research Center, France, \*University of Sciences and Technologies of Lille, France,  
\*\*IRSEEM, France ..... 109

### ***Characterization of Flexible Interconnects in Mobile Devices***

P. Kotiranta, I. Kelander, M. Rouvala, J. Takaneva  
Nokia, Finland ..... 113

### ***Considerations on Impedance Matrix Determination for Accurate Passive Device Characterization***

M. Wojnowski, M. Engl, R. Weigel\*  
Infineon Technologies AG, Germany, \*University of Erlangen-Nuremberg, Germany ..... 117

### ***Fundamentals of a 3-D “Snowball” Model for Surface Roughness Power Losses***

P. G. Huray, S. Hall\*, S. Pytel\*, F. Oluwafemi\*, R. Mellitz\*, D. Hua\*, P. Ye\*  
University of South Carolina, USA, \*INTEL, USA ..... 121

## Session 9 – Optical Interconnects

### ***Coupling and Signal Propagation Model of Multimode Waveguides with Rough Core-Cladding Interfaces***

K. Halbe, I. Roda, E. Griese  
University of Siegen, Germany ..... 127

### ***Prospects of a Polymer-Waveguide-Based Board-Level Optical Interconnect Technology***

R. Dangel, C. Berger, R. Beyeler, L. Dellmann, F. Horst, T. Lamprecht, N. Meier, B. J. Offrein  
IBM Research GmbH, Switzerland ..... 131

### ***Preserving Signal Integrity in a SOA-based De-Multiplexer used in OTDM interconnections***

C. Crognale, V. Ricchiuti, S. Caputo\*, S. Saracino\*\*  
TechnoLabs S.p.A., Italy, \*SMD Elettronica, Italy, \*\*Siemens S.p.A., Italy ..... 135

## Session 10 – 3D Modeling

### ***Fast FDTD Simulation of Multiscale 3D Models Using Laguerre-MNA***

K. Srinivasan, E. Engin, M. Swaminathan  
Georgia Institute of Technology, USA ..... 141

### ***Progress in Representation and Validation of Physics-Based Via Models***

C. Schuster, G. Sellin\*, Y. H. Kwark\*\*, M. B. Ritter\*\*, J. L. Drewniak\*  
Technical University of Hamburg-Harburg, Germany, \*University of Missouri-Rolla, USA  
\*\*IBM T J Watson Research Center, USA ..... 145

## **Accurate Capacitance Extraction in the Entire Package Model Using A Parallel Kernel Independent Hierarchical Extractor**

K. Butt, I. Jeffrey, M. Al-Qedra, F. Ling\*, V. Okhmatovski

University of Manitoba, Canada, \*Cadence Design Systems, USA .....

149

## **Session 11 – Packaging and Power Integrity**

### **Toward a Systematic Sensitivity Analysis of On-Chip Power Grids Using Factor Analysis**

D. A. Andersson, L. J Svensson, P. Larsson-Edefors

Chalmers University of Technology, Sweden ..... 155

### **A simple filtering approach to improve the return loss of a PCB to DIE transition trough a PBGA package for over GHz applications**

J.R. Cubillo, J. Gaubert, S. Bourdel, H. Barthélémy, P. Pannier

L2MP, France ..... 159

### **Interconnection effects in Package on Package design**

P. Pulici, G. Candela\*, G. Campardo, G. P. Vanalli, P. P. Stoppino, A. Losavio, T. Lessio, M. Dellutri, D. Guarnaccia, F. Lo Iacono

STMicroelectronics, Italy, \*Politecnico di Milano, Italy ..... 163

## **Poster Session A - Modeling and Analysis of Interconnects**

### **Robust Passivity Enforcement of Frequency Dependent Transmission Line Models**

B. Gustavsen

SINTEF, Norway ..... 169

### **Modeling Propagation Characteristics of Multimode Graded-Index Waveguides with Finite Elements using Edge-Based Elements**

T. Kuehler, E. Griese

University of Siegen, Germany ..... 173

### **Modeling of Electromagnetic Effects in Complete RF blocks**

J. Niehof, H.H.J.M. Janssen, W.H.A. Schilders

NXP Semiconductors Research, The Netherlands ..... 177

### **Application of Measured Twinax Cable S-Parameters**

Z. Chen

IBM Corporation, USA ..... 179

### **The Low-Loss Interconnects Simulation by Perturbation Methods**

A. Ligocka, W. Bandurski

Poznań University of Technology, Poland ..... 182

**An Absolutely-Stable Arbitrarily high-order Implicit Numerical Integration Method and its application to the Time-Domain Simulation of Interconnect Circuits**

E. Gad, M. Nakhla\*, R. Achar\*, Y. Zhou\*  
University of Ottawa, Canada, \*Carleton University, Ottawa, Canada ..... 186

**Skew and EMI Management in Differential Microstrip Lines up to 15GHz**

M. R. Burford, P. A. Levin\*, T. J. Kazmierski  
University of Southampton, UK, \*Xyratech Technology Ltd, UK ..... 188

**Differential Insertion Loss and Deterministic Jitter for Different Types of Differential Transmission Lines in High-Speed Serial Backplane Bus**

H. Osaka, Y. Uematsu, K. Yamamoto, H. Kanai, N. Chujo  
Hitachi Ltd., Japan ..... 192

**Crosstalk Timing Model for High-Speed Interconnects with Impedance Discontinuity**

A. Kuo, A. Labun\*, N. Swart\*, A. Ivanov  
University of British Columbia, Canada, \*University of British Columbia Okanagan, Canada ..... 194

**Calculation of Crosstalks in Multiple-Conductor Cables**

B. M. Levin  
Lod, Israel ..... 198

**Evaluation of the propagation constants of differential PCB Interconnections**

V. Ricchiuti, A. Orlandi\*, G. Antonini\*  
TechnoLabs S.p.A., Italy, \*University of L'Aquila, Italy ..... 202

## **Poster Session B – Chip, Packaging and Material Issues**

**Fast Calculation of PEEC Macromodels using Frequency Derivatives**

D. Deschrijver, G. Antonini\*, T. Dhaene  
University of Antwerp, Belgium, \*University of L'Aquila, Italy ..... 209

**Electromagnetic Coupling Analysis of High Density Bent Interconnects**

S. Ghosh, A. Roy, A. Chakrabarty  
Indian Institute of Technology, India ..... 213

**Analytical Calculation of the Point-to-Point Partial Inductance of a Perfect Ground Plane**

U. Paoletti, T. Hisakado, O. Wada  
Kyoto University, Japan ..... 217

**Analytical Crosstalk Model with Inductive Coupling in VLSI Interconnects**

J.V.R. Ravindra, M.B. Srinivas  
International Institute of Information Technology (IIIT), India ..... 221

**RLC Crosstalk Calculation with Dissymmetrical Attacks**

J.E. Lorival, D. Deschacht  
LIRMM, France ..... 225

<b>Dielectric Modeling, Characterization, and Validation up to 40 GHz</b>	
S. G. Pytel, G. Barnes, D. Hua, A. Moonshiram, G. Brist, R. I. Mellitz, S. H. Hall, P. G. Huray*	
Intel Corporation, USA, *University of South Carolina, USA .....	229
<b>Reduced Order Models for HF Interconnect over Lossy Semiconductor Substrate</b>	
D. Ioan, G. Ciuprina, S. Kula	
Politehnica University of Bucharest, Romania .....	233
<b>Power supply noise investigation of a multilayered IC package: full wave simulation and model validation</b>	
A. Ciccomancini Scogna, C. Ritota*	
CST of America, USA, *Tiesse, Italy .....	237
<b>Measurement of Interconnect Loss Due to Dummy Fills</b>	
A. Tsuchiya, H. Onodera	
Kyoto University, Japan .....	241
<b>Impact of Process Variations on Bus-Encoding Schemes for Delay Minimization in VLSI Interconnects</b>	
C. Raghunandan, K. S. Sainarayanan, M. B. Srinivas	
International Institute of Information Technology (IIIT), India .....	245