

2008 IEEE WORKSHOP
ON
SIGNAL PROCESSING SYSTEMS

SIPS 2008

Proceedings

OCTOBER 8–10, 2008
WASHINGTON, D.C. METRO AREA, U.S.A.



SPONSORED BY

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
IEEE SIGNAL PROCESSING SOCIETY
IEEE CIRCUITS AND SYSTEMS SOCIETY

TABLE OF CONTENTS

L-Arch: DSP ARCHITECTURES

L-Arch.1: A HIGHLY PARALLEL TURBO PRODUCT CODE DECODER1 WITHOUT INTERLEAVING RESOURCE

Camille Leroux, Christophe Jego, Patrick Adde, Michel Jezequel, Deepak Gupta, Institut TELECOM, TELECOM Bretagne, France

L-Arch.2: A DIGIT-SERIAL ARCHITECTURE FOR INVERSION AND7 MULTIPLICATION IN GF(2M)

Junfeng Fan, Ingrid Verbauwhede, Katholieke Universiteit Leuven, Belgium

L-Arch.3: UNIFIED DECODER ARCHITECTURE FOR LDPC/TURBO13 CODES

Yang Sun, Joseph Cavallaro, Rice University, United States

L-Arch.4: EFFICIENT INTERPOLATION ARCHITECTURE FOR19 SOFT-DECISION REED-SOLOMON DECODING BY APPLYING SLOW-DOWN

Xinmiao Zhang, Jiangli Zhu, Case Western Reserve University, United States

L-Arch.5: A 100MHZ REAL-TIME TONE MAPPING PROCESSOR WITH25 INTEGRATED PHOTOGRAPHIC AND GRADIENT COMPRESSION IN 0.13 UM TECHNOLGY

Ching-Te Chiu, Tsun-Hsien Wang, Wei-Ming Ke, Chen-Yu Chuang, Jih-Siao Huang, Wei-Su Wong, Ren-Song Tsay, National Tsing Hua University, Taiwan

L-Arch.6: A UNIFIED INSTRUCTION SET PROGRAMMABLE31 ARCHITECTURE FOR MULTI-STANDARD ADVANCED FORWARD ERROR CORRECTION

Frederik Naessens, Bruno Bougard, Siebert Bressinck, Lieven Hollevoet, Praveen Raghavan, Liesbet Van der Perre, Francky Catthoor, IMEC, Belgium

PS-1: POSTER SESSION 1

PS-1.1: A METHOD FOR IMPROVING THE EFFICIENCY OF A37 TWO-LEVEL MEMORY HIERARCHY

Radomir Jakovljevic, University of Belgrade, Yugoslavia; Aleksandar Beric, Silicon Hive, Netherlands

PS-1.3: HARDWARE ACCELERATION FOR TRACKING BY COMPUTING43 LOW-ORDER GEOMETRICAL MOMENTS

Julien A. Vijverberg, Eindhoven University of Technology, Netherlands; Peter H.N. de With, Eindhoven University of Technology/ CycloMedia Technology B.V., Netherlands

PS-1.4: EFFICIENT IMAGE RECONSTRUCTION USING PARTIAL 2D49 FOURIER TRANSFORM

Lanping Deng, Chi-Li Yu, Chaitali Chakrabarti, Arizona State University, United States; Jungsub Kim, Vijay Narayanan, Pennsylvania State University, United States

PS-1.5: PARALLEL CHANNEL INTERLEAVERS FOR 3GPP2/UMB	55
<i>Mohammad Mansour, QUALCOMM Inc., United States</i>	
PS-1.6: NEW SIMPLIFIED SUM-PRODUCT ALGORITHM FOR LOW	61
COMPLEXITY LDPC DECODING	
<i>Myung Hun Lee, Jae Hee Han, Myung Hoon Sunwoo, Ajou University, Republic of Korea</i>	
PS-1.7: A SYSTOLIC ARCHITECTURE OF A SEQUENTIAL MONTE	67
CARLO-BASED EQUALIZER FOR FREQUENCY-SELECTIVE MIMO CHANNELS	
<i>Mahdi Shabany, P. Glenn Gulak, University of Toronto, Canada</i>	
PS-1.8: LOCATION-CONSTRAINED PARTICLE FILTER FOR RSSI-BASED	73
INDOOR HUMAN POSITIONING AND TRACKING SYSTEM	
<i>Chih-Hao Chao, Chun-Yuan Chu, An-Yeu Wu, National Taiwan University, Taiwan</i>	
PS-1.9: COOPERATIVE OFDM FOR ENERGY-EFFICIENT WIRELESS	77
SENSOR NETWORKS	
<i>Weiguo Tang, Lei Wang, University of Connecticut, United States</i>	
PS-1.10: HIGH-THROUGHPUT DUAL-MODE SINGLE/DOUBLE BINARY	83
MAP PROCESSOR DESIGN FOR WIRELESS WAN	
<i>Chun-Yu Chen, Cheng-Hung Lin, An-Yeu (Andy) Wu, National Taiwan University, Taiwan</i>	
PS-1.11: TRADE-OFF ANALYSIS OF DECODING ALGORITHMS AND	88
ARCHITECTURES FOR MULTI-STANDARD LDPC DECODER	
<i>Robert Priewasser, Klagenfurt University, Austria; Bruno Bougard, IMEC, Belgium; Mario Huemer, Klagenfurt University, Austria</i>	
 L-CC: CODING AND COMMUNICATIONS	
L-CC.1: ERROR CORRECTION FOR MULTI-LEVEL NAND FLASH	94
MEMORY USING REED-SOLOMON CODES	
<i>Bainan Chen, Xinmiao Zhang, Case Western Reserve University, United States; Zhongfeng Wang, Broadcom Corporation, United States</i>	
L-CC.2: IMPACT OF ROUND-OFF ERROR ON THE DECISIONS OF THE	100
LOG SUM-PRODUCT ALGORITHM FOR LDPC DECODING	
<i>Nikos Kanistras, Vassilis Paliouras, University of Patras, Greece</i>	
L-CC.3: TWO-DIMENSIONAL CROSSTALK AVOIDANCE CODES	106
<i>Xuebin Wu, Zhiyuan Yan, Lehigh University, United States; Yuan Xie, Pennsylvania State University, United States</i>	
L-CC.4: MULTI-MODE SUB-NYQUIST RATE DIGITAL-TO-ANALOG	112
CONVERSION FOR DIRECT WAVEFORM SYNTHESIS	
<i>Stanley Yuan-Shih Chen, Nam-Seog Kim, Jan M. Rabaey, University of California, Berkeley, United States</i>	
L-CC.5: AN IMPLEMENTATION FRIENDLY LOW COMPLEXITY	118
MULTIPLIERLESS LLR GENERATOR FOR SOFT MIMO SPHERE DECODERS	
<i>Min Li, David Novo, Bruno Bougard, Frederik Naessens, Liesbet Van Der Perre, Francky Catthoor, IMEC, Belgium</i>	

L-CC.6: REDUCED-COMPLEXITY MSGR-BASED MATRIX INVERSION.....	124
<i>Lei Ma, Kevin Dickson, John McAllister, John McCanny, Mathini Sellathurai, Institute of Electronics, Communications and Information Technology, Queen's University, Belfast, United Kingdom</i>	
 L-AS: APPLICATION-SPECIFIC HARDWARE AND SOFTWARE TECHNIQUES	
L-AS.1: KALMAN FILTERING BASED MOTION ESTIMATION FOR VIDEO CODING WITH ADAPTIVE BLOCK PARTITIONING	129
<i>Yi Luo, Mehmet Celenk, Ohio University, United States</i>	
L-AS.2: FAST MULTIPLE REFERENCE FRAME SELECTION METHODS FOR H.264/AVC	135
<i>Wang Ho Shin, Sung Dae Kim, Myung Hoon Sunwoo, Ajou university, Republic of Korea</i>	
L-AS.3: MINIMAL COMPLEXITY LOW-LATENCY ARCHITECTURES FOR VITERBI DECODERS	140
<i>Renfei Liu, Keshab Parhi, University of Minnesota, Twin Cities, United States</i>	
L-AS.4: EFFICIENT ORDERING SCHEMES FOR SPHERE DECODER	146
<i>Yongmei Dai, Zhiyuan Yan, Lehigh University, United States</i>	
L-AS.5: ANALYSIS OF BELIEF PROPAGATION FOR HARDWARE REALIZATION	152
<i>Chao-Chung Cheng, Chia-Kai Liang, Yen-Chieh Lai, Homer Chen, Liang-Gee Chen, National Taiwan University, Taiwan</i>	
L-AS.6: BIO-INSPIRED UNIFIED MODEL OF VISUAL SEGMENTATION SYSTEM FOR CAPTCHA CHARACTER RECOGNITION	158
<i>Chi-Wei Lin, Yu-Han Chen, Liang-Gee Chen, National Taiwan University, Taiwan</i>	
 PS-2: POSTER SESSION 2	
PS-2.1: VIDEO DECODER RECONFIGURATIONS AND AVS EXTENSIONS IN THE NEW MPEG RECONFIGURABLE VIDEO CODING FRAMEWORK	164
<i>Dandan Ding, Zhejiang University, China; Christophe Lucarz, Marco Mattavelli, Ecole Polytechnique Fédérale de Lausanne, Switzerland; Lu Yu, Zhejiang University, China</i>	
PS-2.2: ON THE VERIFICATION OF MULTI-STANDARD SOC'S FOR RECONFIGURABLE VIDEO CODING BASED ON ALGORITHM/ARCHITECTURE CO-EXPLORATION	170
<i>Gwo Giun Lee, He-Yuan Lin, Ming-Jiun Wang, Bo-Han Chen, Yuan-Long Cheng, National Cheng Kung University, Taiwan</i>	
PS-2.3: EFFICIENT REALIZATION OF A CAL VIDEO DECODER ON A MOBILE TERMINAL (POSITION PAPER)	176
<i>Carl Von Platen, Johan Eker, Ericsson Research, Sweden</i>	
PS-2.4: SCHEDULING OF DATAFLOW MODELS WITHIN THE RECONFIGURABLE VIDEO CODING FRAMEWORK	182
<i>Jani Boutellier, University of Oulu, Finland; Veeranjanyulu Sadhanala, Indian Institute of Technology, India; Christophe Lucarz, Philip Brisk, Marco Mattavelli, Ecole Polytechnique Fédérale de Lausanne, Switzerland</i>	

PS-2.5: EFFICIENT DATA FLOW VARIABLE LENGTH DECODING IMPLEMENTATION FOR THE MPEG RECONFIGURABLE VIDEO CODING FRAMEWORK	188
<i>Jianjun Li, Dandan Ding, Christophe Lucarz, Samuel Keller, Marco Mattavelli, EPFL, Switzerland</i>	
PS-2.6: DEFECT-TOLERANT DIGITAL FILTERING WITH UNRELIABLE MOLECULAR ELECTRONICS	194
<i>Shuo Wang, Jianwei Dai, Lei Wang, University of Connecticut, United States</i>	
PS-2.7: TRAFFIC-BALANCED IP MAPPING ALGORITHM FOR 2D-MESH ON-CHIP-NETWORKS	200
<i>Ting-Jung Lin, Shu-Yen Lin, An-Yeu (Andy) Wu, National Taiwan University, Taipei, Taiwan, ROC, Taiwan</i>	
PS-2.8: DSP IMPLEMENTATION OF PROBABILISTIC SOUND SOURCE LOCALIZATION	204
<i>Seung Seob Yeom, Jong Suk Choi, Yoon Seob Lim, Korea Institute of Science and Technology, Republic of Korea; Mignon Park, Yonsei University, Republic of Korea</i>	
PS-2.9: SOFT DECODER ARCHITECTURE OF LT CODES	210
<i>Kai Zhang, Xinming Huang, Chen Shen, Worcester Polytechnic Institute, United States</i>	
PS-2.10: LOW-COMPLEXITY HIGH-SPEED 4-D TCM DECODER	216
<i>Jinjin He, Zhongfeng Wang, Huaping Liu, Oregon State University, United States</i>	
PS-2.11: ERROR-RESILIENT LOW-POWER VITERBI DECODERS VIA STATE CLUSTERING	221
<i>Rami Abdallah, Naresh Shanbhag, University of Illinois at Urbana Champaign, United States</i>	
PS-2.12: FURTHER COST REDUCTION OF ADAPTIVE ECHO AND NEXT CANCELLERS FOR HIGH-SPEED ETHERNET TRANSCEIVERS	227
<i>Jie Chen, Keshab K. Parhi, University of Minnesota, Twin Cities, United States</i>	
 L-DM: DESIGN METHODS	
L-DM.1: POWER EFFICIENT DYNAMIC-RANGE UTILISATION FOR DSP ON FPGA	233
<i>Stephen McKeown, Roger Woods, John McAllister, Queens University Belfast, United Kingdom</i>	
L-DM.2: HIERARCHICAL RUN TIME DEADLOCK DETECTION IN PROCESS NETWORKS	239
<i>Bin Jiang, Ed Depretere, Bart Kienhuis, LIACS, Netherlands</i>	
L-DM.3: APPLICATION-DRIVEN ADAPTIVE FIXED-POINT REFINEMENT FOR SDRS	245
<i>David Novo, Min Li, Bruno Bougard, imec, Belgium; Frederik Naessens, IMEC, Belgium; Liesbet van der Perre, Francky Catthoor, imec, Belgium</i>	
L-DM.4: LOW-COMPLEXITY POLYNOMIALS MODULO INTEGER WITH LINEARLY INCREMENTED VARIABLE	251
<i>Perttu Salmela, Harri Sorokin, Jarmo Takala, Tampere University of Technology, Finland</i>	

L-DM.5: SMARTCELL: A POWER-EFFICIENT RECONFIGURABLE ARCHITECTURE FOR DATA STREAMING APPLICATIONS257

Cao Liang, Xinming Huang, Worcester Polytechnic Institute, United States

L-SS-MLC: SPECIAL SESSION ON SOCS AND DSPS WITH MULTIPLE CORES

L-SS-MLC.1: THE SUPPORT OF SOFTWARE DESIGN PATTERNS FOR STREAMING RPC ON EMBEDDED MULTICORE PROCESSORS263

Kun-Yuan Hsieh, Yen-Chih Liu, Chi-Hua Lai, Jenq-Kuen Lee, National Tsing-Hua University, Taiwan

L-SS-MLC.2: EFFICIENT MAPPING OF ADVANCED SIGNAL PROCESSING ALGORITHMS ON MULTI-PROCESSOR ARCHITECTURES269

Bhavana B. Manjunath, Aaron Williams, Chaitali Chakrabarti, Antonia Papandreou-Suppappola, Arizona State University, United States

L-SS-MLC.3: PARALLELIZATION OF ADABOOST ALGORITHM ON MULTI-CORE PROCESSORS275

Yen-Kuang Chen, Wenlong Li, Xiaofeng Tong, Intel, United States

L-SS-RVC: SPECIAL SESSION ON RECONFIGURABLE VIDEO CODING

L-SS-RVC.1: AUTOMATIC SOFTWARE SYNTHESIS OF DATAFLOW PROGRAM: AN MPEG-4 SIMPLE PROFILE DECODER CASE STUDY281

Ghislain Roquier, Matthieu Wipliez, Mickaël Raulet, INSA de Rennes, France; Jörn W. Janneck, Ian D. Miller, David B. Parlour, Xilinx inc., United States

L-SS-RVC.2: SYNTHESIZING HARDWARE FROM DATAFLOW PROGRAMS: AN MPEG-4 SIMPLE PROFILE DECODER CASE STUDY287

Jörn W. Janneck, Ian D. Miller, David B. Parlour, Xilinx Inc., United States; Ghislain Roquier, Matthieu Wipliez, Mickaël Raulet, IETR/INSA, France

L-SS-RVC.3: VALIDATION OF BITSTREAM SYNTAX AND SYNTHESIS OF PARSERS IN THE MPEG RECONFIGURABLE VIDEO CODING FRAMEWORK293

Mickaël Raulet, Jonathan Piat, INSA de Rennes, France; Christophe Lucarz, Marco Mattavelli, Ecole Polytechnique Fédérale de Lausanne, France

Author Index