2008 IEEE/ACM International Conference on Computer-Aided Design Digest of Technical Papers

San Jose, CA
10-13 November 2008

Pages 1-411

IEEE Catalog Number: CFP 08CAD-PRT
ISBN: 978-1-4244-2819-9

TABLE OF CONTENTS

VOLUME 1

Session 1A **Floorplanning**
Moderators: ***Bill Halpin – Synopsys, Inc.***
Louis Scheffer – Janelia Farm, Howard Hughes Medical Institute

1A.1 **Network Flow-based Power Optimization under Timing Constraints in MSV-driven Floorplanning** 1
Qiang Ma, Evangeline F.Y. Young

1A.2 **Linear Constraint Graph for Floorplan Optimization with Soft Blocks** 9
Jia Wang, Hai Zhou

1A.3 **A Novel Fixed-outline Floorplanner with Zero Deadspace for Hierarchical Design** 16
Ou He, Sheqin Dong, Jinian Bian, Satoshi Goto, Chung-Kuan Cheng

Session 1B **Logic and High-level Synthesis**
Moderators: ***Sunil P. Khatri – Texas A&M Univ.***
Victor Kravets – IBM Corp., T.J. Watson Research Center

1B.1 **Synthesis from Multi-cycle Atomic Actions as a Solution to the Timing Closure Problem** 24
Michal Karczmarek, Arvind

1B.2 **To SAT or Not to SAT: Ashenhurst Decomposition in a Large Scale** 32
Hsuan-Po Lin, Jie-Hong R. Jiang, Ruei-Rung Lee

1B.3 **Boolean Factoring and Decomposition of Logic Networks** 38
Alan Mishchenko, Robert K. Brayton, Satrajit Chatterjee

1B.4 **On the Numbers of Variables to Represent Sparse Logic Functions** 45
Tsutomu Sasao

Session 1C **Test Power and Temperature Control**
Moderators: ***Kartik Mohanram – Rice Univ.***
Jim Plusquellic – Univ. of New Mexico

1C.1 **Effective IR-drop Reduction in At-speed Scan Testing using Distribution-controlling X-Identification** 52
Kohei Miyase, Kenji Noda, Hideaki Ito, Kazumi Hatayama, Takashi Aikyo, Yuta Yamato, Hiroshi Furukawa, Xiaoqing Wen, Seiji Kajihara

1C.2 **Temperature-aware Test Scheduling for Multiprocessor Systems-on-Chip** 59
David R. Bild, Sanchit Misra, Thidapat Chantem, Prabhat Kumar, Robert P. Dick, X. Sharon Hu, Li Shang, Alok Choudhary

1C.3 **On Capture Power-aware Test Data Compression for Scan-based Testing** 67
Jia Li, Xiao Liu, Yubin Zhang, Yu Hu, Xiaowei Li, Qiang Xu

Session 1D **Simulation and Optimization of Analog Systems**
Moderators: ***Eric Grimme – Intel Corp.***
Saurabh Tiwary – Cadence Research Labs

1D.1 **MAPS: Multi-algorithm Parallel Circuit Simulation** 73
Xiaoji Ye, Wei Dong, Peng Li, Sani Nassif

1D.2 **Yield-aware Hierarchical Optimization of Large Analog Integrated Circuits** 79
Guo Yu, Peng Li

1D.3 **Model Reduction via Projection onto Non-linear Manifolds with Applications to Analog Circuits and Bio-chemical Systems** 85
Chenjie Gu, Jaijeet Roychowdhury

Session 2A **Physical Synthesis and Optimization**
Moderators: ***Masanori Hashimoto – Osaka Univ.***
Patrick Groeneveld – Magma Design Automation, Inc.

2A.1 **Algorithms for Simultaneous Consideration of Multiple Physical Synthesis Transforms for Timing Closure** 93
Huan Ren, Shantanu Dutt

2A.2 **Delay-optimal Simultaneous Technology Mapping and Placement with Applications to Timing Optimization** 101
Yifang Liu, Rupesh Shelar, Jiang Hu

2A.3 **PaRS: Fast and Near-optimal Grid-Based Cell Sizing for Library-Based Design** 107
Tai-Hsuan Wu, Azadeh Davoodi

2A.4 **A Polynomial Time Approximation Scheme for Timing Constrained Minimum Cost Layer Assignment** 112
Shiyan Hu, Zhuo Li, Charles J. Alpert

2A.5 **On the Decreasing Significance of Large Standard Cells in Technology Mapping** 116
Jae-sun Seo, Igor L. Markov, Dennis Sylvester, David Blaauw

Session 2B **Decision Procedures in Verification**
Moderators: ***Sanjit Seshia – Univ. of California, Berkeley***
Chung-Yang (Ric) Huang – National Taiwan Univ.

2B.1 **Verification of Arithmetic Datapaths using Polynomial Function Models and Congruence Solving** 122
Neal Tew, Priyank Kalla, Namrata Shekhar, Sivaram Gopalakrishnan

2B.2 **Automated Abstraction by Incremental Refinement in Interpolant-based Model Checking** 129
Marco Murciano, Gianpiero Cabodi, Paolo Camurati

2B.3 **A Succinct Memory Model for Automated Design Debugging** 137
Brian Keng, Hratch Mangassarian, Andreas Veneris

2B.4 **The Analysis of Cyclic Circuits with Boolean Satisfiability** 143
John D. Backes, Brian D. Fett, Marc D. Riedel

Session 2C **Power Estimation and Optimization**
Moderators: ***Youngsoo Shin – KAIST***
Jörg Henkel – Univ. of Karlsruhe

2C.1 **System-level Power Estimation using an On-chip Bus Performance Monitoring Unit** 149
Youngjin Cho, Younghyun Kim, Sangyoung Park, Naehyuck Chang

2C.2 **Minimizing the Energy Cost of Throughput in a Linear Pipeline by Opportunistic Time Borrowing** 155
Mohammad Ghasemazar, Massoud Pedram

2C.3 **Accurate Energy Breakeven Time Estimation for Run-time Power Gating** 161
Hao Xu, Wen-Ben Jone, Ranga Vemuri

2C.4 **Simultaneous Control of Power/Ground Current, Wakeup Time and Transistor Overhead in Power Gated Circuits** 169
Yongho Lee, Deog-Kyoon Jeong, Taewhan Kim

Session 2D **Recent Progress in SSTA**
Moderators: ***Xin Li – Carnegie Mellon Univ.***
Dusan Petranovic – Mentor Graphics Corp.

2D.1 **Efficient Block-based Parameterized Timing Analysis Covering All Potentially Critical Paths** .. 173
Khaled R. Heloue, Sari Onaissi, Farid N. Najm

2D.2 **Adjustment-based Modeling for Statistical Static Timing Analysis with High Dimension of Variability** 181
Lin Xie, Azadeh Davoodi, Jun Zhang, Tai-Hsuan Wu

2D.3 **Post-silicon Timing Characterization by Compressed Sensing** 185
Davood Shamsi, Petros Boufounos, Farinaz Koushanfar

2D.4 **Practical, Fast Monte Carlo Statistical Static Timing Analysis: Why and How** 190
Amith Singhee, Sonia Singhal, Rob A. Rutenbar

2D.5 **On Efficient Monte Carlo-based Statistical Static Timing Analysis of Digital Circuits** 196
Javid Jaffari, Mohab Anis

Session 3A **Placement**
Moderators: ***Bill Halpin – Synopsys, Inc.***
Patrick Madden – Binghamton Univ.

3A.1 **Pyramids: An Efficient Computational Geometry-based Approach for Timing-driven Placement** . 204
Tao Luo, David A. Papa, Zhuo Li, C. N. Sze, Charles J. Alpert, David Z. Pan

3A.2 **Guiding Global Placement with Wire Density** 212
Kalliopi Tsota, Cheng-Kok Koh, Venkataramanan Balakrishnan

3A.3 **Constraint Graph-based Macro Placement for Modern Mixed-size Circuit Designs** 218
Hsin-Chen Chen, Yi-Lin Chuang, Yao-Wen Chang, Yung-Chung Chang

Session 3B **Sequential Synthesis**
Moderators: ***Timothy Kam – Intel Corp.***
Satrajit Chatterjee – Intel Corp.

3B.1 **Pulse Width Allocation with Clock Skew Scheduling for Optimizing Pulsed Latch-based Sequential Circuits** 224
Hyein Lee, Seungwhun Paik, Youngsoo Shin

3B.2 **A Novel Sequential Circuit Optimization with Clock Gating Logic** 230
Yu-Min Kuo, Shih-Hung Weng, Shih-Chieh Chang

3B.3 **Scalable and Scalably-verifiable Sequential Synthesis** 234
Alan Mishchenko, Michael L. Case, Robert K. Brayton, Stephen Jang

Session 3C **System-level Thermal and Power Management**
Moderators: ***Jinfeng Liu – Synopsys, Inc.***
Naehyuck Chang – Seoul National Univ.

3C.1 **System-level Thermal Aware Design of Applications with Uncertain Execution Time** 242
Sushu Zhang, Karam S. Chatha

3C.2 **Proactive Temperature Balancing for Low Cost Thermal Management in MPSoCs** 250
Ayse K. Coskun, Tajana Simunic Rosing, Kenny C. Gross

3C.3 **A Framework for Predictive Dynamic Temperature Management of Microprocessor Systems** .. 258
Omer Khan, Sandip Kundu

3C.4 **A Voltage-frequency Island Aware Energy Optimization Framework for Networks-on-Chip** 264
Wooyoung Jang, Duo Ding, David Z. Pan

Session 3D **Modeling and Simulation of Process Variability**
Moderators: ***Eric Keiter – Sandia National Labs***
Subarna Sinha – Synopsys, Inc.

3D.1 **Statistical Modeling of Metal-gate Work-function Variability in Emerging Device Technologies and Implications for Circuit Design** 270
Hamed Dadgour, Vivek De, Kaustav Banerjee

3D.2 **Large-scale Atomistic Approach to Random-Dopant-Induced Characteristic Variability in Nanoscale CMOS Digital and High-frequency Integrated Circuits** 278
Yiming Li, Chih-Hong Hwang, Ta-Ching Yeh, Tien-Yeh Li

3D.3 **A New Method to Improve Accuracy of Leakage Current Estimation for Transistors with Non-rectangular Gates due to Sub-wavelength Lithography Effects** 286
Kuen-Yu Tsai, Meng-Fu You, Yi-Chang Lu, Philip C.W. Ng

3D.4 **Linear Analysis of Random Process Variability** 292
Victoria Wang, Dejan Marković

Session 4A **Placement and Beyond**
Moderators: ***Louis Scheffer – Janelia Farm, Howard Hughes Medical Institute***
Evangeline F.Y. Young – The Chinese Univ. of Hong Kong

4A.1 **Design and Optimization of a Digital Microfluidic Biochip for Protein Crystallization** 297
Tao Xu, Krishnendu Chakrabarty, Vamsee K. Pamula

4A.2 **Thermal-aware Floorplanning for Task Migration Enabled Active Sub-threshold Leakage Reduction** 302
Hushrav Mogal, Kia Bazargan

4A.3 **Deterministic Analog Circuit Placement using Hierarchically Bounded Enumeration and Enhanced Shape Functions** 306
Martin Strasser, Michael Eick, Helmut Graeb, Ulf Schlichtmann, Frank M. Johannes

Session 4B **Circuit and System Optimization and Modeling**
Moderators: ***Elad Alon – Univ. of California, Berkeley***
Dejan Marković – Univ. of California, Los Angeles

4B.1 **Optimization-based Framework for Simultaneous Circuit-and-System Design-space Exploration: A High-speed Link Example** 314
Ranko Sredojević, Vladimir Stojanović

4B.2 **Breaking the Simulation Barrier: SRAM Evaluation through Norm Minimization** 322
Lara Dolecek, Masood Qazi, Devavrat Shah, Anantha Chandrakasan

4B.3 **Power Supply Noise Aware Workload Assignment for Multi-core Systems** 330
Aida Todri, Malgorzata Marek-Sadowska, Joseph Kozhaya

Session 5A **Global Routing**
Moderators: ***Mustafa Ozdal – Intel Corp.***
Prashant Saxena – Synopsys, Inc.

5A.1 **NTHU-Route 2.0: A Fast and Stable Global Router** 338
Yen-Jung Chang, Yu-Ting Lee, Ting-Chi Wang

5A.2 **FastRoute 3.0: A Fast and High Quality Global Router Based on Virtual Capacity** 344
Yanheng Zhang, Yue Xu, Chris Chu,

5A.3 **Multi-layer Global Routing Considering Via and Wire Capacities** 350
Chin-Hsiung Hsu, Huang-Yu Chen, Yao-Wen Chang

Session 5B **System-level Simulation**
Moderator: ***Andreas Kuehlmann – Cadence Research Labs***

5B.1 **Race Analysis for SystemC using Model Checking** 356
Nicolas Blanc, Daniel Kroening

5B.2 **MC-Sim: An Efficient Simulation Tool for MPSoC Designs** 364
Jason Cong, Karthik Gururaj, Guoling Han, Adam Kaplan, Mishali Naik, Glenn Reinman

5B.3 **Verifying External Interrupts of Embedded Microprocessor in SoC with On-chip Bus** 372
Fu-Ching Yang, Jing-Kun Zhong, Ing-Jer Huang

Session 5C **Analog and Memory Design Enablers**
Moderators: ***Peter Feldmann – IBM Corp., T.J. Watson Research Center***
Xin Li – Carnegie Mellon Univ.

5C.1 **SRAM Dynamic Stability: Theory, Variability and Analysis** 378
Wei Dong, Peng Li, Garng M. Huang

5C.2 **Impulse Sensitivity Function Analysis of Periodic Circuits** 386
Jaeha Kim, Brian S. Leibowitz, Metha Jeeradit

5C.3 **Automated Extraction of Expert Knowledge in Analog Topology Selection and Sizing** 392
Trent McConaghy, Pieter Palmers, Michiel Steyaert, Georges G. Gielen

5C.4 **Importance Sampled Circuit Learning Ensembles for Robust Analog IC Design** 396
Peng Gao, Trent McConaghy, Georges G. Gielen

Session 5D **EMBEDDED TUTORIAL: Graphene Electronics: Design and CAD Challenges and Opportunities**
Moderators: ***Subhasish Mitra – Stanford Univ.***
Iris Bahar – Brown Univ.
Organizer: ***Kartik Mohanram – Rice Univ.***

5D.1 **Physical Models for Electron Transport in Graphene Nanoribbons and their Junctions** 400
Azad Naeemi, James D. Meindl

5D.2 **Characterization and Modeling of Graphene Field-effect Devices** 406
Ken Shepard, Inanc Meric, Philip Kim

VOLUME 2

5D.3 **Graphene Nanoribbon FETs: Technology Exploration and CAD** 412
Kartik Mohanram, Jing Guo

Session 6A **Physical Design for Performance Improvement & Noise Immunity**
Moderators: ***C. W. Jim Chang – Synopsys, Inc.***
Shantanu Dutt – Univ. of Illinois

6A.1 **Clock Buffer Polarity Assignment Combined with Clock Tree Generation for Power/Ground Noise Minimization** 416
Yesin Ryu, Taewhan Kim

6A.2 **Decoupling Capacitance Allocation for Timing with Statistical Noise Model and Timing Analysis** 420
Takashi Enami, Masanori Hashimoto, Takashi Sato

6A.3 **Transition-aware Decoupling-capacitor Allocation in Power Noise Reduction** 426
Po-Yuan Chen, Che-Yu Liu, TingTing Hwang

6A.4 **Placement Based Multiplier Rewiring for Cell-based Designs** 430
Fan Mo, Robert K. Brayton

Session 6B **Novel Design Methodologies for System Architecture**
Moderators: ***Xiaojian Yang – Synopsys, Inc.***
Helia Naeimi – Intel Corp.

6B.1 **Correct-by-Construction Microarchitectural Pipelining** 434
Timothy Kam, Michael Kishinevsky, Jordi Cortadella, Marc Galceran-Oms

6B.2 **Performance Optimization of Elastic Systems using Buffer Resizing and Buffer Insertion** 442
Dmitry E. Bufistov, Jorge Júlvez, Jordi Cortadella

6B.3 **Performance Estimation and Slack Matching for Pipelined Asynchronous Architectures with Choice** 449
Gennette D. Gill, Vishal Gupta, Montek Singh

6B.4 **Diastolic Arrays: Throughput-driven Reconfigurable Computing** 457
Myong Hyon Cho, Chih-Chi Cheng, Michel Kinsy, G. Edward Suh, Srinivas Devadas

Session 6C **DFM Methods for Advanced Lithography**
Moderators: ***Steffen Rochel – Blaze DFM, Inc.***
Azadeh Davoodi – Univ. of Wisconsin

6C.1 **Layout Decomposition for Double Patterning Lithography** 465
Andrew B. Kahng, Chul-Hong Park, Xu Xu, Hailong Yao

6C.2 **Electrically Driven Optical Proximity Correction Based on Linear Programming** 473
Shayak Banerjee, Praveen Elakkumanan, Lars W. Liebmann, Michael Orshansky

6C.3 **A Highly Efficient Optimization Algorithm for Pixel Manipulation in Inverse Lithography Technique** 480
Jinyu Zhang, Min-Chun Tsai, Wei Xiong, Yan Wang, Zhiping Yu

6C.4 **Overlay Aware Interconnect and Timing Variation Modeling for Double Patterning Technology** 488
Jae-Seok Yang, David Z. Pan

6C.5 **Exact Basic Geometric Operations on Arbitrary Angle Polygons using Only Fixed Size Integer Coordinates** 494
Alexey Lvov, Ulrich Finkler

Session 7A **Advances in Routing**
Moderators: ***Chris Chu – Iowa State Univ.***
Ting-Chi Wang – National Tsing-Hua Univ.

7A.1 **BSG-Route: A Length-matching Router for General Topology** 499
Tan Yan, Martin D. F. Wong

7A.2 **Double Patterning Technology Friendly Detailed Routing** 506
Minsik Cho, Yongchan Ban, David Pan

7A.3 **Routing for Chip-Package-Board Co-design Considering Differential Pairs** 512
Jia-Wei Fang, Kuan-Hsien Ho, Yao-Wen Chang

7A.4 **Area-I/O Flip-Chip Routing for Chip-Package Co-design** 518
Jia-Wei Fang, Yao-Wen Chang

7A.5 **Obstacle-avoiding Rectilinear Steiner Tree Construction** 523
Liang Li, Evangeline F. Y. Young

Session 7B **System-level Optimization Issues in Highly Parallel Architectures**
Moderators: ***Robert P. Dick – Northwestern Univ.***
Mike Kishinevsky – Intel Corp.

7B.1 **Evaluation of Voltage Interpolation to Address Process Variations** 529
Kevin Brownell, Gu-Yeon Wei, David Brooks

7B.2 **Efficient Online Computation of Core Speeds to Maximize the Throughput of Thermally Constrained Multi-core Processors** 537
Ravishankar Rao, Sarma Vrudhula

7B.3 **ROAdNoC: Runtime Observability for an Adaptive Network on Chip Architecture** 543
Mohammad A. Al Faruque, Thomas Ebi, Jörg Henkel

7B.4 **FBT: Filled Buffer Technique to Reduce Code Size for VLIW Processors** 549
Talal Bonny, Jörg Henkel

7B.5 **Advancing Supercomputer Performance through Interconnection Topology Synthesis** 555
Yi Zhu, Michael Taylor, Scott B. Baden, Chung-Kuan Cheng

Session 7C **Advances in Embedded Systems**
Moderators: ***James C. Hoe – Carnegie Mellon Univ.***
Luca P. Carloni – Columbia Univ.

7C.1 **Texture Filter Memory - A Power-efficient and Scalable Texture Memory Architecture for Mobile Graphics Processors** 559
B. V. N. Silpa, Anjul Patney, Tushar Krishna, Preeti R. Panda, G. S. Visweswaran

7C.2 **SPM Management using Markov Chain Based Data Access Prediction** 565
Taylan Yemliha, Shekhar Srikantaiah, Mahmut Kandemir, Ozcan Ozturk

7C.3 **Process Variation Aware System-level Task Allocation using Stochastic Ordering of Delay Distributions** 570
Love Singhal, Elaheh Bozorgzadeh

7C.4 **Game-theoretic Timing Analysis** 575
Sanjit A. Seshia, Alexander Rakhlin

7C.5 **Integrated Code and Data Placement in Two-dimensional Mesh Based Chip Multiprocessors** ... 583
Taylan Yemliha, Shekhar Srikantaiah, Mahmut T. Kandemir, Mustafa Karakoy, Mary Jane Irwin

Session 8A **Alternative Circuit Fabrics**
Moderators: ***Eli Bozorgzadeh – Univ. of California, Irvine***
Deming Chen – Univ. of Illinois

8A.1 **Hybrid CMOS-STTRAM Non-volatile FPGA: Design Challenges and Optimization Approaches** .. 589
Somnath Paul, Saibal Mukhopadhyay, Swarup Bhunia

8A.2 **On the Modeling of Resistance in Graphene Nanoribbon (GNR) for Future Interconnect Applications** 593
Tamer Ragheb, Yehia Massoud

8A.3 **A Low-overhead Fault Tolerance Scheme for TSV-based 3D Network on Chip Links** 598
Igor Loi, Shinobu Fujita, Subhasish Mitra, Thomas H. Lee, Luca Benini

Session 8B **Thermal Analysis and Optimization**
Moderators: ***David Atienza – Ecole Polytechnique Fédérale de Lausanne***
Iris Bahar – Brown Univ.

8B.1 **ThermalScope: Multi-scale Thermal Analysis For Nanometer-scale Integrated Circuits** 603
Nicholas Allec, Zyad Hassan, Li Shang, Robert P. Dick, Ronggui Yang

8B.2 **Parameterized Transient Thermal Behavioral Modeling For Chip Multiprocessors** 611
Duo Li, Sheldon X.-D. Tan, Eduardo Hernandez Pacheco, Murli Tirumala

8B.3 **Temperature Aware Task Sequencing and Voltage Scaling** 618
Ramkumar Jayaseelan, Tulika Mitra

Session 8C **Path Delay Anomaly Identification for Quality and Security**
Moderators: ***Alfred L. Crouch – ASSET InterTech, Inc.***
Xinli Gu – Cisco Systems, Inc.

8C.1 **Statistical Path Selection for At-speed Test** 624
Vladimir Zolotov, Jinjun Xiong, Hanif Fatemi, Chandu Visweswariah

8C.2 **Power Supply Signal Calibration Techniques for Improving Detection Resolution to Hardware Trojans** 632
Reza M. Rad, Xiaoxiao Wang, Mohammad Tehranipoor, Jim Plusquellic

8C.3 **Path-RO: A Novel On-chip Critical Path Delay Measurement under Process Variations** 640
Xiaoxiao Wang, Mohammad Tehranipoor, Ramyanshu Datta

Session 8D **Techniques for Next Generation Interconnect Modeling**
Moderators: ***Peter Feldmann – IBM Corp., T.J. Watson Research Center***
Zhenhai Zhu – Cadence Research Labs

8D.1 **Multigrid on GPU: Tackling Power Grid Analysis on Parallel SIMT Platforms** 647
Zhuo Feng, Peng Li

8D.2 **Efficient and Accurate Eye Diagram Prediction for High Speed Signaling** 655
Rui Shi, Wenjian Yu, Yi Zhu, Chung-Kuan Cheng, Ernest S. Kuh

8D.3 **A Capacitance Solver for Incremental Variation-aware Extraction** 662
Tarek A. El-Moselhy, Abe Elfadel, Luca Daniel

Session 9A **Security Issues in ICs**
Moderators: ***Mondira (Mandy) Deb Pant – Intel Corp.***
Seda Memik – Northwestern Univ.

9A.1 **Lightweight Secure PUFs** 670
Mehrdad Majzoobi, Farinaz Koushanfar, Miodrag Potkonjak

9A.2 **Hardware Protection and Authentication through Netlist Level Obfuscation** 674
Rajat Subhra Chakraborty, Swarup Bhunia

9A.3 **MUTE-AES: A Multiprocessor Architecture to Prevent Power Analysis Based Side Channel Attacks of the AES Algorithm** 678
Jude Angelo Ambrose, Sridevan Parameswaran, Aleksandar Ignjatovic

Session 9B **Modeling Approaches for Reliability and Stress Analysis**
Moderators: ***Arijit Raychowdhury – Intel Corp.***
Eli Bozorgzadeh – Univ. of California, Irvine

9B.3 **A Statistical Approach for Full-chip Gate-oxide Reliability Analysis** 685
Kaviraj Chopra, Cheng Zhuo, David Blaauw, Dennis Sylvester

9B.2 **STEEL: A Technique for Stress-enhanced Standard Cell Library Design** 693
Brian T. Cline, Vivek Joshi, Dennis Sylvester, David Blaauw

9B.1 **Process Variability-aware Transient Fault Modeling and Analysis**.....**700**
Natasa Miskov-Zivanov, Kai-Chiang Wu, David Bla

Session 9C **Improving FPGA Reliability**
Moderators: ***Sherief Reda – Brown Univ.***
Rajeev Jayaraman – Xilinx, Inc.

9C.1 **Robust FPGA Resynthesis Based on Fault-tolerant Boolean Matching** 706
Yu Hu, Zhe Feng, Lei He, Rupak Madjumdar

9C.2 **Fault Tolerant Placement and Defect Reconfiguration for Nano-FPGAs** 714
Amit K. Agarwal, Jason Cong, Brian Tagiku

9C.3 **Thermal-aware Reliability Analysis for Platform FPGAs** 722
Prasanth Mangalagiri, Sungmin Bae, Ramakrishnan Krishnan, Yuan Xie, Vijaykrishnan Narayanan

Session 9D **Advances in Model Order Reduction**
Moderators: ***Yaping Zhan – Advanced Micro Devices, Inc.***
Amith Singhee – IBM Corp., T.J. Watson Research Center

9D.1 **Guaranteed Stable Projection-based Model Reduction for Indefinite and Unstable Linear Systems** 728
Bradley N. Bond, Luca Daniel

9D.2 **Sparse Implicit Projection (SIP) for Reduction of General Many-terminal Networks** 736
Zuochang Ye, Zhenhai Zhu, Joel R. Phillips, Dmitry Vasilyev

9D.3 **Modeling and Simulation for On-chip Power Grid Networks by Locally Dominant Krylov Subspace Method** 744
Boyuan Yan, Sheldon X. -D. Tan, Gengsheng Chen, Lifeng Wu

Session 10A **Design Techniques for Emerging Technologies**
Moderators: ***Jaeha Kim – Rambus, Inc.***
Ken Shepard – Columbia Univ.

10A.1 **Integrated Circuit Design with NEM Relays** 750
Fred Chen, Hei Kam, Dejan Marković, Tsu-Jae King Liu, Vladimir Stojanović, Elad Alon

10A.2 **Module Locking in Biochemical Synthesis** 758
Brian D. Fett, Marc D. Riedel

10A.3 **Robust Reconfigurable Filter Design Methodology using Analytic Variability Quantification Techniques** 765
Arthur Nieuwoudt, Jamil Kawa, Yehia Massoud

Session 10B **EMBEDDED TUTORIAL: Learning from Silicon: Correlating Measurements, Models and Design**
Moderator: ***Eli Chiprout – Intel Corp.***
Organizer: ***Eli Chiprout – Intel Corp.***

10B.1 **Using Test Data to Improve IC Quality and Yield** 771
Anne Gattiker

10B.3 **Silicon Feedback to Improve Frequency of High-performance Microprocessors - An Overview** ... 778
Chandramouli Kashyap, Kip Killpack, Chirayu S. Amin, Pouria Bastani

Session 10C **Exploiting Logic Constraints for Noise Analysis**
Moderators: ***Sheldon Tan – Univ. of California, Riverside***
Zhenhai Zhu – Cadence Research Labs

10C.1 **Incorporating Logic Exclusivity (LE) Constraints in Noise Analysis using Gain Guided Backtracking Method** 783
Ruiming Li, An-Jui Shey, Michel Laudes

10C.2 **Constrained Aggressor Set Selection for Maximum Coupling Noise** 790
Debjit Sinha, Gregory Schaeffer, Soroush Abbaspour, Frank Borkam, Alex Rubin

10C.3 **Context-sensitive Static Transistor-level IR Analysis** 797
Weiqing Guo, Yu Zhong, Tom Burd

Session 10D **Advances in Oscillator Macromodeling**
Moderators: ***Saurabh Tiwary – Cadence Research Labs***
Peng Li – Texas A&M Univ.

10D.1 **Frequency-aware PPV: A Robust Phase Macromodel for Accurate Oscillator Noise Analysis** 803
Xiaolue Lai

10D.2 **Smoothed Form of Nonlinear Phase Macromodel for Oscillators** 807
Mark M. Gourary, Sergey G. Rusakov, Sergey L. Ulyanov, Michael M. Zharov, Brian Mulvaney, Kiran K. Gullapalli

10D.3 **Comprehensive Procedure for Fast and Accurate Coupled Oscillator Network Simulation** 815
Prateek Bhansali, Shweta Srivastava, Xiaolue Lai, Jaijeet Roychowdhury