

2008

International Symposium on System-on-Chip

Proceedings

Tampere University of Technology
Tampere, Finland

TABLE OF CONTENTS

PER Performance Enhancement through Antenna And Transceiver Co-Design for Multi-band OFDM UWB Communication	1
<i>Peng Wang, Hannu Tenhunen, Dian Zhou, Li-Rong Zheng</i>	
Trade-offs in Mapping High-level Dataflow Graphs onto ASIPs	6
<i>V.Guzma, S.S. Bhattacharyya, P. Kellomaki, J. Takala</i>	
An ASIC-Design-Based Configurable SOC Architecture for Networked Media.....	10
<i>Ning Ma, Zhibo Pang, Hannu Tenhunen, Li-Rong Zheng</i>	
Congestion-aware Task Mapping in Heterogeneous MPSoCs.....	14
<i>Ewerson Carvalho, Fernando Moraes</i>	
Optimizing Routing Tables on Systems-on-Chip with Content–Addressable Memories	18
<i>Stergios Stergiou, Jawahar Jain</i>	
Balancing Wrapper Chains of SoC Core Based on Best Interchange Decreasing.....	24
<i>Maoxiang Yi, Huaguo Liang, Zhengfeng Huang</i>	
Area-Efficient Low-Cost Low-Dropout Regulators Using MOS Capacitors.....	28
<i>Hamed Aminzadeh, Reza Lotfi, Khalil Mafinezhad</i>	
A 65nm CMOS Down-Sampling Micromixer with Enhanced DC Current Capability.....	32
<i>Kurt Schweiger, Horst Zimmermann</i>	
A 1V Current-Mode Filter in 65nm CMOS Using Capacitance Multiplication.....	36
<i>Heimo Uhrmann, Horst Zimmermann</i>	
FPGA Implementation of a 2G Fibre Channel Link Encryptor with Authenticated Encryption Mode GCM.....	40
<i>L. Henzen, F. Carbognani, N. Felber, W. Fichtner</i>	
On the Credibility of Load-latency Measurement of Network-on-chips.....	44
<i>Erno Salminen, Ari Kulmala, Timo D. Hamalainen</i>	
Realizing a flexible constraint length Viterbi decoder for software radio on a de Bruijn interconnection network	51
<i>Ganesh Garga, Mythri Alle, Keshavan Varadarajan, S.K Nandy, H.S Jamadagni</i>	
Tlmco-simulation for an Open Source Mpsoc Platformunder Starsoc Environment.....	55
<i>Sami Boukhechem, El-Bay Bourennane</i>	
A Flexible Modeling and Simulation Framework for Design Space Exploration	61
<i>Camille Jalier, Didier Lattard, Gilles Sassatelli</i>	
Energy Analysis of Re-Injection Based Deadlock Recovery Routing Algorithms.....	65
<i>H. Kooti, M. Mirza-Aghatabar, S. Hessabi, A. Tavakkol</i>	
UML profile for Estimating Application Worst Case Execution Time on System-On-Chip.....	69
<i>Fateh Boutekkouk, Sébastien Bilavarn, Michel Auguin, Mohammed Benmohammed</i>	
Specification of GNSS Application for Multiprocessor Platform	75
<i>Heikki Hurskainen, Jussi Raasakka, Jari Nurmi</i>	
Inherent Reliability Evaluation of Networks-on-Chip Based on Analytical Models.....	81
<i>Mojtaba Valinataj, Siamak Mohammadi, Saeed Safari</i>	
Implementation of W-CDMA Slot Synchronization on a Reconfigurable System-on-Chip.....	85
<i>Fabio Garzia, Claudio Brunelli, Carmelo Giliberto, Roberto Airoldi, Jari Nurmi</i>	

FlexPath NP - A Network Processor Architecture with Flexible Processing Paths.....	89
<i>Michael Meitinger, Rainer Ohlendorf, Thomas Wild, Andreas Herkersdorf</i>	
Micronmesh for Fault-Tolerant GALS Multiprocessors on FPGA.....	95
<i>Heikki Kariniemi, Jari Nurmi</i>	
Configuring Smart Objects over Cognitive Radio	103
<i>K. Nikunen, H. Heusala, J. Komulainen</i>	
Real-Time Execution Monitoring on Multi-Processor System-on-Chip	107
<i>Kalle Holma, Tero Arpinen, Erno Salminen, Marko Hannikainen, Timo D. Hamalainen</i>	
Using Soft Processors for Component Design in SOC: A Case-Study of Timers	113
<i>M. Ortiz, M. Brox, F. Quiles, A. Gersnoviez, C. Moreno, M. Montijano</i>	
Synthesis for Variable Pipelined Function Units.....	119
<i>Yosi Ben-Asher, Nadav Rotem</i>	
A Two-Phase Return-to-Zero (RZ) Asynchronous Transceiver Circuit for Pipe-Lined SoC Interconnects	121
<i>Muhammad E. S. Elrabaai</i>	
High Resolution Flash Time-to-Digital Converter with Sub-Picosecond Measurement Capabilities	125
<i>Nikolaos Minas, David Kinniment, Gordon Russell, Alex Yakovlev</i>	
RF Transmitter Architecture Investigation for Power Efficient Mobile WiMAX Applications	129
<i>Liang Rong, Fredrik Jonsson, Lirong Zheng, Mats Carlsson, Charlotta Hedenäs</i>	
Evaluation of Heterogeneous Multiprocessor Architectures by Energy and Performance Optimization	133
<i>Heikki Orsila, Erno Salminen, Marko Hannikainen, Timo D. Hamalainen</i>	
Integrating High Speed Multipliers in Coarse Grain Reconfigurable Arrays.....	139
<i>Stavros Georgopoulos, Grigoris Dimitroulakos, Costas E. Goutis</i>	
Analyzing Models of Computation for Software Defined Radio Applications	143
<i>Heikki Berg, Claudio Brunelli, Ulf Lücking</i>	
Multi-Objective Genetic Optimized Multiprocessor SoC Design	147
<i>Mohammad Arjomand, Hamid Sarbazi-Azad, S. Hamid Amiri</i>	
A 110 dB, 3-mW Fourth-order Σ-Δ Modulator for Atmospheric Pressure Sensor	151
<i>Taeyoon Kim, Wonki Park, Heesun Ahn, Kyongwon Min, Sangyong Lee, Jongchan Choi, Chulwoo Kim, Kynnyun Kim, Sungchul Lee</i>	
A State Based Framework for Efficient System-level Power Estimation of Of Custum Reconfigurable Cores.....	155
<i>Ali Ahmadiania, Balal Ahmad, Tughrul Arslan</i>	
Low Noise Amplifier Architecture Analysis for UWB System.....	159
<i>Peng Wang, Fredrik Jonsson, Dian Zhou, Li-Rong Zheng</i>	
Impact of Power-Management Granularity on The Energy-Quality Trade-off for Soft And Hard Real-Time Applications	163
<i>Aleksandar Milutinovic, Kees Goossens, Gerard J.M. Smit</i>	

Author Index