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Session 10: Circuit Simulation (CONVENTION HALL [HAKONE 東(higashi)])

Chairpersons: K. Ishikawa, *Renesas Technol. Corp.*
V. Axelrad, *Sequoia Design System.*

14:30 **10-1** **Synthetic Soft Error Rate Simulation Considering Neutron-induced Single Event Transient from Transistor to LSI-chip level**
M. Hane, H. Nakamura, K. Tanaka, K. Watanabe, Y. Tosaka, K. Ishikawa, and S. Kumashiro
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14:50 **10-2** **Analysis of Temperature and Process Variation Effects on Photo Sensor Circuits Using Device/Circuit Mixed-Mode Simulations**
M. Mochizuki, H. Hayashi, T. Chiba, and K. Fukuda
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15:30 **10-3** **A Surface Potential Based Poly-Si TFT Model for Circuit Simulation**
S. Miyano[1], Y. Shimizu[1], T. Murakami[2], and M. Miura-Mattausch[2]
[1]*Advanced LCD Technologies Development Center Co. Ltd. and* [2]*Hiroshima Univ., Japan*.....373

15:50 **10-4** **A New Unified Compact Model for Quasi-Ballistic Transport: Application to the Analysis of Circuit Performances of a Double-Gate Architecture**
S. Martinie[1,2], D. Munteanu[2], G. Le Carval[1], and J.L. Autran[2,3]
[1]*CEA-LETI MINATEC,* [2]*IM2NP-CNRS, and* [3]*Univ. Inst. of France (IUF), France*..... 377

16:10 **10-5** **Non-Quasi-Static Carrier Dynamics of MOSFETs under Low-Voltage Operation**
M. Miyake[1], D. Hori[1], N. Sadachika[1], U. Feldmann[1], M. Miura-Mattausch[1], H.J. Mattausch[1], T. Iizuka[2], K. Matsuzawa[2], Y. Sahara[2], T. Hoshida[2], and T. Tsukada[2]
[1]*Hiroshima Univ. and* [2]*Semicon. Technol. Academic Res. Center, Japan*.....381