

2008 Formal Methods in Computer-Aided Design

**Portland, Oregon, USA
17-20 November 2008**

ISBN: 978-1-4244-2735-2

Library of Congress: 2008906093

TABLE OF CONTENTS

Invited Tutorial: Considerations in the Design and Verification of Microprocessors for Safety-Critical and Security-Critical Applications	1
<i>David S. Hardin</i>	
Invariant-Strengthened Elimination of Dependent State Elements	9
<i>Michael L. Case, Alan Mishchenko, Robert K. Brayton, Jason Baumgartner, Hari Mony</i>	
Optimal Constraint-Preserving Netlist Simplification	18
<i>Jason Baumgartner, Hari Mony, Adnan Aziz</i>	
Recording Synthesis History for Sequential Verification	27
<i>Alan Mishchenko, Robert Brayton</i>	
BackSpace: Formal Analysis for Post-Silicon Debug	35
<i>Flavio M. De Paula, Marcel Gort, Alan J. Hu, Steven J. E. Wilton, Jin Yang</i>	
Automatic Formal Verification of Block Cipher Implementations	45
<i>Eric Smith, David L. Dill</i>	
Verifying an Arbiter Circuit	52
<i>Chao Yan, Mark R. Greenstreet</i>	
Formal Verification of Hardware Support for Advanced Encryption Standard	61
<i>Anna Slobodová</i>	
BACH : Bounded ReAchability CHecker for Linear Hybrid Automata	65
<i>Lei Bu, You Li, Linzhang Wang, Xuandong Li</i>	
Going with the Flow: Parameterized Verification Using Message Flows	69
<i>Murali Talupur, Mark R. Tuttle</i>	
Automatic Non-Interference Lemmas for Parameterized Model Checking	77
<i>Jesse Bingham</i>	
Model Checking Nash Equilibria in MAD Distributed Systems	85
<i>Federico Mari, Igor Melatti, Ivano Salvo, Enrico Tronci, Lorenzo Alvisi, Allen Clement, Harry Li</i>	
A Theory-Based Decision Heuristic for DPLL(T)	93
<i>Dan Goldwasser, Ofer Strichman, Shai Fine</i>	
A Write-Based Solver for SAT Modulo the Theory of Arrays	101
<i>Miquel Bofill, Robert Nieuwenhuis, Albert Oliveras, Enric Rodríguez-Carbonell, Albert Rubio</i>	
Scaling Up the Formal Verification of Lustre Programs with SMT-Based Techniques	109
<i>George Hagen, Cesare Tinelli</i>	
Word-Level Sequential Memory Abstraction for Model Checking	118
<i>Per Bjesse</i>	
Combining Predicate and Numeric Abstraction for Software Model Checking	127
<i>Arie Gurfinkel, Sagar Chaki</i>	
A Refinement Approach to Design and Verification of On-Chip Communication Protocols	136
<i>Peter Böhm, Tom Melham</i>	
Symbolic Program Analysis Using Term Rewriting and Generalization	144
<i>Nishant Sinha</i>	

Machine-Code Verification for Multiple Architectures - An Application of Decompilation into Logic	153
<i>Magnus O. Myreen, Michael J. C. Gordon, Konrad Slind</i>	
Scheduling Optimisations for SPIN to Minimise Buffer Requirements in Synchronous Data Flow	161
<i>Pieter H. Hartel, Theo C. Ruys, Marc C. W. Geilen</i>	
A Temporal Language for SystemC	171
<i>Deian Tabakov, Gila Kamhi, Moshe Y. Vardi, Eli Singerman</i>	
Augmenting a Regular Expression-Based Temporal Logic with Local Variables	180
<i>Cindy Eisner, Dana Fisman</i>	
Beyond Vacuity: Towards the Strongest Passing Formula	188
<i>Hana Chockler, Arie Gurfinkel, Ofer Strichman</i>	
A Theory of Mutations with Applications to Vacuity, Coverage, and Fault Tolerance	196
<i>Orna Kupferman, Wenchao Li, Sanjit A. Seshia</i>	
Trading-Off SAT Search and Variable Quantifications for Effective Unbounded Model Checking	205
<i>G. Cabodi, P. Camurati, L. Garcia, M. Murciano, S. Nocco, S. Quer</i>	
Automatic Generation of Local Repairs for Boolean Programs	213
<i>Roopsha Samanta, Jyotirmoy V. Deshmukh, E. Allen Emerson</i>	
Consistency Checking of All Different Constraints over Bit-Vectors within a SAT Solver	223
<i>Armin Biere, Robert Brummayer</i>	
Mechanized Information Flow Analysis through Inductive Assertions	227
<i>Warren A. Hunt Jr., Robert Bellarmine Krug, Sandip Ray, William D. Young</i>	
Author Index	