

37th International Symposium on Multiple-Valued Logic

(ISMVL 2007)

**Oslo, Norway
13 – 16 May 2007**



IEEE Catalog Number: CFP07034-PRT
ISBN: 978-1-4244-3017-8

TABLE OF CONTENTS

KEYNOTE ADDRESS

Grand Challenges of Nanoelectronics and Possible Architectural Solutions: What Do Shannon, von Neumann, Kolmogorov, and Feynman Have to Do With Moore	1
<i>Valeriu Beiu</i>	

INVITED PAPER

The Ternary Calculating Machine of Thomas Fowler	8
<i>Mark Glusker</i>	

SESSION 1A: THEORY 1

Automated Reasoning in Some Local Extensions of Ordered Structures	12
<i>Viorica Sofronie-Stokkermans and Carsten Ihlemann</i>	
Reading the Sampling Theorem in Multiple-Valued Logic: A Journey from the (Shannon) Sampling Theorem to the Shannon Decomposition Rule	18
<i>Radomir S. Stanković and Jaakko Astola</i>	
Model-Characterizing Formulas and Normal Forms in Gödel Logics	24
<i>Heng Zhang and Mingyi Zhang</i>	

SESSION 1B: LOGIC FUNCTIONS

Spectral Analysis of Special Properties of Ternary Functions	30
<i>Claudio Moraga, Milena Stanković, and Suzana Stojković</i>	
Representations of Elementary Functions Using Edge-Valued MDDs	36
<i>Shinobu Nagayama and Tsutomu Sasao</i>	
Experimental Studies on SAT-Based ATPG for Gate Delay Faults	43
<i>Stephan Eggersgluß, Daniel Tille, Görschwin Fey, Rolf Drechsler, Andreas Glowatz, Friedrich Hapke, and Jürgen Schöffel</i>	

SESSION 2A: THEORY 2A: THEORY (CLONES)

Polynomials as Generators of Minimal Clones	49
<i>Hajime Machida and Michael Pinsker</i>	
Restriction-Closed Hyperclones	55
<i>B. A. Romov</i>	
Monoidal Intervals of Partial Clones	61
<i>L. Haddad, H. Machida, and I. G. Rosenberg</i>	

SESSION 2B: QUANTUM COMPUTING 1

Variable Reordering and Sifting for QMDD	67
<i>D. Michael Miller, David Y. Feinstein, and Mitchell A. Thornton</i>	
GF(4) Based Synthesis of Quaternary Reversible/Quantum Logic Circuits.....	74
<i>Mozammel H. A. Khan and Marek A. Perkowski</i>	
A Generalization of the Deutsch-Jozsa Algorithm to Multi-valued Quantum Logic	82
<i>Yale Fan</i>	

SESSION 3A: THEORY 3

The Genetic Code as a Multiple-Valued Function and Its Implementation Using Multilayer Neural Network Based on Multi-valued Neurons	87
<i>Igor Aizenberg and Claudio Moraga</i>	
Non-deterministic Multi-valued Matrices for First-Order Logics of Formal Inconsistency	93
<i>Arnon Avron and Anna Zamansky</i>	
New Fastest Linearly Independent Transforms over GF(3).....	99
<i>Bogdan J. Falkowski, Cicilia C. Lozano, and Tadeusz Łuba</i>	
Inversion/Division in Galois Field Using Multiple-Valued Logic.....	105
<i>Nabil Abu-Khader and Pepe Siy</i>	

SESSION 3B: QUANTUM COMPUTING 2

Boolean Functions of Low Polynomial Degree for Quantum Query Complexity Theory	111
<i>Rūsiņš Freivalds and Līva Garkāje</i>	
Quantum Robots for Teenagers.....	114
<i>Arushi Raghuvanshi, Yale Fan, Michal Woyke, and Marek Perkowski</i>	
Quantum Mechanical Model of Emotional Robot Behaviors.....	122
<i>Martin Lukac and Marek Perkowski</i>	
Quantum Realization of Some Ternary Circuits Using Muthukrishnan-Stroud Gates	128
<i>Asif I. Khan, Nadia Nusrat, Samira M. Khan, Masud Hasan, and Mozammel H. A. Khan</i>	

SESSION 4A: THEORY 4

2-SAT Problems in Some Multi-valued Logics Based on Finite Lattices	133
<i>Witold Charatonik and Michał Wrona</i>	
A Complete Resolution Calculus for Signed Max-SAT	139
<i>Carlos Ansótegui, María L. Bonet, Jordi Levy, and Felip Manyà</i>	
Efficient Algorithm for Calculation of Quaternary Fixed Polarity Arithmetic Expansions	145
<i>Bogdan J. Falkowski, Cicilia C. Lozano, and Tadeusz Łuba</i>	

SESSION 4B: CIRCUIT DESIGN 1

Multiple-Valued Logic Circuits Design Using Negative Differential Resistance Devices	151
<i>Krzysztof S. Berezowski and Sarma B. K. Vrudhula</i>	

Low-Power Multiple-Valued Reconfigurable VLSI Using Series-Gating Differential-Pair Circuits	158
<i>Nobuaki Okada and Michitaka Kameyama</i>	

Equalization Techniques for Multiple-Valued Data Transmission and Their Application	164
<i>Yasushi Yuminaka and Kazuyoshi Yamamura</i>	

SESSION 5A: THEORY 5

The Rough Powerset Monad	170
<i>P. Eklund and M. A. Galán</i>	

Exploiting Homogeneous Dual Polarity Routes in Implementation of Algorithms for Optimization of Galois Field Expressions for Ternary Functions	176
<i>Dragan Janković, Radomir S. Stanković, and Claudio Moraga</i>	

Automated Reasoning Algorithm for Linguistic Valued Lukasiewicz Propositional Logic	182
<i>Jun Liu, Luis Martínez López, Yang Xu, and Zhirui Lu</i>	

SESSION 5B: CIRCUIT DESIGN 2

Fast Addition Using Balanced Ternary Counters Designed with CMOS Semi-floating Gate Devices	188
<i>Henning Gundersen and Yngvar Berg</i>	

Algorithm-Level Optimization of Multiple-Valued Arithmetic Circuits Using Counter Tree Diagrams	194
<i>Naofumi Homma, Katsuhiko Degawa, Takafumi Aoki, and Tatsuo Higuchi</i>	

On Designs of Radix Converters Using Arithmetic Decompositions—Binary to Decimal Converters	202
<i>Yukihiro Iguchi, Tsutomu Sasao, and Munehiro Matsuura</i>	

SESSION 6A: THEORY 6

On the Axiomatization of Generalized Entropic Metrics	210
<i>Dan A. Simovici</i>	

Characterization of Partial Sheffer Functions in 3-Valued Logic	216
<i>Lucien Haddad and Dietlinde Lau</i>	

Power Indexes in Voting Systems and Multiple-Valued Logic	222
<i>Yoshinori Yamamoto</i>	

SESSION 6B: CIRCUIT DESIGN 3

A Ternary Analog-to-Digital Converter System	228
<i>Tomoki Tanoue, Munehiko Nagatani, and Takao Waho</i>	

Dual Data-Rate Cyclic D/A Converter Using Semi Floating-Gate Devices	232
<i>René Jensen and Yngvar Berg</i>	

Fault Tolerant CMOS Logic Using Ternary Gates	237
<i>Yngvar Berg, Rene Jensen, Johannes Lomsdalen, Henning Gundersen, and Snorre Aunet</i>	

SESSION 7A: THEORY 7

Universal VLSI Based on a Redundant Multiple-Valued Sequential Logic Operation	243
<i>Tasuku Ito and Michitaka Kameyama</i>	
An Application of 16-Valued Logic to Design of Reconfigurable Logic Arrays	249
<i>Tsutomu Sasao</i>	
Linearization of Ternary Decision Diagrams by Using the Polynomial Chrestenson Spectrum	255
<i>Milena Stankovic, Suzana Stojkovic, and Claudio Moraga</i>	

SESSION 7B: CIRCUIT DESIGN 4

Modeling a Fully Scalable Reed-Solomon Encoder/Decoder over GF(pm) in SystemC	261
<i>André Süflow and Rolf Drechsler</i>	
Design of a Processing Element Based on Quaternary Differential Logic for a Multi-core SIMD Processor	267
<i>Hirokatsu Shirahama, Akira Mochizuki, Takahiro Hanyu, Masami Nakajima, and Kazutami Arimoto</i>	
Asynchronous Peer-to-Peer Simplex/Duplex-Compatible Communication System Using a One-Phase Signaling Scheme	273
<i>Tomohiro Takahashi, Kazuyasu Mizusawa, and Takahiro Hanyu</i>	

SESSION 8A: THEORY 8

Classifications and Enumeration of Bases in P3(2)	279
<i>Dietlinde Lau and Masahiro Miyakawa</i>	
Simulation of Gate Circuits with Feedback in Multi-valued Algebras	285
<i>Janusz Brzozowski and Yuli Ye</i>	
Properties and Fast Algorithms for Ternary Walsh Transform	291
<i>Bogdan J. Falkowski and Shixing Yan</i>	
Weighted and Ordered Direct Cover Algorithms for Minimization of MVL Functions	297
<i>Mostafa Abd-El-Barr and Bambang A. B. Sarif</i>	

SESSION 8B: CIRCUIT DESIGN 5

Four-State Magnetic Random Access Memory and Ternary Content Addressable Memory Using CoFe-Based Magnetic Tunnel Junctions	303
<i>T. Uemura, T. Marukame, K.-I. Matsuda, and M. Yamamoto</i>	
Evaluation of Toggle Coverage for MVL Circuits Specified in the SystemVerilog HDL	309
<i>Mahsan Amoui, Daniel Große, Mitchell A. Thornton, and Rolf Drechsler</i>	
Limits to a Correct Evaluation in RTD-Based Quaternary Inverters	315
<i>Juan Núñez, José M. Quintana, and María J. Avedillo</i>	
Evaluation and Comparison of Threshold Logic Gates	321
<i>Vasilios Lirigis and Elena Dubrova</i>	

SESSION 9A: CIRCUIT DESIGN 6

Towards First-Order Symbolic Trajectory Evaluation	328
<i>Donglin Li, Otmane Ait-Mohamed, and Sa'ed Abed</i>	
Survey of Stochastic Computation on Factor Graphs	335
<i>Saeed Sharifi Tehrani, Shie Mannor, and Warren J. Gross</i>	
A Note on Possible Applications of Fourier Representations in Circuit Design over Reprogrammable Technological Platforms	341
<i>Radomir S. Stanković and Jaakko Astola</i>	

SESSION 9B: CIRCUIT DESIGN 7

Quaternary Look-Up Tables Using Voltage-Mode CMOS Logic Design	347
<i>Ricardo Cunha, Henri Boudinov, and Luigi Carro</i>	
High-Performance Multiple-Valued Comparator Based on Active-Load Dual-Rail Differential Logic for Crosstalk-Noise Reduction	353
<i>Akira Mochizuki, Masatomo Miura, and Takahiro Hanyu</i>	
Experiment Result of Down Literal Circuit and Analog Inverter on CMOS Double- Polysilicon Process	359
<i>Motoi Inaba</i>	
Author Index	