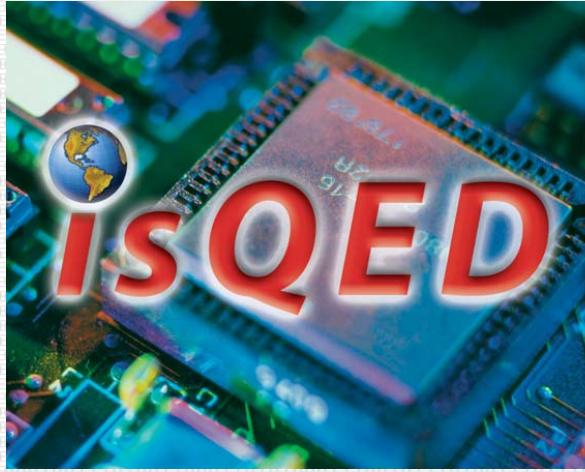


Proceedings of the

ISQED 2009



2009

2009
10th International
Symposium on

QUALITY ELECTRONIC DESIGN

16-18 March 2009
San Jose, California



ISQED

www.isqed.org

www.isqed.org

International Society for Quality Electronic Design

10th International Symposium on Quality Electronic Design (ISQED 2009)

Session 1A: Aging Aware Design

Small Embeddable NBTI Sensors (SENS) for Tracking On-Chip Performance Decay	1
Adam Cabe, Zhenyu Qi, Stuart Wooters, Travis Blalock and Mircea Stan, University of Virginia	
An Unified FinFET Reliability Model Including High K Gate Stack Dynamic Threshold Voltage, Hot Carrier Injection, and Negative Bias Temperature Instability	7
Chenyue Ma ^{1,2} , Bo Li ¹ , Lining Zhang ² , Jin He ^{1,2} , Xing Zhang ² , Xinnan Lin ¹ , and Mansun Chan ³ ¹ Shenzhen Graduate School of Peking Univ, ² Peking Univ, ³ Hong Kong University of Science and Technology	
NBTI-Aware Statistical Circuit Delay Assessment	13
Balaji Vaidyanathan ^{1,2} , Anthony S. Oates ¹ , Yuan Xie ² , Yu Wang ³ , ¹ TSMC, ² Penn. State Univ., ³ Tsinghua Univ.	
On the Efficacy of Input Vector Control to Mitigate NBTI Effects and Leakage Power	19
Yu Wang ¹ , Xiaoming Chen ¹ , Wenping Wang ² , Varsha Balakrishnan ² , Yu Cao ² , Yuan Xie ³ and Huazhong Yang ¹ ¹ Tsinghua Univ., ² Arizona State Univ., ³ Pennsylvania State Univ.	

Session 1B: Robust Circuits

Power & Variability Test Chip Architecture and 45nm-Generation Silicon-Based Analysis for Robust, Power-Aware SoC Design	27
Ramnath Venkatraman, Ruggero Castagnetti, Andres Teene, Benjamin Mbouombouo and Shiva Ramesh, LSI Corp	
On-Chip Dynamic Worst-Case Crosstalk Pattern Detection and Elimination for Bus-based Macro-cell Designs	33
Hariharan Sankaran and Srinivas Katkoori, University of South Florida	
Worst Case Timing Jitter and Amplitude Noise in Differential Signaling	40
Wei Yao, Yiyu Shi, Lei He, Sudhakar Pamarti, Yu Hu, UCLA	
A PVT Aware Accurate Statistical Logic Library for High-κ Metal-Gate Nano-CMOS	47
Dhruva Ghai ¹ , Saraju P. Mohanty ¹ , Elias Kougiianos ¹ , Priyadarsan Patra ² , ¹ University of North Texas, ² Intel Corporation	

Session 1C: Library & Modeling

A General Piece-wise Nonlinear Library Modeling Format and Size Reduction Technique for Gate-level Timing, SI, Power, and Variation Analysis	55
Xin Wang, Alireza Kasnavi and Harold Levy, Synopsys Inc	
Leakage Optimization Using Transistor-Level Dual Threshold Voltage Cell Library	62
Chandra S. Nagarajan ¹ , Lin Yuan ² , Gang Qu ³ , Barbara G. Stamps ⁴ , ¹ Cisco Corp., ² Synopsys Inc., ³ Univ. of Maryland, ⁴ Atmel Corp	
Accurate Closed-form Parameterized Block-based Statistical Timing Analysis Applying Skew-normal Distribution	68
Chun-Yu Chuang ¹ and Wai-Kei Mak ² , ¹ ITRI, ² National Tsing Hua University	
Characterization of Sequential Cells for Constraint Sensitivities	74
Savithri Sundareswaran ¹ , Jacob Abraham ² , Rajendran Panda ¹ , Yun Zhang ¹ and Amit Mittal ¹ ¹ Freescale, ² The Univ. of Texas at Austin	

Session 1D: Design & Modeling in Emerging Technologies

PETE: A Device/Circuit Analysis Framework for Evaluation and Comparison of Charge Based Emerging Devices.....	80
Charles Augustine ¹ , Arijit Raychowdhury ² , Yunfei Gao ¹ , Mark Lundstrom ¹ , Kaushik Roy ¹ ¹ Purdue University, ² Intel	
Architecture Design Exploration of Three-Dimensional (3D) Integrated DRAM	86
Rakesh Anigundi ¹ , Hongbin Sun ² , James Lu ¹ , Ken Rose ¹ , and Tong Zhang ¹ ¹ Rensselaer Polytechnic Institute, ² Xi'an Jiaotong University	
Accurate Buffer Modeling with Slew Propagation in Subthreshold Circuits	91
Jeremy Tolbert and Saibal Mukhopadhyay, Georgia Institute of Technology	
Robust Differential Asynchronous Nanoelectronic Circuits	97
Bao Liu, The University of Texas at San Antonio	

Session 2A: Circuits for Noise & Variation Tolerance

An Enhanced Topology for Reliability of a High Performance 3.3V I/O Buffer in a Single-well Bulk CMOS 1.8v-oxide Low voltage Process	103
Karthik Rajagopal, Aatmesh, and Vinod Menezes, Texas Instruments	
The Design of a Low-Power High-Speed Current Comparator in 0.35-μm CMOS Technology	107
Soheil Ziabakhsh ¹ , Hosein Alavi-Rad ¹ , Mohammad Alavi-Rad ² , Mohammad Mortazavi ² ¹ Guilan University, ² Sharif University of Technology	
Comparison of Supply Noise and Substrate Noise Reduction in SiGe BiCMOS and FDSOI Processes	112
Wai Leng Cheong, Brian Owens, HuiEn Pham, Christopher Hanken, Jim Le, Terri Fiez and Kartikeya Mayaram, Oregon State University	
An Effective Staggered-Phase Damping Technique for Suppressing Power-Gating Resonance Noise during Mode Transition	116
Charbel J. Akl ¹ , Rafic A. Ayoubi ² , Magdy A. Bayoumi ¹ , ¹ Univ of Louisiana at Lafayette, ² Univ of Balamand	

Session 2B: Power vs Performance Trade-offs

Design and Application of Multi-Modal Power-Gating Structures	120
Ehsan Pakbaznia and Massoud Pedram, University of Southern California	
Revisiting the Linear Programming Framework for Leakage Power vs. Performance Optimization	127
Kwangok Jeong, Andrew B. Kahng and Hailong Yao, University of California at San Diego	
Parameter Tuning in SVM-Based Power Macro-Modeling	135
Antonio Gusmão, L. Miguel Silveira and José Monteiro, TU Lisbon	
Performance-Energy Tradeoffs in Reliable NoCs	141
Ying-Cherng Lan ¹ , Michael Chin Chen ¹ , Wei-De Chen ¹ , Sao-Jie Chen ¹ , Yu-Hen Hu ² ¹ National Taiwan University, ² University of Wisconsin, Madison	

Session 2C: Process Variation

3D-GCP: An Analytical Model for the Impact of Process Variations on the Critical Path Delay Distribution of 3D ICs.....	147
Siddharth Garg and Diana Marculescu, Carnegie Mellon University	
Control of Design Specific Variation in Etch-Assisted Via Pattern Transfer by Means of Full-Chip Simulation.....	156
Valeriy Sukharev ¹ , Ara Markosian ¹ , Armen Kteyan ¹ , Levon Manukyan ¹ , Nikolay Khachatryan ¹ , Jun-Ho Choy ¹ , Hasmik Lazaryan ¹ , Henrik Hovsepyan ¹ , Seiji Onoue ² , Takuo Kikuchi ² , Tetsuya Kamigaki ² ¹ Mentor Graphics Corporation, ² Toshiba Corporation	
New Subthreshold Concepts in 65nm CMOS Technology.....	162
Farshad Moradi ¹ , Dag T. Wisland ¹ , Hamid Mahmoodi ² , Ali Peiravi ³ , Snorre Aunet ¹ , Tuan Vu Cao ¹ ¹ University of Oslo, ² San Francisco State University, ³ Ferdowsi University of Mashhad	
On-Chip Transistor Characterization Arrays with Digital Interfaces for Variability Characterization.....	167
Simeon Realov, William McLaughlin, K. L. Shepard, Columbia University	

Session 2D: Embedded Papers

Variability-Aware Optimization of Nano-CMOS Active Pixel Sensors using Design and Analysis of Monte Carlo Experiments	172
Dhruva Ghai, Saraju Mohanty and Elias Kougiannos, University of North Texas	
Yield Evaluation of Analog Placement with Arbitrary Capacitor Ratio.....	179
Jwu-E Chen ¹ , Pei-Wen Luo ² and Chin-Long Wey ¹ , ¹ National Central University, ² Industrial Technology Research Institute	
Analysis of Performance and Reliability Trade-Off in Dummy Pattern Design for 32-nm Technology	185
Aditya Karmarkar, Xiaopeng Xu, Victor Moroz, Greg Rollins and Xiao Lin, Synopsys	
Statistical Yield Analysis of Silicon-On-Insulator Embedded DRAM.....	190
R. Kanj, R. Joshi, JB Kuang, J. Kim, M. Meterelliyo, W. Reohr, S. Nassif and K. Nowka, IBM Corp.	
Effect of Regularity-Enhanced Layout on Printability and Circuit Performance of Standard Cells	195
Hiroki SUNAGAWA, Haruhiko TERADA, Akira TSUCHIYA, Kazutoshi KOBAYASHI and Hidetoshi ONODERA, Kyoto University	
Trading Off Higher Execution Latency for Increased Reliability in Tile-based Massive Multi-core Architectures.....	201
Enric Musoll, ConSentry Networks	
A Simulation-Based Strategy used in Electrical Design for Reliability	208
Yan Liu, Scott Hareland, Donald Hall, Bill Wold, Roger Hubing, Robert Mehregan, Ronen Malka, Manish Sharma and Tom Lane, Medtronic, Inc.	
Estimation and Optimization of Reliability of Noisy Digital Circuits.....	213
Satish Sivaswamy, Kia Bazargan and Marc Riedel, University of Minnesota	
Combinational Logic SER Estimation with the Presence of Re-convergence.....	220
Biwei Liu, Shuming Chen, Yi Xu, National University of Defense Technology	
Effect of NDD Dosage on Hot-Carrier Reliability in DMOS Transistors	226
Jone F. Chen ¹ , Kuen-Shiuan Tian ¹ , Shiang-Yu Chen ¹ , Kuo-Ming Wu ² and C. M. Liu ² ¹ National Cheng Kung University, ² Taiwan Semiconductor Manufacturing Company	

Side Channel Aware Leakage Management in Nano-scale Cryptosystem-on-Chip (CoC)	230
Amirali Khatib Zadeh and Catherine Gebotys, University of Waterloo	
An Effective Approach to Detect Logic Soft Errors in Digital Circuits Based on GRAAL	236
Hai YU, Michael Nicolaidis and Lorena Anghel, TIMA	
An Efficient Approach to SiP Design Integration.....	241
Meng-Syue Chan, Chun-Yao Wang and Yung-Chih Chen, National Tsing Hua University	
A New Low Power Test Pattern Generator Using a Variable-Length Ring Counter	248
Bin Zhou ¹ , Yi-zheng Ye ¹ , Zhao-lin Li ² , Xin-chun Wu ¹ , Rui Ke ¹ , ¹ Harbin Institute of Technology, ² Tsinghua University	
A Case Study on Logic Diagnosis for System-on-Chip	253
Youssef Benabboud ¹ , Alberto Bosio ¹ , Patrick Girard ¹ , Serge Pravossoudovitch ¹ , Arnaud Virazel ¹ , Laroussi Bouzaida ² and Isabelle Izaute ² , ¹ LIRMM - UM2-CNRS, ² STMICROELECTRONICS	
Proactive Management of X's in Scan Chains for Compression.....	260
Anshuman Chandra, Yasunari Kanzawa and Rohit Kapur, Synopsys	
A Built-In Self-Calibration Scheme for Pipelined ADCs	266
Hsiu-Ming (Sherman) Chang ¹ , Kuan-Yu Lin ² , Chin-Hsuan Chen ¹ and Kwang-Ting (Tim) Cheng ¹ , ¹ UC Santa Barbara, ² ITRI	
A Geometric Approach to Register Transfer Level Satisfiability	272
Héctor Navarro ¹ , Saeid Nooshabadi ² , Juan A. Montiel-Nelson ¹ , Víctor Navarro-Botello ¹ , J. Sosa ¹ and José C. García ¹ , ¹ Univ. of Las Palmas de Gran Canaria, ² Gwangju Institute of Science and Technology	
Efficient Diagnosis Algorithms for Drowsy SRAMs	276
Bing-Wei Huang and Jin-Fu Li, National Central University	
Incremental Power Optimization for Multiple Supply Voltage Design.....	280
Yuchun Ma, Xiang Qiu, Xiangqing He and Xianlong Hong, Tsinghua University	
IP Protection Platform Based on Watermarking Technique	287
Yun Du, Yangshuo Ding, Yujie Chen and Zhiqiang Gao, Tsinghua University	
Statistical Static Performance Analysis of Asynchronous Circuits Considering Process Variation.....	291
Mohsen Raji, Behnam Ghvavami and Hossein Pedram, Amirkabir University of Technology	
A Software Pipelining Algorithm in High-Level Synthesis for FPGA Architectures.....	297
Lei Gao ¹ , David Zaretsky ² , Gaurav Mittal ² , Dan Schonfeld ¹ and Prith Banerjee ² , ¹ University of Illinois at Chicago, ² Binachip Inc	
Phenomenological Model for Gate Length Bias Dependent Inverter Delay Change with Emphasis on Library Characterization	303
Qian Ying Tang ¹ , Qiang Chen ² , Niloy Chatterjee ² , Vedank Tripathi ² , Natarajan Nandagopalan ² , and Sridhar Tirumala ² , ¹ UC Berkeley, ² Synopsys	
Statistical Decoupling Capacitance Allocation By Efficient Numerical Quadrature Method.....	309
Thom Jefferson Eguia, Ning Mi and Sheldon Tan, University of California Riverside	
A Novel ACO-based Pattern Generation for Peak Power Estimation in VLSI Circuits.....	317
Yi-Ling Liu, Chun-Yao Wang, Yung-Chih Chen and Ya-Hsin Chang, National Tsing Hua University	
Switch Level Optimization of Digital CMOS Gate Networks	324
Leomar Rosa Jr. ¹ , Felipe Schneider ² , Renato Ribas ³ and Andre Reis ² , ¹ UFPeI, ² Nangate Inc, ³ UFRGS	

Session 3A: System Level Modeling & Design

hArtes Design Flow for Heterogeneous Platforms	330
Muhammad Rashid ¹ , Fabrizio Ferrandi ² and Koen Bertels ³	
¹ Thomson R&D France, ² Politecnico di Milano, ³ Delft University	
An Efficient Reliability Evaluation Approach for System-Level Design of Embedded Systems.....	339
Adeel Israr, Abdulhadi Shoufan and Sorin Huss, TU Darmstadt	
A Case Study on System-Level Modeling by Aspect-Oriented Programming	345
Feng Liu ¹ , Otmane Ait Mohamed ² , Xiaoyu Song ³ and Qingping Tan ¹	
¹ National Lab of Parallel Distributed Processing., ² Concordia University Montreal, ³ Portland State University	
Performance Evaluation of Wireless Networks on Chip Architectures	350
Amlan Ganguly ¹ , Kevin Chang ¹ , Partha Pande ¹ , Benjamin Belzer ¹ and Alireza Nojeh ²	
¹ Washington State University, ² University of British Columbia	

Session 3B: System & Interface Validation

Validating Physical Access Layer of WiMAX Using System Verilog	356
Albert Chiang ¹ , Wei-Hua Han ¹ and Bhanu Kapoor ² , ¹ Synopsys, ² Mimasic	
Accelerating Jitter Tolerance Qualification for High Speed Serial Interfaces.....	360
Yongquan Fan and Zeljko Zilic, McGill University	
Improving the Accuracy of Rule-based Equivalence Checking of System-level Design Descriptions by Identifying Potential Internal Equivalences	366
Hiroaki Yoshida and Masahiro Fujita, University of Tokyo and CREST	
Efficient SAT-Based Techniques for Design of Experiments by Using Static Variable Ordering ...	371
Miroslav Velez and Ping Gao, Aries Design Automation	
An Abstraction Mechanism to Maximize Stimulus Portability Across RTL, FPGA, Software Models and Silicon of SoCs.....	377
Mrinal Bose, Prashant Naphade, Jayanta Bhadra and Hillel Miller, Freescale Semiconductor Inc	

Session 3C: Quality Digital Design

Timing Yield Estimation of Digital Circuits using a Control Variate Technique	382
Javid Jaffari and Mohab Anis, Spry Design Automation & University of Waterloo	
A Unified Gate Sizing Formulation for Optimizing Soft Error Rate, Cross-talk Noise and Power under Process Variations.....	388
Koustav Bhattacharya and Nagarajan Ranganathan, University of South Florida	
TuneLogic: Post-Silicon Tuning of Dual-Vdd Designs.....	394
Stephen Bijansky, Sae Kyu (Scott) Lee and Adnan Aziz, University of Texas at Austin	
A Case for Exploiting Complex Arithmetic Circuits towards Performance Yield Enhancement	401
Shingo Watanabe ¹ , Masanori Hashimoto ² and Toshinori Sato ³	
¹ Kyushu Institute of Technology, ² Osaka University, ³ Fukuoka University	
A Systematic Approach to Modeling and Analysis of Transient Faults in Logic Circuits	408
Natasa Miskov-Zivanov and Diana Marculescu, Carnegie Mellon University	

Session 3D: Embedded Papers

ESD Event Simulation Automation using Automatic Extraction of the Relevant Portion of a Full Chip	414
Thorsten Weyl ¹ , Dave Clarke ¹ , Karl Rinne ² and James A. Power ¹ , ¹ Analog Devices, ² University of Limerick	
Parametric Analysis to Determine Accurate Interconnect Extraction Corners for Design Performance	419
Ayhan Mutlu, Kelvin Le, Ruben Molina and Mustafa Celik, Extreme DA Corporation	
Exploratory Study on Circuit and Architecture Design of Very High Density Diode-Switch Phase Change Memories.....	424
Shu Li and Tong Zhang, Rensselaer Polytechnic Institute	
Adaptive Voltage Controlled Nanoelectronic Addressing for Yield, Accuracy and Resolution.....	430
Bao Liu, University of Texas at San Antonio	
Defect Characterization in Magnetic Field Coupled Arrays	436
Anita Kumari, Javier Pulecio and Sanjukta Bhanja, University of South Florida	
CAD Utilities to Comprehend Layout-Dependent Stress Effects in 45 nm High-Performance SOI Custom Macro Design.....	442
Akif Sultan, John Faricelli, Sushant Suryagandh, Hans VanMeer, Kaveri Mathur, James Pattison, Sean Hannon, Greg Constant, Kalyana Kumar, Kevin Carrejo, Joe Meier, Rasit Topaloglu, Darin Chan, Uwe Hahn, Thorsten Knopp, Victor Andrade, Bill Gardiol, Steve Hejl, David Wu, James Buller, Larry Bair, Ali Icel, Yuri Apanovich, AMD	
A 1.2 Volt, 90nm, 16-Bit Three Way Segmented Digital to Analog Converter (DAC) for Low Power Applications	447
Maruthi Chandrasekhar Bh and Sudeb Dasgupta, Indian Institute of Technology, Roorkee	
Design Methodology of High Performance On-Chip Global Interconnect Using Terminated Transmission-Line	451
Yulei Zhang ¹ , Ling Zhang ¹ , Alina Deutsch ² , George Katopis ² , Daniel Dreps ² , James Buckwalter ¹ , Ernest Kuh ³ and Chung-Kuan Cheng ¹ , ¹ UC San Diego, ² IBM, ³ UC Berkeley	
New Word-line Driving Scheme for Suppressing Oxide-Tunneling Leakage in Sub-65-nm SRAMs.....	459
Ji-Hye Bong ¹ , Yong-Jin Kwon ¹ , Kyeong-Sik Min ^{1,2} and Sung-Mo (Steve) Kang ² , ¹ Kookmin Univ, ² UC Merced	
Adaptive Leakage Control on Body Biasing for Reducing Power Consumption in CMOS VLSI Circuit.....	465
Xin He, Syed Al-Kadry and Afshin Abdollahi, University of California, Riverside	
Standby Power Reduction and SRAM Cell Optimization for 65nm Technology.....	471
S Lakshminarayanan ¹ , Junho Joung ¹ , Geetha Narasimhan ¹ , Ravi Kapre ¹ , Miroslav Slanina ¹ , James Tung ¹ , Morgan Whately ¹ , C.L Hou ² , W.J Liao ² , S.C Lin ² , P-G Ma ² , C-W Fan ² , M-C Hsieh ² , F-C Liu ² , K-L Yeh ² , W-C. Tseng ² and S.W. Lu ² , ¹ Cypress Semiconductor, ² United Microelectronics Corporation	
Optimization Strategies to Improve Statistical Timing.....	476
Parimala Viswanath, Pranav Murthy, Debajit Das, Ramakrishnan Venkatraman, Ajoy Mandal, Arvind Veeravalli and Udayakumar H, Texas Instruments India Ltd.	
Clock Gating Effectiveness Metrics: Applications to Power Optimization	482
Jithendra Srinivas, Madhusudan Rao, Jairam S, Udayakumar H, Jagdish Rao, SDTC TI India	
Buffer/Flip-Flop Block Planning for Power-Integrity-Driven Floorplanning	488
Hsin-Hwa Pan ¹ , Hung-Ming Chen ² and Chia-Yi Chang ³ ² AnaGlobe Technology, Inc., ² National Chiao Tung University, ³ Realtek Semiconductor Corp.	
On Temperature Planarization Effect of Copper Dummy Fills in Deep Nanometer Technology.....	494
Basab Datta and Wayne Burlison, University of Massachusetts-Amherst	

Fast Characterization of Parameterized Cell Library	500
Uday Doddannagari ¹ , Shiyun Hu ² and Weiping Shi ³	
¹ Spanion Inc, ² Michigan Technological University, ³ Texas A&M University	
Cell Shifting Aware of Wirelength and Congestion	506
Liu Dawei, Qiang Zhou, Jinian Bian, Yici Cai and Xianlong Hong, Tsinghua University	
Lagrangian Relaxation Based Register Placement for High-Performance Circuits	511
Mei-Fang Chiang ¹ , Takumi Okamoto ² and Takeshi Yoshimura ¹ , ¹ Waseda University, ² NEC Corp	
Implementation of Power Managed Hyper Transport System for Transmission of HD Video	517
Adithya V. Kodati, Koneswara S. Vemuri, Lili He and Morris Jones, San Jose State University	
Power Aware Placement for FPGAs with Dual Supply Voltages	522
Zohreh Karimi and Majid Sarrafzadeh, UCLA	
VLSI Architectures of Perceptual Based Video Watermarking for Real-Time Copyright Protection	527
Saraju Mohanty, Elias Kougiannos, Wei Cai, Manish Ratnani, University of North Texas	
VeriC: A Semi-Hardware Description Language to Bridge the Gap Between ESL Design and RTL Models	535
Shu-Hsuan Chou, Che-Neng Wen, Yan-Ling Liu and Tien-Fu Chen, National Chung Cheng University	
Power Estimation Methodology for a High-Level Synthesis Framework	541
Sumit Ahuja ¹ , Deepak A Mathaikutty ² , Gaurav Singh ¹ , Joe Stetzer ¹ , Sandeep Shukla ¹ and Ajit Dingankar ²	
¹ Virginia Tech, ² Intel Corp.	
Variability Aware Modeling of SoCs: From Device Variations to Manufactured System Yield	547
Miguel Miranda, Bart Dierickx, Paul Zuber, Petr Dobrovolny, Florian Kutscherauer, Philippe Roussel and P. Poliakov, IMEC	
Kriging Model Combined with Latin Hypercube Sampling for Surrogate Modeling of Analog Integrated Circuit Performance	554
Hailong You, Maofeng Yang, Dan Wang and Xinzhang Jia, Xidian University	
 Session 4A: Co Design Applications for IC Packaging	
Retrospective on Electronics Technology and Prospective Methods for Co-Design of IC Packaging and Manufacturing Improvements	559
Joseph Fjelstad, Verdant Electronics	
50GB/s Signaling on Organic Substrates Using PMTL Technology	565
Farhang Yazdani ¹ , Jamal S. Izadian ² , ¹ BroadPak Corp, ² RFconnext Inc.	
Die/Wafer Stacking with Reciprocal Design Symmetry (RDS) for Mask Reuse in Three-dimensional (3D) Integration Technology	569
Syed M. Alam ¹ , Robert E. Jones ² , Scott Pozder ² and Ankur Jain ²	
¹ EverSpin Technologies, Inc., ² Freescale Semiconductor	
Parallel Flow to Analyze the Impact of the Voltage Regulator Model in Nanoscale Power Distribution Network	576
Amirali Shayan ¹ , Xiang Hu ¹ , He Peng ¹ , Wenjian Yu ² , Wanping Zhang ¹ and Chung-Kuan Cheng ¹	
¹ University of California San Diego, ² Tsinghua University, ³ Qualcomm Inc.	

Session 4B: Novel Design Methodologies

An Analytic Model for Ge/Si Core/Shell Nanowire MOSFETs Considering Drift-Diffusion and Ballistic Transport	582
Lining Zhang ^{1,2} , Jin He ^{1,2} , Jian Zhang ² , Feng Liu ² , Yue Fu ² , Yan Song ² and Xing Zhang ^{1,2} ¹ Shenzhen Graduate School of Peking University, ² Peking University	
Zero Clock Skew Synchronization with Rotary Clocking Technology	588
Vinayak Honkote and Baris Taskin, Drexel University	
Place and Route Considerations for Voltage Interpolated Designs.....	594
Kevin Brownell, Ali Durlav Khan, David Brooks and Gu-Yeon Wei, Harvard University	
Crosstalk Pessimism Reduction with Path Based Analysis.....	601
Genichi Tanaka and Koichi Nakashiro, Renesas Technology Corp.	

Session 4C: Memory Design Solutions

The Impact of BEOL Lithography Effects on the SRAM Cell Performance and Yield	607
Ying Zhou ¹ , Rouwaida Kanj ² , Kanak Agarwal ² , Zhuo Li ² , Rajiv Joshi ² , Sani Nassif ² and Weiping Shi ¹ ¹ Texas A&M University, ² IBM Corp.	
Process Variation Impact on FPGA Configuration Memory	613
Yanzhong Xu, Lin-Shih Liu, Mark Chan and Jeff Watt, Altera Corporation	
Efficient Statistical Analysis of Read Timing Failures in SRAM Circuits	617
Soner Yaldiz, Umut Arslan, Xin Li, Larry Pileggi, Carnegie Mellon University	
Increasing Memory Yield in Future Technologies through Innovative Design.....	622
Costas Argyrides ¹ , Ahmad Al-Yamani ² , Carlos Lisboa ³ , Luigi Carro ³ and Dhiraj Pradhan ¹ ¹ University of Bristol, ² KFUPM, SA, ³ UFRGS	

Session 5A: Clock and Noise

An Efficient Current-Based Logic Cell Model for Crosstalk Delay Analysis	627
Debasish Das ¹ , William Scott ² , Shahin Nazarian ² and Hai Zhou ¹ , ¹ Northwestern Univ, ² Magma Design Automation	
An Application-Specific Adjoint Sensitivity Analysis Framework for Clock Mesh Sensitivity Computation.....	634
Xiaoji Ye and Peng Li, Texas A&M University	
Early Clock Prototyping for Design Analysis and Quality Entitlement.....	641
Vishweshwara Ramamurthy, Ramakrishnan Venkatraman and Vipul Kadodwala, Texas Instruments India	
Automatic Register Banking for Low-Power Clock Trees.....	647
Wenting Hou, Dick Liu and Pei-Hsin Ho, Synopsys Inc.	
A Study of Decoupling Capacitor Effectiveness in Power and Ground Grid Networks.....	653
Aida Todri ¹ , Malgorzata Marek-Sadowska ¹ , Francois Maire ² and Christophe Matheron ² ¹ UC Santa Barbara, ² STMicroelectronics	

Session 5B: Poly Analysis & Delivery Systems

A 0.56-V 128kb 10T SRAM Cell Using Column Line Assist (CLA) Scheme	659
Shunsuke Okumura ¹ , Yusuke Iguchi ¹ , Shusuke Yoshimoto ¹ , Hidehiro Fujiwara ¹ , Hiroki Noguchi ¹ , Koji Nii ² , Hiroshi Kawaguchi ¹ and Masahiko Yoshimoto ¹ , ¹ Kobe University, ² Renesas Technology	
Design and Implementation of a Sub-threshold BFSK Transmitter	664
Suganth Paul ¹ , Rajesh Garg ² , Sunil Khatri ² and Sheila Vaidya ³ ¹ Intel Corporation, ² Texas A&M University, ³ Lawrence Livermore National Laboratory	
A Universal Level Converter Towards the Realization of Energy Efficient Implantable Drug Delivery Nano-Electro-Mechanical-Systems	673
Saraju Mohanty ¹ , Dhruva Ghai ¹ , Elias Kougianos ¹ and Bharat Joshi ² ¹ University of North Texas, ² University of North Carolina at Charlotte	
Temperature Effects on Energy Optimization in Sub-Threshold Circuit Design	680
Basab Datta and Wayne Burlison, University of Massachusetts-Amherst	
Charge Recovery Logic as a Side Channel Attack Countermeasure.....	686
Amir Moradi, Mehrdad Khatir, Mahmoud Salmasizadeh, Mohammad-T. Manzuri Shalmani, Sharif Univ of Technology	

Session 5C: Test Power and Noise

Impact of SoC Power Management Techniques on Verification and Testing	692
Bhanu Kapoor ¹ , Shankar Hemmady ² , Shireesh Verma ³ , Kaushik Roy ⁴ and Manuel D'Abreu ⁵ ¹ Mimasic, ² Synopsys, ³ Conexant, ⁴ Purdue University, ⁵ Sandisk Corp	
A Study on Impact of Loading Effect on Capacitive Crosstalk Noise.....	696
Alodeep Sanyal, Abhisek Pan and Sandip Kundu, University of Massachusetts at Amherst	
Simultaneous Test Pattern Compaction, Ordering and X-Filling for Testing Power Reduction	702
Ju-Yueh Lee, Yu Hu, Rupak Majumdar and Lei He, UCLA	
Markov Source Based Test Length Optimized SCAN-BIST Architecture	708
Aftab Farooqi ¹ , Richard O. Gale ¹ , Sudhakar M. Reddy ² , Brian Nutter ¹ and Chris Monico ¹ ¹ Texas Tech University, ² University of Iowa	
Calculation of Stress Probability for NBTI-Aware Timing Analysis	714
Alexander Stempkovsky, Alexey Glebov and Sergey Gavrilov Research Institute for Design Problems in Microelectronics (IPPM RAS)	

Session 6A: Advances in Timing Analysis & Floor Planning

Derating for Static Timing Analysis: Theory and Practice	719
Ali Dasdan ¹ , Santanu Kolay ¹ and Mustafa Yazgan ² , ¹ Yahoo! Inc., ² Extreme DA Inc.	
An Information Theoretic Framework to Compute the MAX/MIN Operations in Parameterized Statistical Timing Analysis	728
Nikolay Rubanov, Cadence Design Systems	
A Generalized V-shaped Multi-level Method for Large Scale Floorplanning.....	734
Song Chen, Zheng Xu and Takeshi Yoshimura, Waseda University	
Simultaneous Buffer and Interlayer Via Planning for 3D Floorplanning	740
Xu He, Sheqin Dong, Yuchun Ma and Xianlong Hong, Tsinghua University	
IR-Drop Management CAD Techniques in FPGAs for Power Grid Reliability	746
Akhilesh Kumar and Mohab Anis, University of Waterloo	

Session 6B: Low Voltage Design

Functionally Valid Gate-level Peak Power Estimation for Processors	753
Sriram Sambamurthy, Sankar Gurumurthy, Ramtilak Vemu and Jacob A. Abraham, University of Texas at Austin	
On-Chip DC-DC Converters for Three-Dimensional ICs.....	759
Jonathan Rosenfeld and Eby Friedman, University of Rochester	
Active Decap Design Considerations for Optimal Supply Noise Reduction.....	765
Xiongfei Meng and Resve Saleh, University of British Columbia	
Efficient Power Network Analysis with Complete Inductive Modeling	770
Shan Zeng ¹ , Wenjian Yu ¹ , Wanping Zhang ² , Jian Wang ¹ , Xianlong Hong ¹ and Chung-Kuan Cheng ² ¹ Tsinghua University, ² UC San Diego	
Parallel Partitioning Based On-Chip Power Distribution Network Analysis Using Locality Acceleration	776
Zhiyu Zeng, Peng Li and Zhuo Feng, Texas A&M University	

Session 6C: Low Voltage & Variation Tolerant Design

SRAM Supply Voltage Scaling: A Reliability Perspective.....	782
Animesh Kumar, Jan Rabaey and Kannan Ramchandran, University of California, Berkeley	
Low Power Adaptive Pipeline Based on Instruction Isolation.....	788
Seung Eun Lee ¹ , Chris Wilkerson ² , Ming Zhang ² , Rajendra Yavatkar ² , Shih-Lien L. Lu ² and Nader Bagherzadeh ¹ ¹ University of California Irvine, ² Intel Corporation	
Post-Silicon Clock-Invert (PSCI) for Reducing Process-Variation Induced Skew in Buffered Clock Networks	794
Charbel J. Akl ¹ , Rafic A. Ayoubi ² and Magdy A. Bayoumi ¹ , ¹ Univ of Louisiana at Lafayette, ² Univ of Balamand	
Variation-Tolerant Hierarchical Voltage Monitoring Circuit for Soft Error Detection.....	799
Ashay Narsale and Michael Huang, University of Rochester	
SEU Hardened Clock Regeneration Circuits	806
Rajballav Dash, Rajesh Garg, Sunil Khatri and Gwan Choi, Texas A&M University	

Session 6D: System Power & Reliability

PVT Variation Impact on Voltage Island Formation in MPSoC Design	814
Sohaib Majzoub, Resve Saleh and Rabab Ward, University of British Columbia	
Uncriticality-directed Scheduling for Tackling Variation and Power Challenges.....	820
Toshinori Sato ¹ and Shingo Watanabe ² , ¹ Fukuoka University, ² Kyushu Institute of Technology	
Design of Energy-Efficient Channel Buffers with Router Bypassing for Network-on-Chips (NoCs)	826
Avinash Kodi ¹ , Ahmed Louri ¹ and Janet Wang ² , ¹ Ohio University, ² University of Arizona	
NBTI Aware Workload Balancing in Multi-core Systems	833
Jin Sun ¹ , Avinash Kodi ² , Ahmed Louri ¹ and Janet Wang ¹ , ¹ Univ. of Arizona, ² Ohio University	
Joint Write Policy and Fault-Tolerance Mechanism Selection for Caches in DSM Technologies: Energy-Reliability Trade-off.....	839
Mehrtaash Manoochehri, Alireza Ejlali and Seyed Ghassem Miremadi, Sharif University of Technology	