2009 10th Latin American Test Workshop

(LATW)

Rio de Janeiro, Brazil
2 – 5 March 2009

IEEE Catalog Number: CFP09LAT-PRT
ISBN: 978-1-4244-4207-2

TABLE OF CONTENTS

SESSION 1: TEST OF SOCS AND NOCS

Measuring Clock-Signal Modulation Efficiency for Systems-on-Chip in Electromagnetic Interference Environment 1
J. Semiao, J. Freijedo, M. Moraes, M. Mallmann, C. Antunes, J. Benfica, F. Vargas, M. Santos, I.C. Teixeira, J.J.R. Andina, J.P. Teixeira, D. Lupi, E. Gatti, L. Garcia, F. Hernandez

On-line Test and Monitoring of Multi-Processor SoCs: A Software-based Approach 7
M. Benabdenbi, F. Pecheux, E. Faure

NoC Interconnection Functional Testing: Using Boundary-Scan to Reduce the Overall Testing Time 13
M.B. Herve, E. Cota, F.L. Kastensmidt, M. Lubaszewski

A Practical Methodology for Experimental Fault Injection to Test Complex Network-Based Systems 19
C.C. Menegotto, T.S. Weber, R.F. Weber

SESSION 2: FAULT MODELING, ANALYSIS AND SIMULATION

A Modern Look at the CMOS Stuck-Open Fault 25
R. Gomez, V. Champac, C. Hawkins, J. Segura

Study of Radiation Effects on PIN Photodiodes with Deep-Trap Levels using Computer Modeling 31
M.A. Cappelletti, A.P. Cedola, S. Baron, G. Casas, E.L.P. Blanca

SESSION 3: FAULT MODELING, ANALYSIS AND DIAGNOSIS

Exploring Machine Learning Techniques for Fault Localization 37
L.C. Ascari, L.Y. Araki, A.R.T. Pozo, S.R. Vergilio

SESSION 4: DESIGN, VERIFICATION/VALIDATION AND SYNTHESIS FOR TESTABILITY

A Case Study for Formal Verification of a Timing Co-Processor 43
C. Rodrigues

High-Level Decision Diagrams based Coverage Metrics for Verification and Test 49
M. Jenihhin, J. Raik, A. Chepurov, U. Reinsalu, R. Ubar

Minimization of Incompletely Specified Finite State Machines Based on Distinction Graphs 55
A. Alberto, A. Simao

BUGTRACER: A System for Integrated Circuit Development Tracking and Statistics Retrieval 61
T.N.C. Cardoso, J.A. Nacif, A.O. Fernandes, C.N. Coelho Jr.

A Method for HW Functional Verification through HW/SW Co-Simulation in Complex Systems: H.264/AVC Decoder as Case Study 65
D.A. Depra, B. Zatt, S. Bampi

SESSION 5: AUTOMATIC TEST GENERATION

On the Derivation of a Minimum Test Set in High Quality Transition Testing 71
T. Iwagaki, M. Kaneko

Using a Two-Dimensional Fault List for Compact Automatic Test Pattern Generation 77
M. Messing, A. Glowatz, F. Hapke, R. Drechsler

SESSION 6: ANALOG AND MIXED SIGNAL TESTING AND DIAGNOSIS

Using Mixed-Mode Test Bus Architecture to RF-Based Fault Injection Analysis and EMC Fault Debug 83
E.R. Da Silva, F. Costa, F.H. Behrens, R.S. Kickhofel, R. Maltione

Analog Test Bus Architecture for Small Die Size and Limited Pin Count Devices with Internal IPs Testability Emphasis 89
E.R. Da Silva, F. Costa, F.H. Behrens, R.S. Kickhofel, R. Maltione

Estimating the Quality of Oscillation Based Test for Detecting Parametric Faults 95
J. Peralta, M. Costamagna, G. Peretti, E. Romero, C. Marques

Execution Time Reduction of Differential Power Analysis Experiments 101
G. Di Natale, M. Flottes, B. Rouzeyre

SESSION 7: DFT, BIST

Turning JTAG Inside Out for Fast Extended Test Access 106
Sergei Devadze, Artur Jutman, Igor Aleksejev, Raimund Ubar

Investigations of the Diagnosibility of Digital Networks with BIST 112
R. Ubar, S. Kostin, J. Raik

SESSION 08: SINGLE-EVENT UPSET (SEU) MODELLING, SIMULATION AND DETECTION

Study of SEU Effects in a Turbo Decoder Bit Error Rate 118
M. Portela-Garcia, M. Garcia-Valderas, C. Lopez-Ongil, L. Entrena, B. Lestriez, L. Berrojo

Pruning Single Event Upset Faults with Petri Nets 123
P. Maistri

SESSION 09: TEST OF EMBEDDED SOFTWARE, PROTOCOL AND WEBS

Testing Requirements for an Embedded Operating System: the Exception Handling Case Study 129
L.T. Beque, T.D. Pra, E. Cota

Mutation Based Testing of Web Services 135
A.L. Da Silva Solino, S.R. Vergilio

Applying FIRMAMENT to Test the SCTP Communication Protocol Under Network Faults 141
T. Siqueira, B. Fiss, R. Weber, S. Cechin, T. Weber

SESSION 10: DEALING WITH SEUS AND RADIATION EFFECTS

Using Bulk Built-In Current Sensors and Recomputing Techniques to Mitigate Transient Faults in Microprocessors 147
F. Leite, T. Balen, M. Herve, M. Lubaszewski, G. Wirth

Using Software Invariants for Dynamic Detection of Transient Errors 153
C.A. Lisboa, C. Grando, A. De Freitas Moreira, L. Carro

Measuring the Effectiveness of Symmetric and Asymmetric Transistor Sizing for Single Event Transient Mitigation in CMOS 90nm Technologies 159
T. Assis, F.L. Kastensmidt, G. Wirth, R. Reis

Recovery Scheme for Hardening System on Programmable Chips 165
C. Meinhardt, R. Reis, M. Violante, M.S. Reorda

Radiation Damage Characterization of Digital Integrated Circuits 171
S. Sondon, P. Mandolesi, P. Julian, F. Palumbo, M. Alurralde, A. Filevich

SESSION 11: FAULT TOLERANT ARCHITECTURES AND TECHNIQUES

Single Element Correction in Sorting Algorithms with Minimum Delay Overhead 176
C.A. Argyrides, C.A. Lisboa, D.K. Pradhan, L. Carro

Fault Tolerance Assessment of PIC Microcontroller Based on Fault Injection 182
A. Eghbal, H.R. Zarandi, P.M. Yaghini

Generating Non-Uniform Distributions for Fault Injection to Emulate Real Network Behavior in Test Campaigns 188
T.S. Weber, J.C. Vacaro, T. Flores De Siqueira, I. Jansch-Porto

Test and Qualification of a Fault Tolerant FPGA Based Active Antenna System for Space Applications 194
E. Brac, P. Ferreyra, R. Velazco, C. Marques

SESSION 12: PROCESS CONTROL AND MEASUREMENTS

Analyzing Structure-based Techniques for Test Coverage on a J2ME Software Product Line 199
L. Silva, S. Soares

NBTI-aware Technique for Transistor Sizing of High-performance CMOS Gates 205
M.B. Da Silva, V.V.A. Camargo, L. Brusamarello, G.I. Wirth, R. Da Silva

Measurement and Control for Risk-based Test Cases and Activities 210
E. Souza, C. Gusmao, K. Alves, J. Venancio, R. Melo

Adaptive Position Digital Control with Deadbeat Response for a Platform on a Mobile Vehicle 216
H.R. Chamorro, C. Bustos, L.A. Lopez

Author Index