

2009 15th IEEE International Symposium on Asynchronous Circuits and Systems

(ASYNC)

**Chapel Hill, North Carolina, USA
17-20 May 2009**



**IEEE Catalog Number: CFP09012-PRT
ISBN: 978-1-4244-3933-1**

Table of Contents

2009 15th IEEE Symposium on Asynchronous Circuits and Systems **ASYNC 2009**

Message from Chairs
Organizing Committee
Technical Program Committee
Keynote Speakers

GALS

Session Chair: Luciano Lavagno

Programmable/Stoppable Oscillator Based on Self-Timed Rings	1
<i>Eslam Yahya, Oussama Elissati, Hatem Zakaria, Laurent Fesquet, and Marc Renaudin</i>	
Design and Implementation of a GALS Adapter for ANoC Based Architectures.....	11
<i>Yvain Thonnart, Edith Beigné, and Pascal Vivet</i>	
A Programmable Adaptive Router for a GALS Parallel System	21
<i>Jian Wu, Steve Furber, and Jim Garside</i>	

NOC

Session Chair: Marly Roncken

Glitch Sensitivity and Defense of Quasi Delay-Insensitive Network-on-Chip Links.....	30
<i>William John Bainbridge and Sean James Salisbury</i>	
The Lackey Self-Timed Switch-Fabric Design Framework.....	40
<i>Scott Fairbanks</i>	
A Delay-Insensitive Address-Event Link	50
<i>Joseph Lin and Kwabena Boahen</i>	

Delay-Insensitivity

Session Chair: Erik Brunvand

A Necessary and Sufficient Timing Assumption for Speed-Independent Circuits	58
<i>Sean Keller, Michael Katelman, and Alain J. Martin</i>	
Fault Tolerant Delay Insensitive Inter-chip Communication	70
<i>Yebin Shi, Steve B. Furber, Jim Garside, and Luis A. Plana</i>	
GHz Asynchronous SRAM in 65nm	78
<i>Jonathan Dama and Andrew Lines</i>	
Synthesis of Multiple Rail Phase Encoding Circuits	88
<i>Andrey Mokhov, Crescenzo D'Alessandro, and Alex Yakovlev</i>	

Arbitration

Session Chair: Alex Yakovlev

- Modular Approach to Multi-resource Arbiter Design98
Stanislavs Golubcovs, Delong Shang, Fei Xia, Andrey Mokhov, and Alex Yakovlev
- Synchronizer Behavior and Analysis108
Ian W. Jones, Suwen Yang, and Mark Greenstreet
- On the Threat of Metastability in an Asynchronous Fault-Tolerant Clock Generation Scheme118
Gottfried Fuchs, Matthias Függer, and Andreas Steininger

Logic Synthesis

Session Chair: Peter Beere

- Prime Indicators: A Synthesis Method for Indicating Combinational Logic Blocks128
William Toms and Doug Edwards
- Characterization of Asynchronous Templates for Integration into Clocked CAD Flows.....140
Kenneth S. Stevens, Yang Xu, and Vikas Vij
- Heuristic Based throughput Analysis and Optimization of Asynchronous Pipelines151
Alexander Smirnov and Alexander Taubin

High-Level Design

Session Chair: Ken Stevens

- An Automatic Approach to Generate Haste Code from Simulink Specifications162
Maurizio Tranchero, Leonardo M. Reyneri, Arjan Bink, and Mark de Wit
- A Behavioral Synthesis Frontend to the Haste/TiDE Design Flow172
*Sune Fallgaard Nielsen, Jens Sparsø, Jonas Braband Jensen,
and Johan Sebastian Rosenkilde Nielsen*
- Bottleneck Analysis and Alleviation in Pipelined Systems: A Fast Hierarchical Approach.....182
Gennette Gill and Montek Singh

Low-Power Design

Session Chair: Steven M. Nowick

- Fine-Grain Leakage Power Reduction Method for m-out-of-n Encoded Circuits
Using Multi-threshold-Voltage Transistors193
Masashi Imai, Kouei Takada, and Takashi Nanya
- Reducing Power Consumption with Relaxed Quasi Delay-Insensitive Circuits.....201
Christopher LaFrieda and Rajit Manohar

Author Index