Proceedings of the

2009 IEEE INTERNATIONAL INTERCONNECT TECHNOLOGY CONFERENCE (IITC)

Royton Sapporo Hotel
Sapporo, Japan

1-3 June 2009

The IITC is sponsored by the IEEE Electron Devices Society, whose goal is to provide a forum for professionals in semiconductor processing, academia and equipment development to present and discuss exciting new science and technology; and Semiconductor International is the media sponsor.

TABLE OF CONTENTS

SESSION 1: PLENARY SESSION
Co-chairs:
Young-Chang Joo, *Seoul National University*
J.D. Luttmer, *DRS-Infrared Technologies*
and John MacNeil, *Aviza Technology*

1.1 **Keynote Presentation: Integrated Digital AV Platform "UniPhier",** *Satoru Fujikawa, Director, R&D Strategic Semiconductor Development Center, Panasonic Corporation, Osaka, Japan* **1**

SESSION 2: PROCESS INTEGRATION I
Co-chairs: Rudi Cartuyvels, *IMEC*
and Andrew McKerrow, *Novellus Systems*

2.1 **Robust and Low Cost Copper Contact Application for Low Power Device at 32 nm-Node and Beyond**, *A. Isobayashi, J.J. Kelly*, T. Watanabe, M. Fujiwara, C. Koburger, III*, J. Maniscalco*, T. Vo*, S.K. Chiang**, J. Ren***, T. Spooner*, M. Takayanagi, T. Usui, and K. Ishimaru, Toshiba America Electronic Components, Inc., Albany, NY, *IBM Research at Albany Nano-Tech, Albany, NY, **Appplied Materials at Albany Nano-Tech, Albany, NY and ***Applied Materials, Santa Clara, CA* **5**

2.2 **Copper Contact Metallization for 22nm and Beyond**, *S.-C. Seo, C.-C. Yang, C.C. Yeh, B Haran, D. Horak, S. Fan, C. Koburger III, D. Canaperi, S.S. Papa rao*, F. Monsieur**, A. Knorr***, A. Kerber***, C.-K. Hu*, J. Kelly, T. Vo, J. Cummings, M. Smalley, K. Petrillo, S. Mehta, S. Schmitz, T. Levin, D.-G. Park*, J.H. Stathis*, T. Spooner, V. Paruchuri, J. Wynne, D. Edelstein*, D. McHerron, and B. Doris, IBM at Albany Nano-Tech, Albany, NY, *IBM T.J. Watson Research Center, Yorktown Heights, NY, **STMicroelectronics, Albany* **8**

2.3 **Highly-Reliable Molecular-Pore-Stack (MPS)-SiOCH/Cu Interconnects with CoWB Metal- cap Films,** *M. Tagami, N. Furutake, N. Inoue, E. Nakazawa, K. Arita, and Y. Hayashi, NEC Electronics Corp., Sagamihara, Japan* **11**

2.4 **Design Impact Study of Wiring Size and Barrier Metal on Device Performance toward 22nm-node Featuring EUV Lithography**, *N. Nakamura, Y. Takigawa, E. Soda, N. Hosoi, Y. Tarumi, H. Aoyama, Y. Tanaka, D. Kawamura, S.Ogawa, N. Oda, S. Kondo, I. Mori, and S. Saito, Semiconductor Leading Edge Technologies, Inc., Tsukuba, Japan* **14**

2.5 **INVITED – Challenges of Low Effective-K Approaches for Future Cu Interconnect,** *T.I. Bao, H.C. Chen, C.J. Lee, H.H. Lu, H.W. Chen, H.Y. Tsai, C.C. Lin, S.P. Jeng, S.L. Shue, C.H. Yu, Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan* **17**

SESSION 3: INTERCONNECT SYSTEMS

Co-chairs: Chen-Neng Liao, *National Tsing-Hua University*
and Nagaraj NS, *Texas Instruments, Inc.*

3.1 **Performance Comparison between Capacitively Driven Low Swing and Conventional Interconnects for Cu and Carbon Nanotube Wire Technologies,** *K.-H. Koo, P. Kapur, J. Park, H-W. Noh, S.S. Wong, and K.C. Saraswat, Stanford University, Stanford, CA* **23**

3.2 **TSV-aware Interconnect Length and Power Prediction for 3D Stacked ICs,** *D.H. Kim, S. Mukhopadhyay and S.K. Lim, Georgia Institute of Technology, Atlanta, GA* **26**

3.3 **INVITED – Building the Human-Chip Interface***, A.A.A. Aarts, M. Bariatto, A. Fontes, H.P. Neves, S. Kisban*, P. Ruther*, J. Penders**, C. Bartic, K. Verstreken, and C. Van Hoof, IMEC, Leuven, Belgium, *University of Freiburg, Freiburg, Germany and **HOLST Centre, Eindhoven, The Netherlands* **29**

SESSION 4: NOVEL MATERIALS AND CONCEPTS

Co-chairs: Kuniko Kikuta, *NEC Electronics*
and Vincent Arnal, *STMicroelectronics*

4.1 **INVITED – Novel Dielectric Deposition Technology for Advanced Interconnect with Air Gap,** *J. Faguet, E. Lee*, J. Liu*, J. Brcka, and O. Akiyama, Tokyo Electron, US Technology Development Center, Albany, NY and *Tokyo Electron US Technology Development Center, Austin, TX* **35**

4.2 **Optimized Integrated Copper Gap-fill Approaches for 2x Flash Devices**, P. Ma, Q. Luo, *A. Sundarrajan, J. Lu, J. Aubuchon, J. Tseng, N. Kumar, M. Okazaki, Y. Wang, Y. Wang, Y. Chen, M. Naik, I. Emesh*, and M. Narasimhan, Applied Materials, Inc., Santa Clara, CA, *Semitool, Kalispell, MT* **38**

4.3 **Back-End-Of-Line Integration Approaches for Resistive Memories,** *V. Jousseaume, J. Buckley, Y. Bernard, P. Gonon*, C. Vallee*, M. Mougenot*, H. Feldis**, S. Minoret, G. Chamiot-Maitral, A. Persico, A.Zenasni, M. Gely, J.P. Barnes, E. Martinez, H. Grampeix, C. Guedj, J.F. Nodin, and B. DeSalvo, CEA-LETI-Mintec, Grenoble, France, *LTM, Grenoble, France and **STMicroelectronics, Crolles, France* **41**

4.4 **Fabrication of 70-nm-diameter Carbon Nanotube Via Interconnects by Remote Plasma-Enhanced Chemical Vapor Deposition and Their Electrical Properties**, *M. Katagiri, Y. Yamazaki, N. Sakuma, M. Suzuki, T. Sakai, M. Wada*, N. Nakamura*, N. Matsunaga*, S. Sato**, M. Nihei**, and Y. Awano**, MIRAI-Selete, Kawasaki, Japan, *Toshiba Corp., Yokohama, Japan, and **MIRAI-Selete, Kanagawa, Japan* **44**

4.5 **INVITED – Conductance Quantization of Gold Nanowires as a Ballistic Conductor,** *K. Takayanagi, Y. Oshima* and Y. Kurui, Tokyo Institute of Technology, Tokyo, Japan and *Interdisciplinary Graduate School of Science and Engineering, Yokohama, Japan* **47**

SESSION 5: TSV/3D PROCESSES AND INTEGRATION

Co-chairs: Scott List, *SRC*
and Tetsu Tanaka, *Tohoku University*

5.1 **Magnetically-Enhanced Capacitively-Coupled Plasma Etching for 300 mm Wafer-Scale Fabrication of Cu Through-Silicon-Vias for 3D Logic Integration,** *W.H. Teh[*, **] , R. Caramto*, S.Arkalgud*, T. Saito***, K. Maruyama***, and K. Maekawa^, *SEMTATECH, Albany, NY, **Intel Corp., Hillsboro, OR, ***Tokyo Electron AT Ltd., Nirasaki, Japan, and ^TEL Technology Center America, Albany, NY* **53**

5.2 **Co-design of Reliable Signal and Power Interconnects in 3D Stacked ICs**, *Y.-J. Lee, M. Healy and S.K. Lim, Georgia Institute of Technology, Atlanta, GA* **56**

5.3 **INVITED – 3D Technologies: Requiring more than 3 Dimensions from Concept to Product,** *B. Swinnen, IMEC, Leuven, Belgium* **59**

5.4 **INVITED – Reliable Through Silicon Vias for 3D Silicon Applications**, *M. Shapiro, M. Interrante*, P. Andry**, B. Dang**, C. Tsang**, R. Liptak*, J. Griffith*, E. Sprogis***, L. Guerin^, V. Truong^, D. Berger*, and J. Knickerbocker**, IBM Microelectronics, Austin, TX, *IBM Microelectronics, Hopewell Junction, NY, **IBM Research, Yorktown Heights, NY, ***IBM Microelectronics, Essex Junction, VT, ^IBM Canada, Bromont, QC, Canada* **63**

SESSION 6: METROLOGY AND PROCESS CONTROL I

Co-chairs: Dorel Toma, *Tokyo Electron U.S. Holdings*
and Shin-Puu Jeng, *TSMC*

6.1 **A Novel Helium Ion Microscope for Interconnect Material Imaging,** *W. Thompson, S. Ogawa*, L.Stern, L. Scipioni, and J. Notte, Carl Zeiss SMT, Peabody, MA and *Semiconductor Leading Edge Technologies, Inc., Tsukuba, Japan* **69**

6.2 **Synchrotron Measurement of the Effect of Dielectric Porosity and Air Gaps on the Stress in Advanced Cu/Low-k Interconnects**, *C.J. Wilson, C. Zhao, L. Zhao**, Zs. Tokei, K. Croes,M. Pantouvaki, G.P. Beyer, A.B. Horsfall*, and A.G. O'Neill*, IMEC, Leuven, Belgium, *Newcastle University, Newcastle, UK and **Intel Corp/IMEC, Leuven, Belgium* **72**

6.3 **Characterization of Low-k SiOCH Layers in Fine-Pitch Cu-Damascene Interconnects by Monoenergetic Positron Beams**, *A. Uedono, N. Inoue*, Y. Hayashi*, K. Eguchi*, T. Nakamura*, Y. Hirose*, M. Yoshimaru*, N. Oshima**, T. Ohdaira**, and R. Suzuki**, University of Tsukuba, Tsukuba, Japan, *Semiconductor Technology Academic Research Center, Yokohama, Japan and **National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan* **75**

6.4 **Plasma Altered Layer Model and Application for Plasma Damage of Porous OSG Films** *H. Shi, H. Huang, J. Bao, J. Im, P.S. Ho, Y. Zhou*, J.T. Pender*, M. Armacost*, and D. Kyser*, The University of Texas, Austin, TX and *Applied Materials, Sunnyvale, CA* 78

SESSION 7: POSTER SESSION

7.1 **Characterization of Plasma Damaged Porous ULK SiCOH Layers in Aspect of Changes in the Diffusion Behavior of Solvents and Repair-Chemicals,** *T. Oszinda, M. Schaller*, D. Fischer*, and S.E. Schulz**, Fraunhofer Center Nanoelektronische Technologien, Dresden, Germany, *AMD Saxony, Dresden, Germany, and **TU Chemnitz/Fraunhofer ENAS, Chemnitz, Germany* 83

7.2 **Upstream Electromigration Study on Multiple Via Structures in Copper Interconnect,** *M. Lin, N. Jou, J.W. Liang, A. Juan, and K.C. Su, United Microeletronics Corp., Hsinchu, Taiwan* 86

7.3 **A Double Thick-Polymer Technology to Realize Low Signal Pad Capacitance Suitable for High-speed Data Transmission,** *K. Kikuchi, J. Sakai*, K. Soejima**, S. Funato, M. Kawano**, H. Kouta*, and S. Yamamichi, NEC Corporation, Sagamihara, Japan, NEC Corporation, Kawasaki, Japan, and **NEC Electronics Corporation, Sagimihara, Japan* 89

7.4 **The Effects of Dielectric Slots on Copper/Low-k Interconnects Reliability,** *A. Heryanto, Y.K. Lim*, K.L. Pey, W. Liu*, J.B. Tan*, D.K. Sohn*, and L.C. Hsia*, Nanyang Technological University, Singapore, *Chartered Semiconductor Manufacturing, Ltd., Singapore* 92

7.5 **Novel PEALD-Ru Formation Technique using H_2 & H_2/N_2 Plasma as a Seed Layer for Direct CVD-Cu Filling,** *D. Jeong, H. Inoue, Y Ohno, K. Namba, and H. Shinriki, ASM Japan, Tokyo, Japan* 95

7.6 **Resist Planarization for Trench First Dual Damascene,** *H. Chibahara, H. Korogi*, Y. Ono, T. Saito, K. Yoshikawa, K. Yonekura, T.Furuhashi, K.Tomita, H. Sakaue*, A. Ueki**, S. Matsumoto*, M. Akazawa, and H. Miyatake, Renesas Technology Corp., Itami, Japan, *Panasonic Corporation, Kyoto, Japan, and **Panasonic Semiconductor Engineering Co., Ltd., Kyoto, Japan* 98

7.7 **New Multi-Step UV Curing Process for Porogen-based Porous SiOC**, *K. Seo, Y. Oka**, K. Nomura*, M. Tsutsue*, E. Kobori*, K. Goto**, Y. Mizukami, T. Ohtsuka*, K. Tsukamoto*, S. Matsumoto*, and T. Ueda*, Pansonic Semiconductor Engineering Co., Ltd., Koyto, Japan, *Pansonic Co., Ltd., Kyoto, Japan, and **Renesas Technology, Corp., Hyogo, Japan* 101

7.8 **Determination of the Impact of Field Enhancement in Low-K Dielectric Breakdown,** *M Bashir and L. Milor, Georgia Institute of Technology, Atlanta, GA* 104

7.9 **Stress Sensitivity Analysis on TSV Structure of Wafer-on-a-Wafer (WOW) by the Finite Element Method (FEM),** *H. Kitada, N. Maeda, K. Fujimoto*, K. Suzuki*, A. Kawai**, K. Arai**, T. Suzuki***, T. Nakamura***, and T. Ohba, University of Tokyo, Tokyo, Japan, *Dai Nippon Printing, Chiba, Japan, **DISCO Corporation, Tokyo, Japan, and ***Fujitsu Laboratories Ltd., Atsugi, Japan* **107**

7.10 **Packaging Characteristics of 6-layer Ultra Low-k/Cu Dual Damascene Interconnect Featuring Advanced Scalable Porous Silica (k=2.1),** *S. Chikaki, E. Soda, A. Gawase, T.Suzuki*, Y. Kawashima**, N. Oda, and S. Saito, Semiconductor Leading Edge Technologies, Inc., Ibaraki, Japan, *Sumitomo Bakelite Co., Ltd., Tochigi, Japan, and **NEC Electronics Corp., Kanagawa, Japan* **110**

7.11 **Effects of N doping in Ru-Ta Alloy Barrier on Film Property and Reliability for Cu Interconnects,** *N. Torazawa, T. Hinomura, K. Mori*, Y. Koyama**, S. Hirao, E. Kobori, H. Korogi, K. Maekawa*, K. Tomita*, H. Chibahara*, N. Suzumura*, K. Asai*, H. Miyatake*, and S. Matsumoto, Panasonic Corporation, Kyoto, Japan, *Renesas Technology Corporation, Hyogo, Japan and **Renesas Semiconductor Engineering Corp., Hyogo, Japan* **113**

7.12 **Theoretical Analyses of Chemical Reactions for Forming Hydrocarbon-Bridged SiOCH Low-k Films in PECVD Processes,** *N. Tajima, Y. Ohashi*, S. Nagano*, Y. Xu**, S. Matsumoto**, T. Kada**, and T. Ohno, National Institute for Materials Science, Tsukuba, Japan, *Taiyo Nippon Sanso Corp., Tokyo, Japan and **Tri Chemical Laboratories, Inc., Uenohara, Japan* **116**

7.13 **Development of Porous Silica Ultra Low-k Films for 32 nm-node Interconnects and Beyond**, *T. Yamazaki, M. Hirakawa, T. Nakayama, and H. Murakami, ULVAC, Inc., Susono, Japan* **119**

7.14 **Technology Nodes,** *M. Vilmay, D. Roy, C. Besset, D. Galpin, C. Monget, P. Vannier, Y. Le Friec, G. Imbert, M. Melliler, S. Petitdidier, O. Robin, J. Guillan, S. Chhun, L. Arnaud*, F. Volpi**, and J-M. Chaix**, STMicroelectronics, Crolles, France, *CEA-Leti-MINATEC, Grenoble, France and **SIMAP Grenoble INP-CNRS, Saint Martin d'Heres, France* **122**

7.15 **Electrode and Substrate Contacts in Carbon Nanofiber Interconnects,** *T. Saito, H. Yabutani, T. Yamada, P. Wilhite, and C.Y. Yang, Santa Clara University, Santa Clara, CA* **125**

7.16 **Thin-Layer Au-Sn Solder Bonding Process for Wafer-Level Packaging, Electrical Interconnects and MEMS Applications,** *N. Belov, T.-K. Chou*, J. Heck*, K. Kornelsen**, D. Spicer**, S. Akhlaghi**, M. Wang, and T. Zhu, Nanochip, Inc., Fremont, CA, *Intel Corp., Santa Clara, CA and **Micralyne, Edmonton, AB, Canada* **128**

7.17 **Metrology of 3D IC with X-ray Microscopy and Nano-scale X-ray CT,** *S. Wang, J.Gelb, S.H. Lau, and W. Yun, Xradia, Inc., Concord, CA* **131**

7.18 **Evaluation of Plasma Damage in Blanket and Patterned Low-k Structures by Near-Field Scanning Probe Microwave Microscope: Effect of Plasma Ash Chemistry**, *A.M. Urbanowicz, V.V.Talanov*, M. Pantouvaki, H. Struyf, S. De Gendt, and M.R. Baklanov, IMEC, Leuven, Belgium and *Solid State Measurements, Inc., Pittsburgh, PA* **134**

7.19 **On Chip Monitoring of Via Degradation**, *F. Ahmed and L. Milor, Georgia Institute of Technology, Atlanta, GA* **137**

7.20 **Defect Study of Manufacturing Feasible Porous Low k Dielectrics Direct Polish for 45nm Technology and Beyond,** *C.-L. Hsu, J.Y. Fang*, A. Yu*, J. Lin*, C. Huang*, J.Y. Wu*, and D-C. Perng, National Cheng Kung University, Tainan, Taiwan and *United Microeletronics Corp., Tainan, Taiwan* **140**

7.21 **Chip-Packaging Interaction in Cu/Very Low-k Interconnect,** *H-P. Wei, H-Y. Tsai, Y-W. Liu, H-W. Chen, S-P. Jeng, and D. CH Yu, Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan* **143**

7.22 **A Self-aligned Airgap Interconnect Scheme,** *H-W. Chen, S-P. Jeng, H-Y. Tsai, Y-W. Liu, H-P. Wei, C.H. Yu and Y.C. Sun, Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan* **146**

7.23 **Advanced BEOL Integration using Porous Low-k (k=2.25) Material with Charge Damageless Electron Beam Cure Technique,** *T. Owada, N. Ohara, H. Watatani, T. Kouno, H. Kudo, H. Ochimizu, T. Sakoda, N. Asami, Y. Ohkura, S.Fukuyama, A. Tsukune, M. Nakaishi, T. Nakamura, Y. Nara, and M. Kase, Fujitsu Microeletronics Ltd., Kuwana, Japan* **149**

7.24 **Enabling 3D Interconnects with Metal Direct Bonding**, *L. Di Cioccio, P. Gueguen, T. Signamarcheix, M Rivoire*, D. Scevola*, R.Calhours*, P. Leduc, M. Assous, and L. Clavelier, CEA-Leti-MINATEC, Grenoble, France and *STMicroelectronics, Crolles, France* **152**

STUDENT/NEW ENGINEER POSTERS

7.25 **Demonstration of TFHM Scalability to 32 nm Node BEOL Interconnect and Extendibility to ELK k ≤ 2.3 Dielectric Material,** *K. Hamioud, V. Arnal, A. Farcy, V. Jousseaume*, A. Zenasni*, O. Gourhant, B. Icard*, J. Pradelles*, S. Manakli, Ph. Brun*, G. Imbert, C. Jayet*, M. Assous*, S. Maitrejean*, M. Vilmay, D. Galpin, C. Monget, J. Guillan, S. Chhun, E. Richard, D. Barbier**, M. Haond, STMicroelectronics, Crolles, France, *CEA-LETI-MINATEC, Grenoble, France and **INL, Villeurbanne, France* **155**

7.26 **Cobalt and Nickel Atomic Layer Depositions for Contact Applications,** *H-B-R. Lee, W-H. Kim, Y. Park, S. Baik, and H. Kim, POSTECH, Pohang, Korea* **157**

7.27 **Growth Analysis of Self-Formed Ti-Rich Interface Layers in Cu(Ti)/Dielectric-layer Samples using Rutherford Backscattering Spectrometry,** *K. Kohama, K. Ito, K. Mori*, K. Maekawa*, Y. Shirai, and M. Murakami, Kyoto University, Kyoto, Japan and *Renesas Technology Corp., Itami, Japan* **159**

7.28 **Novel Low-k SiOC (k=2.4) with Superior Tolerance to Direct Polish and Ashing for Advanced BEOL Integration,** *N. Asami, T. Owada, S. Akiyama, N. Ohara, Y. Iba, T. Kouno, H. Kudo, S. Takesako, T. Osada, T. Kirimura, H. Watatani, A. Uedono*, Y. Nara, and M. Kase, Fujitsu Microelectronics Ltd., Kuwana, Japan and *University of Tsukuba, Tsukuba, Japan* **161**

7.29 **A Wafer-Level 3D Integration Using Bottom-Up Copper Electroplating and Hybrid Metal-Adhesive Bonding,** *C. Song, Z. Wang, Z. Tan, and L. Liu, Tsinghua University, Beijing, China* **163**

7.30 **Effect of Wet Pre-treatment on Interfacial Adhesion Energy of Direct Cu-Cu Bond,** *E.J. Jang, B. Kim*, T. Matthias*, S. Hyun**, H.J. Lee**, and Y.B. Park**, Andong National University, Andong, Korea, *EV Group, Tempe, AZ and **Korea Institute of Machinery & Materials, Daejeon, Korea* **165**

7.31 **Study of Low Resistance TSV using Electroless Plated Copper and Tungsten-alloy Barrier,** *F. Inoue, T. Yokoyama, S. Tanaka*, K. Yamamoto*, M. Koyanagi, **, T. Fukushima**, Z. Wang***, and S. Shingubara, Kansai University, Suita, Japan, *National Institute of Communication Technology, Tokyo, Japan, **Tohoku University, Sendai, Japan, and ***Shaanxi Normal University, Xi'an, China* **167**

7.32 **Withdrawn**

7.33 **A Novel High Coplanarity Lead Free Copper Pillar Bump Fabrication Process***, H-J. Hsu, J-T. Huang, K-Y. Lee, R-G. Wu and T-C. Tsai, National Taipei University of Technology, Taipei, Taiwan* **169**

7.34 **The Integration of SWNTs with CMOS IC After Covering Nickel/Gold on the Aluminum Electrodes,** *J-T. Huang, K-Y. Jenq, P-C. Lin, H-J. Hsu, T-C. Tsai, and C-K. Chen, National Taipei University of Technology, Taipei, Taiwan* **171**

7.35 **Atomic Layer Deposition of Copper Thin Film using Cu^{II}(diketoiminate)$_2$ and H_2,** *B. Han, K-M. Park, K. Park*, J-W. Park**, and W-J. Lee, Sejong University, Seoul, Korea, *KAIST, Daejeon, Korea, and **UP Chemical Corp., Pyeongtaek, Korea* **173**

7.36 **Ruthenium Films Deposited under H_2 by MOCVD using a Novel Liquid Precursor,** *T. Kadota, C. Hasegawa and H. Nihei, Ube Industries, Ltd., Ube, Japan* **175**

SESSION 8: RELIABILITY

Co-chairs: Toshiaki Hasegawa, *Sony Corp.*
and Mike Armacost, *Applied Materials*

8.1 **INVITED – Reliability Failure Modes in Interconnects for the 45nm Technology Node and Beyond,** *L. Arnaud, D. Galpin*, S. Chhun*, C. Monget*, E. Richard*, D. Roy*, C. Besset*, M. Vilmay*, L. Doyen*, P. Waltz*, E. Petitprez*, F. Terrier* G. Imbert*, Y. Le Friec*, CEA LETI Minatec, Grenoble France and *STMicroelectronics, Crolles France* **179**

8.2 **Correlation between I-V Slope and TDDB Voltage Acceleration for Cu/Low-k Interconnects**, *F. Chen, J. Gambino, M Shinosky, B. Li, O. Bravo*, M. Angyal*, D. Badami, and J. Aitken, IBM Systems & Technology Group, Essex Junction, VT and *IBM Microelectronics, Hopewell Junction, NY* **182**

8.3 **Constant Field Stressing of Via-to-Line Spacing for Accurate Projection of Intrinsic TDDB Lifetime***, T. Kamoshima, K. Makabe, M. Amishiro, T. Furusawa, Y. Takata, and M. Ogasawara, Renesas Technology Corp., Hitachinaka, Japan* **185**

8.4 **Copper Wiring Encapsulation at Semi-Global Level to Enhance Wiring and Dielectric Reliabilities for Next-Generation Technology Nodes,** *H. Kudo, M. Haneda, T. Tabira, M.Sunayama, N. Ohtsuka, N. Shimizu, K. Yanai, H. Ochimizu, A. Tsukune, H. Matsuyama, and T. Futatsugi, Fujitsu Microelectronics Ltd., Kuwana, Japan* **188**

8.5 **Novel Scalable TDDB Model for Large-Area MIM Decoupling Capacitors in High Performance LSIs,** *N. Inoue, I. Kume, T. Iwaki, A. Shida, S. Yokogawa, M Furumiya, and Y. Hayashi, NEC Electronics Corp., Sagamihara, Japan* **191**

SESSION 9: MATERIALS AND UNIT PROCESSES I

Co-chairs: Andreas Klipp, *BASF Electronic Materials*
and Hiroshi Toyoda, *Toshiba Corp.*

9.1 **Deposition Behavior and Diffusion Barrier Property of CVD MnO_x**, *K. Matsumoto, K. Neishi*, H. Itoh, H. Sato, S. Hosaka, and J. Koike*, Tokyo Electron, Ltd., Nirasaki, Japan and *Tohoku University, Sendai, Japan* **197**

9.2 **Metallization of sub-30 nm Interconnects: Comparison of Different Liner/Seed Combinations***,L. Carbonell, H. Volders, N. Heylen, K. Kellens, R. Caluwaerts, K. Devriendt, E. Altamirano Sanchez, J. Wouters, V. Gravey*, K.Shah**, Q. Luo**, A. Sundarrajan**, J. Lu**, J. Aubuchon**, P. Ma**, M. Narasimhan**, A. Cockburn*, Zs. Tokei, and G.P. Beyer, IMEC, Leuven, Belgium, *Applied Materials Belgium, Leuven, Belgium and **Applied Materials, Santa Clara, CA* **200**

9.3 **Thin Low-k SiOC(N) Dielectric / Ruthenium Stacked Barrier Technology,** *N. Tarumi, N. Oda, S. Kondo, and S. Ogawa, Semiconductor Leading Edge Technologies, Inc., Tsukuba, Japan* **203**

9.4 **A New Perspective of Barrier Material Evaluation and Process Optimization,** L. Zhao, Zs. *Tokei*, G.G. Gischia*, H. Volders*, and G.P. Beyer*, Intel Corp., Leuven, Belgium and *IMEC, Leuven, Belgium*, **206**

SESSION 10: PACKAGING
Co-chairs: Takeshi Furusawa, *Renesas Technology*
and Didier Louis, *CEA/LETI*

10.1 **INVITED – New Trends in Wafer Level Packaging,** *N. Sillon, D. Henry, J-C. Souriau, J. Brun, H. Boutry, and S. Cheramy, CEA-Leti, Grenoble, France* **211**

10.2 **INVITED – Interconnection with Copper Pillar Bumps: Process and Applications,** *C.H. Lee, Amkor Technology Korea, Inc., Seoul, Korea* **214**

10.3 **Impact of Chip Package Interaction on Cu/Ultra Low-k Interconnect Delamination in Flip Chip Package with Large Die,** *C.J. Uchibori and M. Lee, Fujitsu Labs America, Inc., Sunnyvale, CA* **217**

10.4 **SMAFTI Packaging Technology for New Interconnect Hierarchy,** *Y. Kurita, N. Motohashi, S. Matsui, K. Soejima, S. Amakawa*, K.Masu*, and M. Kawano, NEC Electronics Corp., Sagamihara, Japan and *Tokyo Institute of Technology, Yokohama, Japan* **220**

SESSION 11: METROLOGY AND PROCESS CONTROL II
Co-chairs: Mike Shapiro, *IBM*
and Scott List, *SRC*

11.1 **INVITED – Evaluation of Line-Edge Roughness in Cu/Low-k Interconnect Patterns with CD-SEM,** *A. Yamaguchi, D. Ryuzaki, K. Takeda, and H. Kawada*, Hitachi Ltd, Central Research Laboratory, Tokyo, Japan and *Hitachi High Technologies Corp., Ibaraki, Japan* **225**

11.2 **Impact of LER on BEOL Dielectric Reliability: A Quantitative Model and Experimental Validation,** *Zs. Tokei, Ph. Roussel, M Stucchi, J.Versluijs, I. Ciofi, L. Carbonell, G.P. Beyer, A. Cockburn*, M. Agustin**, and K. Shah**, IMEC, Leuven, Belgium, *Applied Materials Belgium, Leuven, Belgium, and **Applied Materials, Santa Clara, CA* **228**

11.3 **A New Physical Model and Experimental Measurements of Copper Interconnect Resistivity Considering Size Effects and Line-Edge Roughness (LER),** *G. Lopez, J. Davis and J. Meindl, Georgia Institute of Technology, Atlanta, GA* **231**

SESSION 12: MATERIALS AND UNIT PROCESSES II
Co-chairs: Shinichi Ogawa, *SELETE*
and Ivo Raaijmakers, *ASM International nv*

12.1 **INVITED – Challenges and Novel Approaches for Photo Resist Removal and Post-Etch Residue Removal for 22nm Interconnects,** *P. Mertens, T.G. Kim, M. Claes, Q.T. Le, G. Vereecke, E. Kesters, S. Suhard, A. Pacco, M. Lux, K. Kenis, A. Urbanowicz, Zs. Tokei, and G. Beyer, IMEC, Leuven, Belgium* **237**

12.2 **In Situ Post Etching Treatment as a Solution To Improve Defect Density For Porous Low-K Integration Using Metallic Hard Masks,** *N. Posseme, R. Bouyssou*, T. Chevolleau*, T. David, V. Arnal**, S. Chhun**, C. Monget**, E. Richard**, D.Galpin**, J.Guillan**, L. Arnaud**, D.Roy**, M Guillermet, J. Ramard**, O. Joubert*, and C.Verove**, CEA-LETI-Minatec, Grenoble, France, *CNRS/LTM, Grenoble, France and **STMicroelectronics, Crolles, France* **240**

12.3 **Advanced Direct-CMUP Process for Porous Low-k Thin Film,** *H. Korogi, H. Chibahara*, S. Suzuki, M. Tsutsue, K. Seo**, Y. Oka*, K. Goto*, M.Akazawa*, H. Miyatake*, S. Matsumoto, and T. Ueda, Panasonic Corp., Kyoto, Japan, *Renesas Technology Group, Itami, Japan, and **Panasonic Semiconductor Engineering Co., Ltd., Kyoto, Japan* **243**

SESSION 13: PROCESS INTEGRATION II

Co-chairs: J.D. Luttmer, *DRS-Infrared Technologies* and Shin-Puu Jeng, *TSMC*

13.1 **Low-k Interconnect Stack with a Novel Self-Aligned Via Patterning Process for 32nm High Volume Manufacturing,** *R. Brain, S. Agrawal, D. Becher, R. Bigwood, M. Buehler, V. Chikarmane, M. Childs, J. Choi, S. Daviess, C. Ganpule, J. He, P. Hentges, I. Jin, S. Klopcic, G. Malyavantham, B. McFadden, J. Neulinger, J. Neirynck, Y. Neirynck, C. Pelto, P. Plekhanov, Y. Shusterman, T. Van, M. Weiss, S.Williams, F. Xia, P. Yashar, and A. Yeoh, Intel Corporation, Hillsboro, OR* **249**

13.2 **Low Resistive and Highly Reliable Copper Interconnects in Combination of Silicide-Cap with Ti-Barrier for 32 nm-Node and Beyond,** *Y. Hayashi, N. Matsunaga, M. Wada, S. Nakao, K. Watanabe, A. Sakata, and H. Shibata, Toshiba Corporation, Yokohama, Japan* **252**

13.3 **Integration and Reliability of CVD Ru Cap for Cu/Low-k Development**, *C.-C. Yang, D.Edelstein**, K.Chanda*, P. Wang*, C.-K. Hu**, E. Liniger**, S. Cohen**, J.R. Lloyd**, B. Li***, F. McFeely**, R.Wisneiff**, T.Ishizaka^, F. Cerio^, K. Suzuki^,, J. Rullan^, A. Selsley^, M Joman^, IBM at Albany Nanotech, Albany, NY, *IBM Semiconductor Research & Development Center, Hopewell Junction, NY,** IBM T.J. Watson Research Center, Yorktown Heights, NY, ***IBM Microelectronics, Essex Junction, VT, and ^TEL Technology Center, Albany, NY* **255**

13.4 **Challenges of Ultra Low-k Integration in BEOL Interconnect for 45nm and Beyond,** *H.Liu, Widodo, S.L. Liew, Z.H. Wang, Y.H. Wang, B.F. Lin, L.Z. Wu, C.S. Seet, W.Lu, C.H. Low, W.P. Liu, M.S. Zhou, L.C. Hsia, Chartered Semiconductor Manufacturing, Ltd., Singapore* **258**