

2009 Symposium on VLSI Circuits

**Kyoto, Japan
16 – 18 June 2009**



**IEEE Catalog Number: CFP09VLS-PRT
ISBN: 978-1-4244-3307-0**

**Copyright © 2009, Japan Society of Applied Physics
All Rights Reserved**

******This publication is a representation of what appears in the IEEE
Digital Libraries. Some format issues inherent in the e-media version may
also appear in this print version.***

IEEE Catalog Number: CFP09VLS-PRT
ISBN 13: 978-1-4244-3307-0

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com

TABLE OF CONTENTS

SESSION 1 – WELCOME AND PLENARY SESSION I

Welcome and Opening Remarks	1
<i>K. Yano, K. Nakamura</i>	
Challenges in Nanoelectronics: Dream or Reality?	2
<i>N. Yokoyama</i>	
Creating Support Circuits for the Nervous System: Considerations for "Brain-Machine" Interfacing	4
<i>A. Csavoy, G. Molnar and T. Denison</i>	

SESSION 2 – CDRS AND LIMITING AMPLIFIERS

A 2 x 22Gb/s SF15.2 CDR/Deserializer in 65nm CMOS Technology	8
<i>N. Nedovic, S. Parikh, A. Kristensson, N. Tzartzanis, W. Walker, S. Reddy, H. Tamura, S. McLeod, T. Yamamoto, Y. Doi, J. Ogawa, M. Kibune, T. Shibasaki, T. Hamada, Y. Tomita, T. Ikeuchi, and N. Kuwata</i>	
Adaptation of CDR and Full Scale Range of ADC-Based SerDes Receiver	10
<i>E.-H. Chen, W. Leven, N. Warke, A. Joy, S. Hubbins, A. Amerasekera and C.-K.K. Yang</i>	
A Reference-Free, Digital Background Calibration Technique for Gated-Oscillator-Based CDR/PLL	12
<i>C.-F. Liang, S.-C. Hwu, Y.-H. Tu, Y.-L. Yang and H.-S. Li</i>	
A Digital Offset-Compensation Scheme for an LA and CDR in 65-nm CMOS	14
<i>S. McLeod, A. Sheikholeslami, T. Yamamoto, N. Nedovic, H. Tamura and W.W. Walker</i>	
A 10-Gb/s Burst-Mode Limiting Amplifier Using a Two-Stage Active Feedback Circuit	16
<i>M. Nogawa, K. Nishimura, J. Terada, M. Nakamura, S. Nishihara and Y. Ohtomo</i>	

SESSION 3 – NON-VOLATILE AND FUSE MEMORIES

Multi-Stacked 1G Cell/Layer Pipe-Shaped BiCS Flash Memory	18
<i>T. Maeda, K. Itagaki, T. Hishida, R. Katsumata, M. Kito, Y. Fukuzumi, M. Kido, H. Tanaka, Y. Komori, M. Ishiduki, J. Matsunami, T. Fujiwara, H. Aochi, Y. Iwata and Y. Watanabe</i>	
Dynamic Vpass ISPP Scheme and Optimized Erase Vth Control for High Program Inhibition in MLC NAND Flash Memories	20
<i>K.-T. Park, M. Kang, S. Hwang, Y. Song, J. Lee, H. Joo, H.-S. Oh, J.-h. Kim, Y.-t. Lee, C. Kim and W. Lee</i>	
Digital Rosetta Stone: A Sealed Permanent Memory with Inductive-Coupling Power and Data Link	22
<i>Y. Yuxiang, N. Miura, S. Imai, H. Ochi and T. Kuroda</i>	
High-Density 3-D Metal-Fuse PROM Featuring 1.37μm^2 1T1R Bit Cell in 32nm High-k Metal-Gate CMOS Technology	24
<i>S.H. Kulkarni, Z. Chen, J. He, L. Jiang, B. Pedersen and K. Zhang</i>	
A 1.25μm^2 Cell 32Kb Electrical Fuse Memory in 32nm CMOS with 700mV Vddmin and Parallel/Serial Interface	26
<i>S. Chung, T.-W. Chung, P.-Y. Ker and F.-L. Hsueh</i>	

SESSION 4 – BIOMEDICAL AND PERSONAL TECHNOLOGY

Asymmetric RF Tags for Ingestible Medication Compliance Capsules	28
<i>H. Yu, C.-M. Tang and R. Bashirullah</i>	
A 490uW Fully MICS Compatible FSK Transceiver for Implantable Devices	30
<i>J. Bae, N. Cho and H.-J. Yoo</i>	
A Super-Regenerative ASK Receiver with $\Delta\Sigma$ Pulse-Width Digitizer and SAR-Based Fast Frequency Calibration for MICS Applications	32
<i>Y.-H. Liu, H.-H. Liu and T.-H. Lin</i>	
A 0.2mm², 27Mbps 3mW ADC/FFT-Less FDM BAN Receiver with Energy Exploitation Capability	34
<i>H. Ishizaki and M. Mizuno</i>	
A Dynamic Real-Time Capacitor Compensated Inductive Coupling Transceiver for Wearable Body Sensor Network	36
<i>S. Lee, J. Yoo, H. Kim and H.-J. Yoo</i>	

SESSION 5 – TRANSMITTERS AND RECEIVERS

A 0.6mW/Gbps, 6.4-8.0Gbps Serial Link Receiver Using Local Injection-Locked Ring Oscillators in 90nm CMOS	38
<i>K. Hu, T. Jiang, J. Wang, F. O'Mahony and P.Y. Chiang</i>	
A 40-Gb/s Transmitter with 4:1 MUX and Subharmonically Injection-Locked CMU in 90-nm CMOS Technology	40
<i>H. Wang and J. Lee</i>	
A 21-Gb/s 87-mW Transceiver with FFE/DFE/Linear Equalizer in 65-nm CMOS Technology	42
<i>H. Wang, C.-C. Lee, A.-M. Lee and J. Lee</i>	
A 12-Gb/s Transceiver in 32-nm Bulk CMOS	44
<i>S. Joshi, J.T.-S. Liao, Y. Fan, S. Hyvonen, M. Nagarajan, J. Rizk, H.-J. Lee and I. Young</i>	
Self-Calibrating Transceiver for Source Synchronous Clocking System with On-Chip TDR and Swing Level Control Scheme	46
<i>Y.-C. Jang, J.-Y. Park, S. Shin, H. Choi, K. Lee, B. Woo, H. Park, W.-S. Kim, Y. Choi, J. Kim, H.-K. Kim, J. Kim, S. Lim, S.-J. Chung, S. Kim, J. Yoo and C. Kim</i>	

SESSION 6 – BIOMEDICAL AND SENSORS

A 190μW-915MHz Active Neural Transponder with 4-Channel Time Multiplexed AFE	48
<i>Z. Xiao, C.-M. Tang, C.-C. Peng, H. Yu and R. Bashirullah</i>	
A 2.6-μW Sub-Threshold Mixed-Signal ECG SoC	50
<i>S.C. Jocke, J.F. Bolus, S.N. Wooters, A.D. Jurik, A.C. Weaver, T.N. Blalock and B.H. Calhoun</i>	
A Micro-Power EEG Acquisition SoC with Integrated Seizure Detection Processor for Continuous Patient Monitoring	52
<i>N. Verma, A. Shoeb, J.V. Guttag and A.P. Chandrakasan</i>	
A CMOS Accelerometer Using Bondwire Inertial Sensing	54
<i>Y.-T. Liao, W. Biederman and B. Otis</i>	

SESSION 7 – SIGMA-DELTA ADCS

A 5th-Order Delta-Sigma Modulator with Single-Opamp Resonator	56
<i>K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, S. Doshio and A. Matsuzawa</i>	
A 500kHz-10MHz Multimode Power-Performance Scalable 83-to-67dB DR CT$\Delta\Sigma$ in 90 nm Digital CMOS with Flexible Analog Core Circuitry	58
<i>P. Crombez, G. Van der Plas, M. Steyaert and J. Craninckx</i>	
Technology Portable, 0.04mm², Ghz-Rate $\Delta\Sigma$ Modulators in 65nm and 45nm CMOS	60
<i>R.H.M. van Veldhoven, N. Nizza and L.J. Breems</i>	
A 79dB 80MHz 8X-OSR Hybrid Delta-Sigma/Pipeline ADC	62
<i>O. Rajaei, T. Musah, S. Takeuchi, M. Aniya, K. Hamashita, P. Hanumolu and U. Moon</i>	

SESSION 8 – SPECIAL NON-VOLATILE MEMORIES

Ferroelectric(Fe)-NAND Flash Memory with Non-Volatile Page Buffer for Data Center Application Enterprise Solid-State Drives (SSD)	64
<i>T. Hatanaka, R. Yajima, T. Horiuchi, S. Wang, X. Zhang, M. Takahashi, S. Sakai and K. Takeuchi</i>	
Fabrication of a Nonvolatile Lookup-Table Circuit Chip Using Magneto/Semiconductor-Hybrid Structure for an Immediate-Power-Up Field Programmable Gate Array	66
<i>D. Suzuki, M. Natsui, S. Ikeda, H. Hasegawa, K. Miura, J. Hayakawa, T. Endoh, H. Ohno and T. Hanyu</i>	
A 5ns Fast Write Multi-Level Non-Volatile 1 K Bits RRAM Memory with Advance Write Scheme	68
<i>S.-S. Sheu, P.-C. Chiang, W.-P. Lin, H.-Y. Lee, P.-S. Chen, Y.-S. Chen, T.-Y. Wu, F.T. Chen, K.-L. Su, M.-J. Kao, K.-H. Cheng and M.-J. Tsai</i>	
32-Mb 2T1R SPRAM with Localized Bi-Directional Write Driver and '1'/'0' Dual-Array Equalized Reference Cell	70
<i>R. Takemura, T. Kawahara, K. Miura, H. Yamamoto, J. Hayakawa, N. Matsuzaki, K. Ono, M. Yamanouchi, K. Ito, H. Takahashi, S. Ikeda, H. Hasegawa, H. Matsuoka and H. Ohno</i>	

SESSION 9 – DATA INTERCONNECT TECHNOLOGY

Crosstalk-Aware PWM-Based On-Chip Global Signaling in 65nm CMOS	72
<i>J.-s. Seo, D. Sylvester and D. Blaauw</i>	
A Simultaneous Tri-Band On-Chip RF-Interconnect for Future Network-on-Chip	74
<i>S.-W. Tam, E. Socher, A. Wong and M.-C.F. Chang</i>	
A 4.7Gb/s Inductive Coupling Interposer with Dual Mode Modem	76
<i>S. Kawai, H. Ishikuro and T. Kuroda</i>	
A Scalable 3D Processor by Homogeneous Chip Stacking with Inductive-Coupling Link	78
<i>Y. Kohama, Y. Sugimori, S. Saito, Y. Hasegawa, T. Sano, K. Kasuga, Y. Yoshida, K. Niitsu, N. Miura, H. Amano and T. Kuroda</i>	

SESSION 10 – PLENARY SESSION II

Future of Mobile Devices - Energy Efficient Sensing, Computing, and Communication	80
<i>T. Ryhänen, Nokia Research Center, and the University of Cambridge</i>	
Human - Area Networking Technology as a Universal Interface – Communications through Natural Human Actions: Touching, Holding, Stepping –	84
<i>Y. Kado</i>	

SESSION 11 – RELIABILITY AND SECURITY

An All-In-One Silicon Odometer for Separately Monitoring HCI, BTI, and TDDB	88
<i>J. Keane, D. Persaud and C.H. Kim</i>	
Post-Silicon Tuning Capabilities of 45nm Low-Power CMOS Digital Circuits	90
<i>M. Meijer, B. Liu, R. van Veen and J.P. de Gyvez</i>	
Tunable Replica Circuits and Adaptive Voltage-Frequency Techniques for Dynamic Voltage, Temperature, and Aging Variation Tolerance	92
<i>J. Tschanz, K. Bowman, S. Walstra, M. Agostinelli, T. Karnik and V. De</i>	
Tunable Duplex LSIs Achieved by Multiple Phase-Modulated Clocks Capable of Predicting Delay-Increase and -Decrease Faults	94
<i>Y. Kameda and M. Mizuno</i>	
Silicon Physical Unclonable Function Resistant to a 10^{25}-Trial Brute Force Attack in 90 nm CMOS	96
<i>S. Stanzione and G. Iannaccone</i>	

SESSION 12 – CLOCK GENERATORS

Multi-Decade Carrier Generation for Cognitive Radios	98
<i>B. Razavi</i>	
A 1.3GHz 350mW Hybrid Direct Digital Frequency Synthesizer in 90nm CMOS	100
<i>H.C. Yeoh, J.-H. Jung, Y.-H. Jung and K.-H. Baek</i>	
A Bandwidth Tracking Technique for a 65nm CMOS Digital Phase-Locked Loop	102
<i>P.-H. Hsieh, J. Maxey and C.-K. Ken Yang</i>	
CMOS Frequency Generation System for W-Band Radars	104
<i>N. Zhang and K.K. O</i>	
A 5GHz Phase-Locked Loop Using Dynamic Phase-Error Compensation Technique for Fast Settling in 0.18-μm CMOS	106
<i>W.-H. Chiu, Y.-H. Huang and T.-H. Lin</i>	

SESSION 13 – DRAM AND INTERFACE

A 31ns Random Cycle VCAT-Based 4F² DRAM with Enhanced Cell Efficiency	108
<i>K.-W. Song, J.-Y. Kim, H. Kim, H.-W. Chung, H. Kim, K. Kim, H.-W. Park, H.C. Kang, S. Kim, N.-k. Tak, D. Park, W.-S. Kim, Y.-T. Lee, Y.C. Oh, G.-Y. Jin, J. Yoo, K. Oh, C. Kim and W.-S. Lee</i>	
A Sub-0.9V Logic-Compatible Embedded DRAM with Boosted 3T Gain Cell, Regulated Bit-Line Write Scheme and PVT-Tracking Read Reference Bias	110
<i>K.C. Chun, P. Jain, J.H. Lee and C.H. Kim</i>	

A 4.3GB/s Mobile Memory Interface With Power-Efficient Bandwidth Scaling	112
<i>R. Palmer, J. Poulton, B. Leibowitz, Y. Frans, S. Li, A. Fuller, J. Eyles, J. Wilson, M. Aleksic, T. Greer, M. Bucher and N. Nguyen</i>	
Wide-Range Fast-Lock Duty-Cycle Corrector with Offset-Tolerant Duty-Cycle Detection Scheme for 54nm 7Gb/s GDDR5 DRAM Interface	114
<i>D. Shin, K.-J. Na, D. Kwon, J.-H. Kang, T. Song, H.-D. Jung, W.-Y. Lee, K.-C. Park, J.-H. Park, Y.-S. Joo, J.-H. Cha, Y. Jung, Y. Kim, D. Han, B.-J. Choi, G.-I. Lee, J.-H. Cho and Y.-J. Choi</i>	

SESSION 14 – DISCRETE-TIME ANALOG

A Highly Reconfigurable 400-1700MHz Receiver Using a Down-Converting Sigma-Delta A/D with 59-dB SNR and 57-dB SFDR Over 4-MHz Bandwidth	116
<i>R. Winoto and B. Nikolić</i>	
A RF Receiver Front-End with Adaptive Discrete-Time Charge-Transfer Filter and Passive Gain-Boosting in 90nm CMOS	118
<i>M.-C. Lee, K. Muhammad and C.-M. Hung</i>	
A 1.28mW 100Mb/s Impulse UWB Receiver with Charge-Domain Correlator and Embedded Sliding Scheme for Data Synchronization	120
<i>L. Liu, T. Sakurai and M. Takamiya</i>	
A 73.1dB SNDR Digitally Assisted Sub-sampler for RF Power Amplifier Linearization Systems	122
<i>S.W. Chung and J.L. Dawson</i>	

SESSION 15 – SRAMS AND CLOCK CIRCUITS

A 45nm 24MB On-Die L3 Cache for the 8-Core Multi-Threaded Xeon® Processor	124
<i>J. Chang, S.-L. Chen, W. Chen, S. Chiu, R. Faber, R. Ganesan, M. Grgek, V. Lukka, W.W. Mar, J. Vash, S. Rusu and K. Zhang</i>	
Clock Generation & Distribution for a 45nm, 8-Core Xeon® Processor with 24MB Cache	126
<i>S. Tam, J. Leung and R. Limaye</i>	
A Differential Data Aware Power-Supplied (D²AP) 8T SRAM Cell with Expanded Write/Read Stabilities for Lower VDDmin Applications	128
<i>M.-F. Chang, J.-J. Wu, K.-T. Chen and H. Yamauchi</i>	
A 45nm 0.6V Cross-Point 8T SRAM with Negative Biased Read/Write Assist	130
<i>M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Ohbayashi, Y. Nakase and H. Shinohara</i>	

SESSION 16 – DC/DC CONVERTERS

20mV Input Boost Converter for Thermoelectric Energy Harvesting	132
<i>E. Carlson, K. Strunz and B. Otis</i>	
Single-Inductor Dual Buck-Boost Output (SIDBBO) Converter with Adaptive Current Control Mode (ACCM) and Adaptive Body Switch (ABS) for Compact Size and Long Battery Life in Portable Devices	134
<i>M.-H. Huang and K.-H. Chen</i>	
A Hybrid DC-DC Converter for Sub-Microwatt Sub-1V Implantable Applications	136
<i>M. Wieckowski, G.K. Chen, M. Seok, D. Blaauw and D. Sylvester</i>	
High-Efficiency, 12V-to-1.5V DC-DC Converter Realized with Switched-Capacitor Architecture	138
<i>V.W. Ng, M.D. Seeman and S.R. Sanders</i>	

RUMP SESSIONS

Summary	140
----------------------	-----

SESSION 17 – IMAGE SENSORS

A 0.45-0.7V Sub-Microwatt CMOS Image Sensor for Ultra-Low Power Applications	142
<i>S. Hanson and D. Sylvester</i>	
A 0.75V CMOS Image Sensor Using Time-Based Readout Circuit	144
<i>K. Cho, D. Lee, J. Lee and G. Han</i>	

A Color-Independent Saturation, Linear Response, Wide Dynamic Range CMOS Image Sensor With Retinal Rod- and Cone-Like Color Pixels	146
<i>S. Kawada, S. Sakai, N. Akahane, K. Mizobuchi and S. Sugawa</i>	
A CMOS Image Sensor With 2.5-e^- Random Noise and 110-ke^- Full Well Capacity Using Column Source Follower Readout Circuits	148
<i>T. Kohara, W. Lee, N. Akahane, K. Mizobuchi and S. Sugawa</i>	

SESSION 18 – FREQUENCY SYNTHESIZERS

A Compact 0.8-6GHz Fractional-N PLL with Binary-Weighted D/A Differentiator and Offset-Frequency Δ-Σ Modulator for Noise and Spurs Cancellation	150
<i>H.-Y. Jian, Z. Xu, Y.-C. Wu and F. Chang</i>	
A 320fs-RMS-Jitter and 300kHz-BW All-Digital Fractional-N PLL with Self-Corrected TDC and Fast Temperature Tacking Loop for WiMax/WLAN 11n	152
<i>H.-H. Chang, C.-H. Fu and M. Chiu</i>	
A Direct Digital Frequency Modulation PLL with All Digital On-Line Self-Calibration for Quad-Band GSM/GPRS Transmitter	154
<i>C.-H. Wang, P.-Y. Wang, L.-W. Ke, D.-Y. Yu, B.-H. Ong, C.-H. Sun, H.-H. Chen, Y.-Y. Chen, C.-M. Kuo, J.-C. Lin, T.-P. Wang and Y.-H. Chen</i>	
A Low-Voltage, 9-GHz, 0.13-μm CMOS Frequency Synthesizer with a Fractional Phase-Rotating and Frequency-Doubling Topology	156
<i>C.-H. Chang and C.-Y. Yang</i>	

SESSION 19 – POWER MANAGEMENT AND HIGH-EFFICIENCY LOGIC

Multi-Phase 1GHz Voltage Doubler Charge-Pump in 32nm Logic Process	158
<i>D. Somasekhar, B. Srinivasan, G. Pandya, F. Hamzaoglu, M. Khellah, T. Karnik and K. Zhang</i>	
A 82% Efficiency 0.5% Ripple 16-Phase Fully Integrated Capacitive Voltage Doubler	160
<i>T.V. Breussegem and M. Steyaert</i>	
Dual-Power-Path RF-DC Multi-Output Power Management Unit for RFID Tags	162
<i>J. Yi, W.-H. Ki, P.K.T. Mok and C.-Y. Tsui</i>	
A 187MHz Subthreshold-Supply Robust FIR Filter with Charge-Recovery Logic	164
<i>W.-H. Ma, J.C. Kao, V.S. Sathe, and M. Papaefthymiou</i>	

SESSION 20 – ANALOG TECHNIQUES

A 28.1dBm Class-D Outphasing Power Amplifier in 45nm LP Digital CMOS	166
<i>H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. Elmala and K. Soumyanath</i>	
Time Difference Amplifier Using Closed-Loop Gain Control	168
<i>T. Nakura, S. Mandai, M. Ikeda and K. Asada</i>	
A Chopper and Auto-Zero Offset-Stabilized CMOS Instrumentation Amplifier	170
<i>J.F. Witte, J.H. Huijsing and K.A.A. Makinwa</i>	
Complex IIP2 Improvement Through Active Cancellation of LO Leakage	172
<i>H. Choo, K. Muhammad and M.-C. Lee</i>	

SESSION 21 – ADVANCED EQUALIZERS

A 19Gb/s 38mW 1-Tap Speculative DFE Receiver in 90nm CMOS	174
<i>D.Z. Turker, A. Rylyakov, D. Friedman, S. Gowda and E. Sánchez-Sinencio</i>	
A 40Gb/s Decision Feedback Equalizer Using Back-Gate Feedback Technique	176
<i>C.-L. Hsieh and S.-I. Liu</i>	
A Data Pattern-Tolerant Adaptive Equalizer Using Spectrum Balancing Method	178
<i>H.-Y. Joo, K.-S. Ha and L.-S. Kim</i>	
A Fractionally Spaced Linear Receive Equalizer with Voltage-to-Time Conversion	180
<i>S. Song, B. Kim and V. Stojanović</i>	

SESSION 22 – CLOCK GENERATION TECHNIQUES

A 10MHz 80μW 67 ppm/$^{\circ}$C CMOS Reference Clock Oscillator with a Temperature Compensated Feedback Loop in 0.18μm CMOS	182
<i>J. Lee and S.H. Cho</i>	
A 0.114-mW Dual-Conduction Class-C CMOS VCO with 0.2-V Power Supply	184
<i>K. Okada, Y. Nomiyama, R. Murakami and A. Matsuzawa</i>	
A 132.7-to-143.5GHz Injection-Locked Frequency Divider in 65nm CMOS	186
<i>B.-Y. Lin and S.-I. Liu</i>	
A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13μm CMOS Technology	188
<i>J. Yu, F.F. Dai and R.C. Jaeger</i>	

SESSION 23 – LOW POWER ADCS

A 0.92mW 10-Bit 50-MS/s SAR ADC in 0.13μm CMOS Process	190
<i>C.-C. Liu, S.-J. Chang, G.-Y. Huang and Y.-Z. Lin</i>	
A 6-Bit 50-MS/s Threshold Configuring SAR ADC in 90-nm Digital CMOS	192
<i>P. Nuzzo, C. Nani, C. Armiento, A. Sangiovanni-Vincentelli, J. Craninckx and G.V. der Plas</i>	
A 12b 11MS/s Successive Approximation ADC with Two Comparators in 0.13μm CMOS	194
<i>J.J. Kang, and M.P. Flynn</i>	
A 1.3μW 0.6V 8.7-ENOB Successive Approximation ADC in a 0.18μm CMOS	196
<i>S.-K. Lee, S.-J. Park, Y. Suh, H.-J. Park and J.-Y. Sim</i>	

SESSION 24 – MM-WAVE TECHNIQUES

A 77 GHz 90 nm CMOS Transceiver for FMCW Radar Applications	198
<i>T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, O. Watanabe and I. Seto</i>	
60-GHz Hybrid Transmit/Receive Switch Using p-n Diode and MOS Transistors	200
<i>C. Mao and K.K. O</i>	
60GHz RF-Path Phase-Shifting Two-Element Phased-Array Front-End in Silicon	202
<i>A. Natarajan, M.-D. Tsai and B. Floyd</i>	
36mW 63GHz CMOS Differential Low-Noise Amplifier with 14GHz Bandwidth	204
<i>Y. Natsukari and M. Fujishima</i>	

SESSION 25 – MEDIA PROCESSOR ARCHITECTURE

3D System Integration of Processor and Multi-Stacked SRAMs by Using Inductive-Coupling Links	206
<i>K. Osada, M. Saen, Y. Okuma, K. Niitsu, Y. Shimazaki, Y. Sugimori, Y. Kohama, K. Kasuga, I. Nonomura, N. Irie, T. Hattori, A. Hasegawa and T. Kuroda</i>	
A 116fps 74mW Mobile Heterogeneous 3D-Media Processor for 3D Display Contents	208
<i>S.-H. Kim, H.-Y. Kim, Y.-J. Kim, K. Chung, D. Kim and L.-S. Kim</i>	
A 22.8GOPS 2.83mW Neuro-Fuzzy Object Detection Engine for Fast Multi-Object Recognition	210
<i>M. Kim, J.-Y. Kim, S. Lee, J. Oh and H.-J. Yoo</i>	
A 1080p@60fps Multi-Standard Video Decoder Chip Designed for Power and Cost Efficiency in a System Perspective	212
<i>D. Zhou, Z. You, J. Zhu, J. Kong, Y. Hong, X. Chen, X. He, C. Xu, H. Zhang, J. Zhou, N. Deng, P. Liu and S. Goto</i>	

SESSION 26 – HIGH-SPEED ADCS

A Self-Background Calibrated 6b 2.7GS/s ADC with Cascade-Calibrated Folding-Interpolating Architecture	214
<i>Y. Nakajima, A. Sakaguchi, T. Ohkido, T. Matsumoto and M. Yotsuyanagi</i>	
A 7.5-GS/s 3.8-ENOB 52-mW Flash ADC with Clock Duty Cycle Control in 65nm CMOS	216
<i>H. Chung, A. Rylyakov, Z.T. Deniz, J. Bulzacchelli, G.-Y. Wei and D. Friedman</i>	
A 1.5-GHz 63dB SNR 20mW Direct RF Sampling Bandpass VCO-Based ADC in 65nm CMOS	218
<i>Y.-G. Yoon and S.H. Cho</i>	

A Dual-Channel 10b 80MS/s Pipeline ADC with 0.16mm² Area in 65nm CMOS	220
<i>X. Yu, F. Lin, K. Li, S. Ranganathan and T. Kwan</i>	

SESSION 27 – WIRELESS TRANSCEIVERS

528mW Zero-IF Full-Segment ISDB-T CMOS Tuner with 10th-Order Channel Filters	222
<i>T. Kamata, K. Okui, M. Fukasawa, K. Tanaka, C. Go, N. Motoyama, T. Matsuoka and K. Taniguchi</i>	
A 2 x V_{DD}-Enabled TV-Tuner RF Front-End Supporting TV-GSM Interoperation in 90nm CMOS	224
<i>P.-I. Mak and R.P. Martins</i>	
A Frequency Translation Technique for SAW-Less 3G Receivers	226
<i>A. Mirzaei, X. Chen, A. Yazdi, J. Chiu, J. Leete and H. Darabi</i>	
A 4-Stream 802.11n Baseband Transceiver in 0.13 μm CMOS	228
<i>A. Burg, S. Haene, M. Borgmann, D. Baum, T. Thaler, F. Carbognani, S. Zwicky, L. Barbero, C. Senning, P. Greisen, T. Peter, C. Foelml, U. Schuster, P. Tejera and A. Staudacher</i>	

SESSION 28 – SIGNAL PROCESSING

A 47 Gb/s LDPC Decoder with Improved Low Error Rate Performance	230
<i>Z. Zhang, V. Anantharam, M.J. Wainwright and B. Nikolić</i>	
A 188-size 2.1mm² Reconfigurable Turbo Decoder Chip with Parallel Architecture for 3GPP LTE System	232
<i>C.-C. Wong, Y.-Y. Lee and H.-C. Chang</i>	
A 58-μW Single-Chip Sensor Node Processor Using Synchronous MAC Protocol	234
<i>T. Takeuchi, S. Izumi, T. Matsuda, H. Lee, Y. Otake, T. Konishi, K. Tsuruda, Y. Sakai, H. Fujiwara, C. Ohta, H. Kawaguchi and M. Yoshimoto</i>	
A 200Mbps+ 2.14nJ/b Digital Baseband Multi Processor System-on-Chip for SDRs	236
<i>V. Derudder, B. Bougard, A. Couvreur, A. Dewilde, S. Dupont, L. Folens, L. Hollevoet, F. Naessens, D. Novo, P. Raghavan, T. Schuster, K. Stinkens, J.-W. Weijers and L. Van der Perre</i>	

SPECIAL SESSION

No Papers are Available from this Session

Author Index