

# **2009 46th ACM/IEEE Design Automation Conference**

**(DAC 2009)**

**San Francisco, CA, USA  
26 – 31 July 2009**

**Pages 1-471**



**IEEE Catalog Number: CFP09DAC-PRT  
ISBN: 978-1-60558-497-3**

# TABLE OF CONTENTS

## SESSION 1 – PANEL

<b>PANEL: System Prototypes: Virtual, Hardware or Hybrid?</b> .....	1
---	---

*N/A*

## SESSION 2 – SPECIAL SESSION:

### MECHANISMS FOR SURVIVING UNCERTAINTY: OPPORTUNITIES AND PROSPECTS

<b>Circuit Techniques for Dynamic Variation Tolerance</b> .....	4
<i>Keith Bowman, James Tschanz, Chris Wilkerson, Shih-Lien Lu, Tanay Karnik, Vivek De, Shekhar Borkar</i>	
<b>Enabling Adaptability Through Elastic Clocks</b> .....	8
<i>Emre Tuncer, Jordi Cortadella, Luciano Lavagno</i>	
<b>Addressing Design Margins Through Error-Tolerant Circuits</b> .....	11
<i>Shidhartha Das, David Blaauw, David Bull, Krisztián Flautner, Rob Aitken</i>	

## SESSION 3 – COMBATING NON-IDEALITIES IN STATIC TIMING ANALYSIS

<b>Worst-Case Aggressor-Victim Alignment with Current-Source Driver Models</b> .....	13
<i>Ravikishore Gandikota, Li Ding, Peivand Tehrani, David Blaauw</i>	
<b>A Moment-Based Effective Characterization Waveform for Static Timing Analysis</b> .....	19
<i>David Ling, Chandu Visweswariah, Peter Feldmann, Soroush Abbaspour</i>	
<b>A False-Path Aware Formal Static Timing Analyzer Considering Simultaneous Input Transitions</b> .....	25
<i>Shihheng Tsai, Chung-Yang Huang</i>	

## SESSION 4 – HIGH-PERFORMANCE PLATFORMS: ADVANCES IN SYSTEM-LEVEL EXPLORATION AND OPTIMIZATION

<b>Way Stealing: Cache-Assisted Automatic Instruction Set Extensions</b> .....	31
<i>Theo Kluter, Philip Brisk, Paolo Ienne, Edoardo Charbon</i>	
<b>SysCOLA: A Framework for Co-Development of Automotive Software and System Platform</b> .....	37
<i>Zhonglei Wang, Andreas Herkersdorf, Wolfgang Haberl, Martin Wechs</i>	
<b>Designing Heterogeneous ECU Networks via Compact Architecture Encoding and Hybrid Timing Analysis</b> .....	43
<i>Michael Glaß, Martin Lukasiewicz, Jürgen Teich, Unmesh D. Bordoloi, Samarjit Chakraborty</i>	
<b>Optimizing Throughput of Power- and Thermal-Constrained Multicore Processors Using DVFS and Per-Core Power-Gating</b> .....	47
<i>Jungseob Lee, Nam Sung Kim</i>	

## SESSION 5 – NOVEL DESIGN AND VERIFICATION METHODOLOGIES

<b>Design Automation for a 3DIC FFT Processor for Synthetic Aperture Radar: A Case Study</b> .....	51
<i>Thorlindur Thorolfsson, Kiran Gonsalves, Paul D. Franzon</i>	
<b>Selective Wordline Voltage Boosting for Caches to Manage Yield under Process Variations</b> .....	57
<i>Yan Pan, Joonho Kong, Serkan Ozdemir, Gokhan Memik, Sung Woo Chung</i>	
<b>Double Patterning Lithography Friendly Detailed Routing with Redundant via Consideration</b> .....	63
<i>Kun Yuan, Katrina Lu, David Z. Pan</i>	
<b>Use of Lithography Simulation for the Calibration of Equation-Based Design Rule Checks</b> .....	67
<i>David Abercrombie, Fedor Pikus, Cosmin Cazan</i>	

## **SESSION 6 – DESIGN AND OPTIMIZATION OF NANOCIRCUITS**

<b>Carbon Nanotube Circuits in the Presence of Carbon Nanotube Density Variations .....</b>	<b>71</b>
<i>Jie Zhang, Nishant Patil, Arash Hazeghi, Subhasish Mitra</i>	
<b>Decoding Nanowire Arrays Fabricated with the Multi-Spacer Patterning Technique.....</b>	<b>77</b>
<i>M. Haykel Ben Jamaa, Yusuf Leblebici, Giovanni De Micheli</i>	
<b>Boolean Logic Function Synthesis for Generalized Threshold Gate Circuits.....</b>	<b>83</b>
<i>Marek Bawiec, Maciej Nikodem</i>	
<b>Improving STT MRAM Storage Density Through Smaller-Than-Worst-Case Transistor Sizing .....</b>	<b>87</b>
<i>Wei Xu, Yiran Chen, Xiaobin Wang, Tong Zhang</i>	

## **SESSION 7 – PANEL**

<b>PANEL: EDA in Flux: Should I Stay or Should I Go?.....</b>	<b>91</b>
<i>N/A</i>	

## **SESSION 8 – SPECIAL SESSION: DAWN OF THE 22NM DESIGN ERA – YES WE CAN!**

<b>Design Perspectives on 22nm CMOS and Beyond .....</b>	<b>93</b>
<i>Shekhar Borkar</i>	
<b>Creating an Affordable 22nm Node Using Design-Lithography Co-Optimization .....</b>	<b>95</b>
<i>Andrzej Strojwas, Tejas Jhaveri, Vyacheslav Rovner, Lawrence T. Pileggi</i>	
<b>Device/Circuit Interactions at 22nm Technology Node .....</b>	<b>97</b>
<i>Kaushik Roy, Jaydeep P. Kulkarni, Sumeet Kumar Gupta</i>	
<b>Beyond Innovation: Dealing with the Risks and Complexity of Processor Design in 22nm .....</b>	<b>103</b>
<i>Carl J. Anderson</i>	

## **SESSION 9 – STATISTICAL METHODS IN STATIC TIMING ANALYSIS**

<b>Physically Justifiable Die-Level Modeling of Spatial Variation in View of Systematic Across Wafer Variability .....</b>	<b>104</b>
<i>Lerong Cheng, Puneet Gupta, Lei He, Costas Spanos, Kun Qian</i>	
<b>A Gaussian Mixture Model for Statistical Timing Analysis.....</b>	<b>110</b>
<i>Shingo Takahashi, Yuki Yoshida, Shuji Tsukiyama</i>	
<b>A Stochastic Jitter Model for Analyzing Digital Timing-Recovery Circuits .....</b>	<b>116</b>
<i>James R. Burnham, Chih-Kong Ken Yang, Haitham Hindi</i>	
<b>Statistical Ordering of Correlated Timing Quantities and its Application for Path Ranking.....</b>	<b>122</b>
<i>Jinjun Xiong, Chandu Visweswariah, Vladimir Zolotov</i>	
<b>A Parametric Approach for Handling Local Variation Effects in Timing Analysis .....</b>	<b>126</b>
<i>Ayhan Mutlu, Jiayong Le, Ruben Molina, Mustafa Celik</i>	

## **SESSION 10 – PROFILING, TEST AND DEBUG OF EMBEDDED SYSTEMS**

<b>Non-Intrusive Dynamic Application Profiling for Multitasked Applications.....</b>	<b>130</b>
<i>Karthik Shankar, Roman Lysecky</i>	
<b>A Trace-Capable Instruction Cache for Cost Efficient Real-Time Program Trace Compression in SOC.....</b>	<b>136</b>
<i>Chun-Hung Lai, Fu-Ching Yang, Chung-Fu Kao, Ing-Jer Huang</i>	
<b>Generating Test Programs to Cover Pipeline Interactions .....</b>	<b>142</b>
<i>Thanh Nga Dang, Abhik Roychoudhury, Tulika Mitra, Prabhat Mishra</i>	
<b>NUDA: A Non-Uniform Debugging Architecture and Non-Intrusive Race Detection for Many-Core .....</b>	<b>148</b>
<i>Chi-Neng Wen, Shu-Hsuan Chou, Tien-Fu Chen, Alan Peisheng Su</i>	

## **SESSION 11 – LOW-POWER DESIGN AND ANALYSIS TECHNIQUES**

<b>Efficient Smart Sampling Based Full-Chip Leakage Analysis for Intra-Die Variation Considering State Dependence.....</b>	<b>154</b>
<i>Vineeth Veetil, Dennis Sylvester, David Blaauw, Saumil Shah, Steffen Rochel</i>	

<b>Resurrecting Infeasible Clock-Gating Functions</b> .....	160
<i>Eli Arbel, Cindy Eisner, Oleg Rokhlenko</i>	
<b>Low-Power Gated Bus Synthesis Using Shortest-Path Steiner Graph for System-On-Chip Communications</b> .....	166
<i>Renshen Wang, Nan-Chi Chou, Bill Salefski, Chung-Kuan Cheng</i>	
<b>ActivaSC: A Highly Efficient and Non-Intrusive Extension for Activity-Based Analysis of SystemC Models</b> .....	172
<i>Cedric Walravens, Yves Vanderperren, Wim Dehaene</i>	

## **SESSION 12 – DESIGN INTEGRITY CHALLENGES**

<b>GPU Friendly Fast Poisson Solver for Structured Power Grid Network Analysis</b> .....	178
<i>Jin Shi, Yici Cai, Wenting Hou, Liwei Ma, Sheldon X.-D. Tan, Pei-Hsin Ho, Xiaoyi Wang</i>	
<b>Fast Vectorless Power Grid Verification Using an Approximate Inverse Technique</b> .....	184
<i>Nahi H. Abdul Ghani, Farid N. Najm</i>	
<b>Computing Bounds for Fault Tolerance Using Formal Techniques</b> .....	190
<i>Görschwin Fey, André Sülflow, Rolf Drechsler</i>	
<b>Clock Skew Optimization via Wiresizing for Timing Sign-Off Covering All Process Corners</b> .....	196
<i>Sari Onaissi, Khaled R. Heloue, Farid N. Najm</i>	

## **SESSION 13 – PANEL**

<b>PANEL: Moore's Law: Another Casualty of the Financial Meltdown?</b> .....	202
<i>N/A</i>	

## **SESSION 14 – SPECIAL SESSION:**

### **VERIFYING AN SOC MONSTER: WHOSE JOB IS IT ANYWAY?**

<b>Holistic Verification: Myth or Magic Bullet?</b> .....	204
<i>Pradip A. Thaker</i>	
<b>Verification Problems in Reusing Internal Design Components</b> .....	209
<i>Warren Stapleton, Paul Tobin</i>	
<b>Exploiting “Architecture for Verification” to Streamline the Verification Process</b> .....	212
<i>David Whipp</i>	
<b>Role of the Verification Team Throughout the ASIC Development Life Cycle</b> .....	216
<i>Eric Chesters</i>	

## **SESSION 15 – TIMING SIMULATION: OPTIMIZED EMBEDDED SOFTWARE AND MPSOCS**

<b>An Efficient Approach for System-Level Timing Simulation of Compiler-Optimized Embedded Software</b> .....	220
<i>Zhonglei Wang, Andreas Herkersdorf</i>	
<b>MPTLsim: A Simulator for X86 Multicore Processors</b> .....	226
<i>Hui Zeng, Matt Yourst, Kanad Ghose, Dmitry Ponomarev</i>	
<b>Trace-Driven Workload Simulation Method for Multiprocessor System-On-Chips</b> .....	232
<i>Tsuyoshi Isshiki, Dongju Li, Hiroaki Kunieda, Toshio Isomura, Kazuo Satou</i>	

## **SESSION 16 – ADVANCES IN EMBEDDED SYSTEM MODELING AND OPTIMIZATION**

<b>Analysis and Mitigation of Process Variation Impacts on Power-Attack Tolerance</b> .....	238
<i>Lang Lin, Wayne Burleson</i>	
<b>Evaluating Design Trade-Offs in Customizable Processors</b> .....	244
<i>Unmesh D. Bordoloi, Huynh Phung Huynh, Samarjit Chakraborty, Tulik Mitra</i>	
<b>A Design Flow for Application Specific Heterogeneous Pipelined Multiprocessor Systems</b> .....	250
<i>Haris Javaid, Sri Parameswaran</i>	
<b>Xquasher: A Tool for Efficient Computation of Multiple Linear Expressions</b> .....	254
<i>Arash Arfaee, Ali Irturk, Nikolay Laptev, Farzan Fallah, Ryan Kastner</i>	

**SESSION 17 – INTERCONNECT OPTIMIZATION FOR EMERGING TECHNOLOGIES**

**ILP-Based Pin-Count Aware Design Methodology for Microfluidic Biochips** ..... 258  
*Cliff Chiung-Yu Lin, Yao-Wen Chang*

**O-Router: An Optical Routing Framework for Low-Power On-Chip Silicon Nano-Photonics Integration** ..... 264  
*Duo Ding, Yilin Zhang, Haiyu Huang, Ray T. Chen, David Z. Pan*

**BDD-Based Synthesis of Reversible Logic for Large Functions** ..... 270  
*Robert Wille, Rolf Drechsler*

**SESSION 18 – DESIGN FLEXIBILITY: BEND IT, SHAPE IT, ANYWAY YOU WANT IT!**

**Soft Connections: Addressing the Hardware-Design Modularity Problem** ..... 276  
*Michael Pellauer, Michael Adler, Derek Chiou, Joel Emer*

**A Computing Origami: Folding Streams in FPGAs** ..... 282  
*Andrei Hagiescu, Weng-Fai Wong, David F. Bacon, Rodric M. Rabbah*

**Retiming and Recycling for Elastic Systems with Early Evaluation** ..... 288  
*Dmitry E. Bufistov, Jordi Cortadella, Marc Galceran-Oms, Jorge Júlvez, Michael Kishinevsky*

**Speculation in Elastic Systems** ..... 292  
*Marc Galceran-Oms, Jordi Cortadella, Mike Kishinevsky*

**SESSION 19 – PANEL**

**PANEL: DFM - Band-Aid or Competitive Weapon?** ..... 296  
*N/A*

**SESSION 20 – SPECIAL SESSION:**

**EMERGING TECHNOLOGIES: BLUE-SKY RESEARCH OR CMOS REPLACEMENT?**

**The Semiconductor Industry’s Nanoelectronics Research Initiative: Motivation and Challenges** ..... 298  
*Jeff Welsler*

**Single-Electron Devices for Ubiquitous and Secure Computing Applications** ..... 301  
*Ken Uchida*

**Digital VLSI Logic Technology Using Carbon Nanotube FETs: Frequently Asked Questions** ..... 304  
*Nishant Patil, Albert Lin, Jie Zhang, H.-S. Philip Wong, Subhasish Mitra*

**CMOS Scaling Beyond 32nm: Challenges and Opportunities** ..... 310  
*Kelin J. Kuhn*

**SESSION 21 – ROUTING: FROM CHIP TO PACKAGE**

**An  $O(n \log n)$  Path-Based Obstacle-Avoiding Algorithm for Rectilinear Steiner Tree Construction** ..... 314  
*Chih-Hung Liu, Shih-Yi Yuan, Sy-Yen Kuo, Yao-Hsin Chou*

**GRIP: Scalable 3-D Global Routing Using Integer Programming** ..... 320  
*Tai-Hsuan Wu, Azadeh Davoodi, Jeffrey T. Linderoth*

**Automatic Bus Planner For Dense PCBs** ..... 326  
*Hui Kong, Tan Yan, Martin D. F. Wong*

**A Correct Network Flow Model for Escape Routing** ..... 332  
*Tan Yan, Martin D. F. Wong*

**Flip-Chip Routing with Unified Area-I/O Pad Assignments for Package-Board Co-Design** ..... 336  
*Jia-Wei Fang, Martin D. F. Wong, Yao-Wen Chang*

**SESSION 22 – SPEED PATH IDENTIFICATION AND SILICON DEBUG**

**Statistical Multilayer Process Space Coverage for At-Speed Test** ..... 340  
*Jinjun Xiong, Yiyu Shi, Vladimir Zolotov, Chandu Visweswariah*

**Speedpath Analysis Based on Hypothesis Pruning and Ranking** ..... 346  
*Nicholas Callegari, Li-C. Wang, Pouria Bastani*

<b>Interconnection Fabric Design for Tracing Signals in Post-Silicon Validation</b> .....	352
<i>Xiao Liu, Qiang Xu</i>	
<b>Online Cache State Dumping for Processor Debug</b> .....	358
<i>Anant Vishnoi, Preeti Ranjan Panda, M. Balakrishnan</i>	

### **SESSION 23 – ANALOG/RF SIMULATION AND STATISTICAL MODELING**

<b>Finding Deterministic Solution from Underdetermined Equation: Large-Scale Performance Modeling by Least Angle Regression</b> .....	364
<i>Xin Li</i>	
<b>A Robust and Efficient Harmonic Balance (HB) Using Direct Solution of HB Jacobian</b> .....	370
<i>Amit Mehrotra, Abhishek Somani</i>	
<b>Stochastic Steady-State and AC Analyses of Mixed-Signal Systems</b> .....	376
<i>Jaeha Kim, Jihong Ren, Mark A. Horowitz</i>	
<b>Parallelizable Stable Explicit Numerical Integration for Efficient Circuit Simulation</b> .....	382
<i>Wei Dong, Peng Li</i>	
<b>Efficient Design-Specific Worst-Case Corner Extraction for Integrated Circuits</b> .....	386
<i>Hong Zhang, Tsung-Hao Chen, Ming-Yuan Ting, Xin Li</i>	

### **SESSION 24 – RECENT ADVANCES IN TIMING, ECO AND LOGIC OPTIMIZATION**

<b>Timing-Driven Optimization Using Lookahead Logic Circuits</b> .....	390
<i>Mihir Choudhury, Kartik Mohanram</i>	
<b>Simulation and SAT-Based Boolean Matching for Large Boolean Networks</b> .....	396
<i>Kuo-Hua Wang, Chung-Ming Chan, Jung-Chang Liu</i>	
<b>New Spare Cell Design for IR Drop Minimization in Engineering Change Order</b> .....	402
<i>Hsien-Te Chen, Chieh-Chun Chang, TingTing Hwang</i>	
<b>Matching-Based Minimum-Cost Spare Cell Selection for Design Changes</b> .....	408
<i>Iris Hui-Ru Jiang, Hua-Yu Chang, Liang-Gi Chang, Huang-Bi Hung</i>	
<b>Handling Don't-Care Conditions in High-Level Synthesis and Application for Reducing Initialized Registers</b> .....	412
<i>Hong-Zu Chou, Kai-Hui Chang, Sy-Yen Kuo</i>	

### **SESSION 25 – PANEL**

<b>PANEL: Oil Fields, Hedge Funds and Drugs</b> .....	416
<i>N/A</i>	

### **SESSION 26 – SPECIAL SESSION: COMPUTATION IN THE POST-TURING ERA**

<b>Human Computation</b> .....	418
<i>Luis von Ahn</i>	
<b>How to Make Computers That Work Like the Brain</b> .....	420
<i>Dileep George</i>	

### **SESSION 27 – ADVANCES IN PHYSICAL SYNTHESIS**

<b>A Fully Polynomial Time Approximation Scheme for Timing Driven Minimum Cost Buffer Insertion</b> .....	424
<i>Shiyan Hu, Zhuo Li, Charles J. Alpert</i>	
<b>Spare-Cell-Aware Multilevel Analytical Placement</b> .....	430
<i>Zhe-Wei Jiang, Meng-Kai Hsu, Yao-Wen Chang, Kai-Yuan Chao</i>	
<b>Handling Complexities in Modern Large-Scale Mixed-Size Placement</b> .....	436
<i>Jackey Z. Yan, Natarajan Viswanathan, Chris Chu</i>	
<b>RegPlace: A High Quality Open-Source Placement Framework for Structured ASICs</b> .....	442
<i>Ashutosh Chakraborty, Anurag Kumar, David Z. Pan</i>	

## **SESSION 28 – JUMPING THE HIGH-LEVEL VERIFICATION HURDLE**

<b>A Novel Verification Technique to Uncover Out-Of-Order DUV Behaviors</b> .....	448
<i>Gabriel Marcilio, Luiz C. V. Santos, Bruno Albertini, Sandro Rigo</i>	
<b>Shortening the Verification Cycle with Synthesizable Abstract Models</b> .....	454
<i>Alon Gluska, Lior Libis</i>	
<b>Non-Cycle-Accurate Sequential Equivalence Checking</b> .....	460
<i>Pankaj Chauhan, Deepak Goyal, Gagan Hasteer, Anmol Mathur, Nikhil Sharma</i>	
<b>Regression Verification</b> .....	466
<i>Benny Godlin, Ofer Strichman</i>	

## **SESSION 29 – THERMAL OPTIMIZATION**

<b>Accurate Temperature Estimation Using Noisy Thermal Sensors</b> .....	472
<i>Yufu Zhang, Ankur Srivastava</i>	
<b>Spectral Techniques for High-Resolution Thermal Characterization with Limited Sensor Data</b> .....	478
<i>Ryan Cochran, Sherief Reda</i>	
<b>Dynamic Thermal Management via Architectural Adaptation</b> .....	484
<i>Ramkumar Jayaseelan, Tulika Mitra</i>	
<b>On-Line Thermal Aware Dynamic Voltage Scaling for Energy Optimization with Frequency/Temperature Dependency Consideration</b> .....	490
<i>Min Bao, Alexandru Andrei, Petru Eles, Zebo Peng</i>	

## **SESSION 30 – NOVEL TECHNIQUES TO MINIMIZE CIRCUIT FAILURE**

<b>SRAM Parametric Failure Analysis</b> .....	496
<i>Jian Wang, Soner Yaldiz, Xin Li, Lawrence T. Pileggi</i>	
<b>Soft Error Optimization of Standard Cell Circuits Based on Gate Sizing and Multi-Objective Genetic Algorithm</b> .....	502
<i>Weiguang Sheng, Liyi Xiao, Zhigang Mao</i>	
<b>Improving Testability and Soft-Error Resilience Through Retiming</b> .....	508
<i>Smita Krishnaswamy, Igor L. Markov, John P. Hayes</i>	
<b>Statistical Reliability Analysis Under Process Variation and Aging Effects</b> .....	514
<i>Yinghai Lu, Li Shang, Hai Zhou, Hengliang Zhu, Fan Yang, Xuan Zeng</i>	

## **SESSION 31 – PANEL**

<b>PANEL: Guess, Solder, Measure, Repeat - How Do I Get My Mixed-Signal Chip Right?</b> .....	520
<i>N/A</i>	

## **SESSION 32 – SPECIAL SESSION: MULTICORE COMPUTING AND EDA**

<b>The Cilk++ Concurrency Platform</b> .....	522
<i>Charles E. Leiserson</i>	
<b>Misleading Performance Claims in Parallel Computations</b> .....	528
<i>David H. Bailey</i>	
<b>Massively Parallel Processing: It's Déjà Vu All Over Again</b> .....	534
<i>Steven P. Levitan, Donald M. Chiarulli</i>	

## **SESSION 33 – LAYOUT-BASED VARIABILITY MODELING AND OPTIMIZATION**

<b>Provably Good and Practically Efficient Algorithms for CMP Dummy Fill</b> .....	539
<i>Chunyang Feng, Hai Zhou, Changhao Yan, Jun Tao, Xuan Zeng</i>	
<b>Predicting Variability in Nanoscale Lithography Processes</b> .....	545
<i>Dragoljub Gagi Drmanac, Frank Liu, Li-C. Wang</i>	
<b>Variability Analysis under Layout Pattern-Dependent Rapid-Thermal Annealing Process</b> .....	551
<i>Yun Ye, Frank Liu, Min Chen, Yu Cao</i>	

## **SESSION 34 – ADVANCES IN CORE VERIFICATION TECHNIQUES**

<b>Event-Driven Gate-Level Simulation with GP-GPUs</b> .....	557
<i>Debapriya Chatterjee, Andrew DeOrio, Valeria Bertacco</i>	
<b>Efficient SAT Solving for Non-Clausal Formulas Using DPLL, Graphs, and Watched Cuts</b> .....	563
<i>Himanshu Jain, Edmund M. Clarke</i>	
<b>Constraints in One-To-Many Concretization for Abstraction Refinement</b> .....	569
<i>Kuntal Nanshi, Fabio Somenzi</i>	

## **SESSION 35 – FUTURE INTERCONNECT TECHNOLOGIES: HOW DO ON-CHIP NETWORKS EVOLVE?**

<b>Spectrum: A Hybrid Nanophotonic-Electric On-Chip Network</b> .....	575
<i>Zheng Li, Dan Fay, Alan Mickelson, Li Shang, Manish Vachharajani, Dejan Filipovic, Wounghang Park, Yihe Sun</i>	
<b>Exploring Serial Vertical Interconnects for 3-D ICs</b> .....	581
<i>Sudeep Pasricha</i>	
<b>No Cache-Coherence: A Single-Cycle Ring Interconnection for Multicore L1-NUCA Sharing on 3-D Chips</b> .....	587
<i>Shu-Hsuan Chou, Chien-Chih Chen, Chi-Neng Wen, Yi-Chao Chan, Tien-Fu Chen, Chao-Ching Wang, Jinn-Shyan Wang</i>	

## **SESSION 36 – ROBUST ANALOG SYSTEM DESIGN**

<b>Thermal-Driven Analog Placement Considering Device Matching</b> .....	593
<i>Po-Hung Lin, Hongbo Zhang, Martin D. F. Wong, Yao-Wen Chang</i>	
<b>Yield-driven Iterative Robust Circuit Optimization Algorithm</b> .....	599
<i>Yan Li, Vladimir Stojanovi?</i>	
<b>Contract-Based System-Level Composition for Analog Circuits</b> .....	605
<i>Xuening Sun, Pierluigi Nuzzo, Chang-Ching Wu, Alberto Sangiovanni-Vincentelli</i>	

## **SESSION 37 – SPECIAL SESSION: WACI: WILD AND CRAZY IDEAS**

<b>Serial Reconfigurable Mismatch-Tolerant Clock Distribution</b> .....	611
<i>Atanu Chattopadhyay, Zeljko Zilic</i>	
<b>Thermal-Aware Data Flow Analysis</b> .....	613
<i>José L. Ayala, David Atienza, Philip Brisk</i>	
<b>Nanoscale Digital Computation Through Percolation</b> .....	615
<i>Mustafa Altun, Marc D. Riedel, Claudia Neuhauser</i>	
<b>A Learning Digital Computer</b> .....	617
<i>Bo Marr, Arindam Basu, Stephen Brink, Paul Hasler</i>	
<b>Programmable Neural Processing on a Smartdust</b> .....	619
<i>Shimeng Huang, Joseph Oresko, Yuwen Sun, Allen C. Cheng</i>	
<b>Human Computing for EDA</b> .....	621
<i>Andrew DeOrio, Valeria Bertacco</i>	
<b>Synthesizing Hardware from Sketches</b> .....	623
<i>Andreas Raabe, Rastislav Bodik</i>	
<b>Endosymbiotic Computing: Enabling Surrogate GUI and Cyber-Physical Connectivity</b> .....	625
<i>Pai H. Chou</i>	

## **SESSION 38 – SPECIAL SESSION: THE TOOL SHOWS THAT MY DESIGN IS WRONG, BUT WHERE IS THE BUG?**

<b>Debugging From High Level Down to Gate Level</b> .....	627
<i>Masahiro Fujita, Yoshihisa Kojima, Amir Masoud Gharehbaghi</i>	
<b>The Day Sherlock Holmes Decided to Do EDA</b> .....	631
<i>Andreas Veneris, Sean Safarpour</i>	
<b>Debugging Strategies for Mere Mortals</b> .....	635
<i>Valeria Bertacco</i>	



<b>MAGENTA: Transaction-Based Statistical Micro-Architectural Root-Cause Analysis</b> .....	639
<i>Gila Kamhi, Alexander Novakovsky, Andreas Tiemeyer, Adriana Wolffberg</i>	
<b>Untwist Your Brain - Efficient Debugging and Diagnosis of Complex Assertions</b> .....	644
<i>Michael Siegel, Adriana Maggiore, Christian Pichler</i>	
<b>Beyond Verification: Leveraging Formal for Debugging</b> .....	648
<i>Rajeev K. Ranjan, Claudionor Coelho, Sebastian Skalberg</i>	

### **SESSION 39 – EMBEDDED SYSTEM DESIGN FOR LOW-POWER**

<b>Power Modeling of Graphical User Interfaces on OLED Displays</b> .....	652
<i>Mian Dong, Yung-Seok Kevin Choi, Lin Zhong</i>	
<b>Energy-Aware Error Control Coding for Flash Memories</b> .....	658
<i>Veera Papirla, Chaitali Chakrabarti</i>	
<b>PDRAM: A Hybrid PRAM and DRAM Main Memory System</b> .....	664
<i>Gaurav Dhiman, Raid Ayoub, Tajana Rosing</i>	
<b>A Voltage-Scalable and Process Variation Resilient Hybrid SRAM Architecture for MPEG-4 Video Processors</b> .....	670
<i>Ik Joon Chang, Debabrata Mohapatra, Kaushik Roy</i>	

### **SESSION 40 – HARDWARE AUTHENTICATION, CHARACTERIZATION AND TRUSTED DESIGN**

<b>A Physical Unclonable Function Defined Using Power Distribution System Equivalent Resistance Variations</b> .....	676
<i>Ryan Helinski, Dhruva Acharyya, Jim Plusquellic</i>	
<b>Hardware Authentication Leveraging Performance Limits in Detailed Simulations and Emulations</b> .....	682
<i>Daniel Y. Deng, Andrew H. Chan, G. Edward Suh</i>	
<b>Hardware Trojan Horse Detection Using Gate-Level Characterization</b> .....	688
<i>Miodrag Potkonjak, Ani Nahapetian, Michael Nelson, Tammara Massey</i>	
<b>Process Variation Characterization of Chip-Level Multiprocessors</b> .....	694
<i>Lide Zhang, Lan S. Bai, Robert P. Dick, Li Shang, Russ Joseph</i>	
<b>Information Hiding for Trusted System Design</b> .....	698
<i>Junjun Gu, Gang Qu, Qiang Zhou</i>	

### **SESSION 41 – TARGETED TEST AND DIAGNOSIS**

<b>On Systematic Illegal State Identification for Pseudo-Functional Testing</b> .....	702
<i>Feng Yuan, Qiang Xu</i>	
<b>Automated Failure Population Creation for Validating Integrated Circuit Diagnosis Methods</b> .....	708
<i>Wing Chiu Tam, Osei Poku, R.D. Blanton</i>	
<b>Fault Models for Embedded-DRAM Macros</b> .....	714
<i>Mango C.-T. Chao, Hao-Yu Yang, Rei-Fu Huang, Shih-Chin Lin, Ching-Yu Chin</i>	
<b>Adaptive Test Elimination for Analog/RF Circuits</b> .....	720
<i>Ender Yilmaz, Sule Ozev</i>	

### **SESSION 42 – CHALLENGES OF MEMORY-AWARE DESIGN FOR EMBEDDED SYSTEMS**

<b>WCET-Aware Register Allocation Based on Graph Coloring</b> .....	726
<i>Heiko Falk</i>	
<b>Optimal Static WCET-Aware Scratchpad Allocation of Program Code</b> .....	732
<i>Heiko Falk, Jan C. Kleinsorge</i>	
<b>A Real-Time Program Trace Compressor Utilizing Double Move-To-Front Method</b> .....	738
<i>Vladimir Uzelać, Aleksandar Milenkovic</i>	
<b>Heterogeneous Code Cache: Using Scratchpad and Main Memory in Dynamic Binary Translators</b> .....	744
<i>José A. Baiocchi, Bruce R. Childers</i>	

## **SESSION 43 – PANEL**

<b>PANEL: From Milliwatts to Megawatts: The System-Level Power Challenge</b> .....	750
<i>N/A</i>	

## **SESSION 44 – PARASITIC EXTRACTION IN THE FACE OF PROCESS VARIABILITY**

<b>A Direct Integral-Equation Solver of Linear Complexity for Large-Scale 3-D Capacitance and Impedance Extraction</b> .....	752
<i>Wenwen Chai, Dan Jiao, Cheng-Kok Koh</i>	
<b>Variational Capacitance Extraction of On-Chip Interconnects Based on Continuous Surface Model</b> .....	758
<i>Wenjian Yu, Chao Hu, Wangyang Zhang</i>	
<b>PiCAP: A Parallel and Incremental Capacitance Extraction Considering Stochastic Process Variation</b> .....	764
<i>Fang Gong, Hao Yu, Lei He</i>	
<b>An Efficient Resistance Sensitivity Extraction Algorithm for Conductors of Arbitrary Shapes</b> .....	770
<i>Tarek El-Moselhy, Ibrahim M. Elfadel, Bill Dewey</i>	

## **SESSION 45 – SCHEDULING, ALLOCATION AND RELIABILITY**

<b>Throughput Optimal Task Allocation under Thermal Constraints for Multicore Processors</b> .....	776
<i>Vinay Hanumaiah, Ravishankar Rao, Sarma Vrudhula, Karam S. Chatha</i>	
<b>An Adaptive Scheduling and Voltage/Frequency Selection Algorithm for Real-Time Energy Harvesting Systems</b> .....	782
<i>Shaobo Liu, Qing Wu, Qinru Qiu</i>	
<b>Software-Assisted Hardware Reliability: Abstracting Circuit-Level Challenges to the Software Stack</b> .....	788
<i>Vijay Janapa Reddi, Meeta S. Gupta, Michael D. Smith, Gu-yeon Wei, David Brooks, Simone Campanoni</i>	
<b>Simultaneous Clock Buffer Sizing and Polarity Assignment for Power/Ground Noise Minimization</b> .....	794
<i>Hochang Jang, Taewhan Kim</i>	

## **SESSION 46 – NETWORK-ON-CHIP ADVANCES FOR POWER, RELIABILITY AND THE MEMORY BOTTLENECK**

<b>An SDRAM-Aware Router for Networks-On-Chip</b> .....	800
<i>Wooyoung Jang, David Z. Pan</i>	
<b>Multiprocessor System-On-Chip Designs with Active Memory Processors for Higher Memory Efficiency</b> .....	806
<i>Junhee Yoo, Sungjoo Yoo, Kiyoung Choi</i>	
<b>Vicis: A Reliable Network for Unreliable Silicon</b> .....	812
<i>David Fick, Andrew DeOrio, Jin Hu, Valeria Bertacco, David Blaauw, Dennis Sylvester</i>	
<b>Technology-Driven Limits on DVFS Controllability of Multiple Voltage-Frequency Island Designs: A System-Level Perspective</b> .....	818
<i>Siddharth Garg, Diana Marculescu, Radu Marculescu, Umit Ogras</i>	
<b>NoC Topology Synthesis for Supporting Shutdown of Voltage Islands in SoCs</b> .....	822
<i>Ciprian Seiculescu, Srinivasan Murali, Luca Benini, Giovanni De Micheli</i>	

## **SESSION 47 – LEVERAGING PARALLELISM IN FPGAS AND MULTICORE SYSTEMS**

<b>Hierarchical Reconfigurable Computing Arrays for Efficient CGRA-Based Embedded Systems</b> .....	826
<i>Yoonjin Kim, Rabi N. Mahapatra</i>	
<b>Multicore Parallel Min-Cost Flow Algorithm for CAD Applications</b> .....	832
<i>Yinghai Lu, Hai Zhou, Li Shang, Xuan Zeng</i>	
<b>FPGA-Targeted High-Level Binding Algorithm for Power and Area Reduction with Glitch-Estimation</b> .....	838
<i>Scott Cromar, Jaeho Lee, Deming Chen</i>	
<b>FPGA-Based Accelerator for the Verification of Leading-Edge Wireless Systems</b> .....	844
<i>Amirhossein Alimohammad, Saeed F. Fard, Bruce F. Cockburn</i>	
<b>Transmuting Coprocessors: Dynamic Loading of FPGA Coprocessors</b> .....	848
<i>Chen Huang, Frank Vahid</i>	

## **SESSION 48 – SPACE AND TIME MANAGEMENT IN EMBEDDED APPLICATIONS**

<b>Dynamic Thread and Data Mapping for NOC Based CMPs</b> .....	852
<i>Mahmut Kandemir, Ozcan Ozturk, Sai P. Muralidhara</i>	
<b>A Commitment-Based Management Strategy for the Performance and Reliability Enhancement of Flash-Memory Storage Systems</b> .....	858
<i>Yuan-Hao Chang, Tei-Wei Kuo</i>	
<b>Quality-Driven Synthesis of Embedded Multi-Mode Control Systems</b> .....	864
<i>Soheil Samii, Petru Eles, Zebo Peng, Anton Cervin</i>	
<b>Context-Sensitive Timing Analysis of Esterel Programs</b> .....	870
<i>Lei Ju, Bach Khoa Huynh, Samarjit Chakraborty, Abhik Roychoudhury</i>	
<b>Scheduling the FlexRay Bus Using Optimization Techniques</b> .....	874
<i>Haibo Zeng, Wei Zheng, Marco Di Natale, Arkadeb Ghosal, Paolo Giusto, Alberto Sangiovanni-Vincentelli</i>	

## **SESSION 49 – PANEL**

<b>PANEL: The Wild West: Conquest of Complex Hardware-Dependent Software Design</b> .....	878
<i>N/A</i>	

## **SESSION 50 – SPECIAL SESSION: TECHNOLOGIES FOR GREEN DATA CENTERS**

<b>Internet-In-A-Box: Emulating Datacenter Network Architectures Using FPGAs</b> .....	880
<i>Jonathan D. Ellithorpe, Zhangxi Tan, Randy H. Katz</i>	
<b>Sustainable Data Centers: Enabled by Supply and Demand Side Management</b> .....	884
<i>Prith Banerjee, Chandrakant D. Patel, Cullen Bash, Parthasarathy Ranganathan</i>	
<b>Green Data Centers and Hot Chips</b> .....	888
<i>Dilip D. Kandlur, Tom W. Keller</i>	

## **SESSION 51 – HOW TO IMPROVE YOUR MEMORY**

<b>Optimum LDPC Decoder: A Memory Architecture Problem</b> .....	891
<i>Erick Amador, Renaud Pacalet, Vincent Rezard</i>	
<b>A DVS-Based Pipelined Reconfigurable Instruction Memory</b> .....	897
<i>Zhiguo Ge, Tulika Mitra, Weng-Fai Wong</i>	
<b>LICT: Left-Uncompressed Instructions Compression Technique to Improve the Decoding Performance of VLIW Processors</b> .....	903
<i>Talal Bonny, Joerg Henkel</i>	
<b>Hierarchical Architecture of Flash-Based Storage Systems for High Performance and Durability</b> .....	907
<i>Sanghyuk Jung, Jin Hyuk Kim, Yong Ho Song</i>	

## **SESSION 52 – SCHEDULING IN TIME AND SPACE**

<b>Reduction Techniques for Synchronous Dataflow Graphs</b> .....	911
<i>Marc Geilen</i>	
<b>A Parameterized Compositional Multi-Dimensional Multiple-Choice Knapsack Heuristic for CMP Runtime Management</b> .....	917
<i>Hamid Shojaei, Amirhossein Ghamarian, Marc Geilen, Sander Stuijk, Rob Hoes, Twan Basten</i>	
<b>Mode Grouping for More Effective Generalized Scheduling of Dynamic Dataflow Applications</b> .....	923
<i>William Plishker, Nimish Sane, Shuvra S. Bhattacharyya</i>	
<b>Efficient Program Scheduling for Heterogeneous Multicore Processors</b> .....	927
<i>Jian Chen, Lizy K. John</i>	

## **SESSION 53 – HEURISTIC APPROACHES TO HARDWARE OPTIMIZATION**

<b>Polynomial Datapath Optimization Using Partitioning and Compensation Heuristics</b> .....	931
<i>Omid Sarbishei, Bijan Alizadeh, Masahiro Fujita</i>	
<b>Register Allocation for High-Level Synthesis Using Dual Supply Voltages</b> .....	937
<i>Insup Shin, Seungwhun Paik, Youngsoo Shin</i>	

<b>GPU-Based Parallelization for Fast Circuit Optimization</b> .....	943
<i>Yifang Liu, Jiang Hu</i>	
<b>Architectural Assessment of Design Techniques to Improve Speed and Robustness in Embedded Microprocessors</b> .....	947
<i>Thomas Baumann, Doris Schmitt-Landsiedel, Christian Pacha</i>	

**SESSION 54 – MODEL ORDER REDUCTION TECHNIQUES AND APPLICATIONS**

<b>ARMS - Automatic Residue-Minimization Based Sampling for Multi-Point Modeling Techniques</b> .....	951
<i>Jorge Fernandez Villena, L. Miguel Silveira</i>	
<b>An Efficient Passivity Test for Descriptor Systems via Canonical Projector Techniques</b> .....	957
<i>Ngai Wong</i>	
<b>A Parameterized Mask Model for Lithography Simulation</b> .....	963
<i>Zhenhai Zhu</i>	
<b>Author Index</b>	