2009 IEEE Bipolar / BiCMOS Circuits and Technology Meeting

(BCTM 2009)

Capri, Italy
12 – 14 October 2009

IEEE Catalog Number: CFP09BIP-PRT
ISBN: 978-1-4244-4894-4

Table of Contents

Tuesday, October 13, 2009

1. Exploring the Limits of SiGe HBTs

(1.1) 10:50–11:15 AM **A Conventional Double-Polysilicon FSA-SEG Si/SiGe:C HBT Reaching 400 GHz f_{MAX}** **p. 1**

P. Chevalier, F. Pourchon, T. Lacave, G. Avenier, Y. Campidelli, L. Depoyan, G. Troillard, M. Buczko, D. Gloria, D. Céli, C. Gaquière, and A. Chantre

This paper summarizes the work carried out to improve performances of a conventional double-polysilicon FSA-SEG SiGe:C HBT towards 400 GHz f_{MAX}. The technological optimization strategy is discussed and electrical characteristics are presented.

(1.2) 11:15–11:40 AM **A 400 GHz f_{MAX} Fully Self-Aligned SiGe:C HBT Architecture** **p. 5**

S. van Huylenbroeck, A. Sibaja-Hernandez, R. Venegas, S. You, G. Winderickx, D. Radisic, W. Lee, P. Ong, T. Vandeweyer, D. Nguyen, K. De Meyer, and S. Decoutere

An improved fully self-aligned SiGe:C HBT architecture featuring a single-step epitaxial collector-base process is described. An f_{MAX} value of 400 GHz is reached by structural as well as intrinsic advancements made to the HBT device.

(1.3) 11:40–12:30 PM **Advanced Process Modules and Architectures for Half-Terahertz SiGe:C HBTs (Invited)** **p. 9**

S. Decoutere, S. van Huylenbroeck, B. Heinemann, A. Fox, P. Chevalier, A. Chantre, T. Meister, K. Aufinger, and M. Schröter

The European project DOTFIVE addresses evolutionary scaling of self-aligned SiGe:C HBTs, investigates novel HBT architectures and develops novel process modules to push SiGe BiCMOS technology towards 500 GHz f_{MAX} and 2.5 ps gate delay.

2. Performance and Operating Constraints of SiGe HBTs

(2.1) 10:50–11:15 AM **Experimental Study of the SOA of SiGe HBTs on SOI (Student)** **p. 17**

P. Cheng, S. Seth, C. Grens, T. Thrivikraman, M. Bellini, J.D. Cressler, J. Babcock, T. Chen, J. Kim, and A. Buchholz

The safe-operating-area of a variety of both bulk and thick-film SOI SiGe

HBTs has been investigated using DC and pulsed-mode output characteristics, as well as RF gain and linearity measurements. RF operation of SiGe HBTs on SOI beyond the traditionally-defined safe-operating-area showed only minor degradation, and actually improved RF linearity.

(2.2) 11:15–11:40 AM **Electrothermal Behavior of Highly-Symmetric Three-Finger Bipolar Transistors (Student)** **p. 21**

L. La Spina, V. d'Alessandro, S. Russo, N. Rinaldi, and L.K. Nanver

Design guidelines are established for improving the electrothermal stability of multi-finger bipolar transistors. A threefold rotational-symmetric topography is proposed to achieve a significant enlargement of the safe operating area as compared to the more conventional parallel-finger designs.

(2.3) 11:40–12:05 AM **Theoretical Analysis and Modeling of Bipolar Transistor Operation Under Base Current Reversal** **p. 25**

M. Costagliola and N. Rinaldi

A two-dimensional theoretical analysis of bipolar transistor operation under reversal base current conditions is presented. This model describes the current crowding effect occurring when the device is biased above the open-base breakdown voltage BV_{CEO}, also known as the "pinch-in" effect.

(2.4) 12:05–12:30 PM **Comparing RF Linearity of npn and pnp SiGe HBTs (Student)** **p. 29**

S. Seth, P. Cheng, C. Grens, J.D. Cressler, J. Babcock, Y. Liu, J. Kim, and A. Buchholz

Linearity characteristics of complementary SiGe HBTs are investigated. At low bias, both devices exhibit similar linearity and gain. The pnp's offers advantages over the npn's in high bias, however, and linearity of both devices improves with frequency. The underlying mechanisms are addressed.

3. Software Defined Radio

(3.1) 10:50–11:40 AM **Future Needs in RF Reconfiguration From a System Point of View (Invited)** **p. 33**

D. Morche and S. Pruvost

This paper presents the new reconfiguration requirements in RF chipset from a system point of view. It will first concentrate on application constraints by considering opportunistic radio and will then study the constraints arising from technology evolution and particularly the variability issue.

(3.2) 11:40–12:05 AM **An Integrated 0.6-4.6 GHz, 5-7 GHz, 10-14 GHz, and 20-28 GHz Frequency Synthesizer for Software-Defined Radio Applications (Student)** **p. 39**

S.A. Osmany, F. Herzel, and J.C. Scheytt

We present an integrated frequency synthesizer which is able to provide in-phase / quadrature phase signals over the frequency bands of 0.6-4.6 GHz, 5-7 GHz, 10-14 GHz, and in-phase signals over 20-28 GHz, for

software-defined radio applications. An integrated voltage controlled oscillator (VCO) with 34% tuning range and a set of high speed dividers are used to accomplish all the frequencies.

(3.3) 12:05–12:30 PM **A Two-Channel, Ultra-Low-Power, SiGe BiCMOS Receiver Front-end for X-Band Phased Array Radars (Student)** **p. 43**

T. Thrivikraman, W.-M.L. Kuo, and J.D. Cressler

We present an ultra-low-power SiGe BiCMOS receiver for X-band phased-array radars. The receiver contains two LNAs and 3-bit phase shifter, consuming 4 mW of dc power with 10 dB of gain and 5 dB NF.

4. RF Building Blocks

(4.1) 2:00–2:25 PM **Large- and Small-Signal Broadband 60 GHz Power Amplifier (Student)** **p. 47**

A. Hamidian and G. Boeck

This paper presents a fully integrated 60 GHz single stage power amplifier (PA) with a cascode topology. The PA achieves the 1 dB bandwidth of more than 9 GHz, from 57 GHz to 66 GHz, and a 3 dB bandwidth of more than 18 GHz (30%), from 51 GHz to 69 GHz, with a power added efficiency (PAE) better than 9% from 57 GHz to 65 GHz.

(4.2) 2:25–2:50 PM **A SiGe:C BiCMOS LNA for 60 GHz Band Applications (Student)** **p. 51**

R. Severino, T. Taris, Y. Deval, D. Belot, and J.-B. Begueret

A new differential LNA dedicated to 60 GHz band has been implemented in a 130 nm BiCMOS technology intended for millimeter-wave applications. The two stage cascode LNA achieves a 21.1 dB maximum gain at 61.5 GHz, a P_{1dB} of -21.2 dBm, a minimum (simulated) noise figure of 4.3 dB, at 10.2 mW power consumption.

(4.3) 2:50–3:15 PM **A Low Power, 1.8-2.6 dB Noise Figure, SiGe HBT Wideband LNA for Multiband Wireless Applications (Student)** **p. 55**

D. Howard, X. Li, and J.D. Cressler

We present a wideband, very low power, SiGe LNA, covering the frequency range of 5-11 GHz, achieving a peak gain of 19.2 dB and 66% fractional bandwidth. The LNA exhibits a Noise Figure (NF) of 1.8-2.6 dB across band and consumes only 9 mW of power.

(4.4) 3:15–3:40 PM **Low-power K-band Pseudo-Stacked Mixer with Linearity Enhancement Technique** **p. 59**

N. Shiramizu, T. Masuda, T. Nakamura, and K. Washio

A low-power transmitter mixer and a receiver mixer operating in the K-band frequency region have been developed. The transmitter mixer achieves a conversion gain of -0.1 dB, and input P_{1dB} of -11 dBm, and the receiver mixer achieves a conversion gain of 11.2 dB and input P_{1dB} of –23 dBm.

(4.5) 3:40–4:05 PM **An 8.7-13.8 GHz Transformer-coupled Varactor-less Quadrature Current-controlled Oscillator RFIC (Student)** **p. 63**

X. Geng and F. Dai

This paper presents an 8.7-13.8 GHz transformer-coupled varactor-less quadrature current-controlled oscillator (QCCO) RFIC. The prototype QCCO achieves a 45.3% tuning range, draws 8-18 mA current under a 1.8 V power supply. The measured phase noise is -86.8 dBc/Hz at 1 MHz offset and -110 dBc/Hz at 10 MHz offset with 11.02 GHz quadrature outputs.

5. Device Physics: Simulation and Structures

(5.1) 2:00–2:50 PM **Electron Transport in Extremely Scaled SiGe HBTs (Invited)** **p. 67**

S.-M. Hong and C. Jungemann

Transport and noise in a THz-SiGe HBT are investigated using classical TCAD tools and full solutions of the more physics-based Boltzmann equation. The transport is quasi-ballistic and the classical models fail to yield accurate results.

(5.2) 2:50–3:15 PM **A Novel Superjunction Collector Design for Improving Breakdown Voltage in High-Speed SiGe HBTs (Student)** **p. 75**

J. Yuan and J.D. Cressler

A novel superjunction collector design is proposed for improving the speed / breakdown voltage trade-off in SiGe HBTs. A SiGe HBT with simulated f_T = 101 GHz, f_{MAX} = 351 GHz, and BV_{CEO} = 3.0 V is achieved.

(5.3) 3:15–3:40 PM **A Novel Device Structure using a Shared-Subcollector, Cascoded Inverse-Mode SiGe HBT for Enhanced Radiation Tolerance (Student)** **p. 79**

T. Thrivikraman, A. Appaswamy, S. Phillips, A. Sutton, E. Wilcox, and J.D. Cressler

We present a novel device structure using an inverse-mode, cascoded (IMC) SiGe HBT for improved heavy-ion irradiation tolerance. The cascoded SiGe device consists of a forward-mode, common-emitter HBT cascoded with a common-base inverse-mode HBT.

6. State-of-the-art Measurements and Parameter Extraction

(6.1) 2:00–2:25 PM **SiGe HBT Noise Parameter Extraction using In-Situ Silicon Integrated Tuner in the mmW Range of 60 – 110 GHz (Student)** **p. 83**

Y. Tagro, D. Gloria, S. Boret, and G. Dambrine

A silicon integrated tuner is presented for use in extracting millimeter-wave noise parameters through a multi-impedance method. This tuner is directly integrated with on-wafer transistor test structures. A gamma of 0.70 has

been achieved and an NF_{min} of 2.6 dB has been extracted on SiGe HBTs at 60GHz.

(6.2) 2:25–2:50 PM **Investigation of High Frequency Coupling Between Probe Tips and Wafer Surface (Student)** **p. 87**

J. Bazzi, C. Raya, A. Curutchet, and T. Zimmer

This paper presents an investigation of the coupling between probes tips and the wafer surface through EM-simulation, and compares the simulation results to measurements. It is pointed out that the results are very dependent on the adjacent structures lying under the probe tips. Different solutions are analyzed to master and/or reduce the coupling and assure reproducibility of measurements.

(6.3) 2:50–3:15 PM **Distributed De-embedding Technique For Accurate On-chip Passive Measurements Based on Open-Short Structures** **p. 91**

H. Veenstra, M. Notten, D. van Goor, and J. Mills

A technique is introduced to derive a distributed model for standard Open-Short de-embedding structures. A significant improvement in accuracy is obtained above 10 GHz if long de-embedding lines are unavoidable, as demonstrated for a 470 pH inductor.

(6.4) 3:15–3:40 PM **Evaluating the Self-Heating Thermal Resistance of Bipolar Transistors by DC Measurements: a Critical Review and Update (Student)** **p. 95**

S. Russo, V. d'Alessandro, L. La Spina, N. Rinaldi, and L.K. Nanver

A comprehensive comparative analysis of the most relevant DC measurement techniques developed to determine the self-heating thermal resistance of bipolar devices is presented. An improved, but still simple extraction approach, is proposed for silicon BJTs with non-negligible Early effect, where use of traditional HBT-devised methods may entail significant inaccuracies.

7. Advanced Modeling and Characterization

(7.1) 4:25–4:50 PM **Compact Model of Zener Tunneling Current in Bipolar Transistors, Featuring a Smooth Transition to Zero Forward Bias Current (Student)** **p. 99**

V. Milovanovic, R. van der Toorn, P. Humphries, D.l Vidal, and A. Vafanejad

We present a physics-based compact model of Zener tunneling current, as it may occur in highly-doped, reverse-biased, base-emitter junctions of bipolar transistors. Our model features an infinitely differentiable transition, at zero bias, to zero tunneling current in the forward-bias regime. A verification of the model on typical modern industrial bipolar technology is presented.

(7.2) 4:50–5:15 PM **SiGe Bipolar ESD Modeling for a Full Chip ESD Simulation** **p. 103**

S. Parthasarathy, G. Coram, J.-J. Hajjar, and J. Salcedo

A new SPICE-compatible compact model is developed to simulate the current

and voltage characteristics of SiGe bipolar devices beyond their breakdown. The enhanced bipolar models are benchmarked versus device-level TLP (transmission line pulsing) measurements and used in full-chip ESD simulation to optimize the circuit design for ESD robustness.

(7.3) 5:15–6:05 PM **Matching is Key to Better Processes (Invited)** **p. 107**

H. Tuinhout

Systematic and random parametric mismatches are major performance limiters as well as causes of re-designs for mixed-signal circuits. Therefore it is extremely important to measure, analyze, understand and document parametric mismatch mechanisms. This paper summarizes the main requirements and techniques for proper mismatch characterization of active and passive IC devices.

8. Signal Processing

(8.1) 4:25–5:15 PM **BiCMOS High-Performance ICs: From DC to mm-Wave (Invited)** **p. 115**

B. Smolders, H. Gul, E. van der Heijden, P. Gamand, and M. Geurts

Progress with Si and SiGe-based BiCMOS technologies over the past few years has been very impressive. This has enabled the implementation of traditional microwave and emerging mm-wave applications in silicon. This paper gives an overview of several high-performance ICs that have been implemented in a state-of-the-art BiCMOS technology (QUBIC4). Examples of high-performance ICs are described, ranging from basic building blocks for mobile applications to highly integrated receiver and transmitter ICs for applications up to the mm-wave range.

(8.2) 5:15–5:40 PM **A Precision Monolithic Waveform Generator With 2,000,000:1 Exponential Sweep Range** **p. 123**

E. Modica and D. Bowers

The circuit described is a monolithic waveform generator with a 2,000,000:1 control range, facilitated by means of simultaneous linear and exponential control ports. The generator outputs square waves and low-distortion triangle and sinusoidal waveforms.

(8.3) 5:40–6:05 PM **Current and Voltage ADC Using a Differential Pair of Single Electron Bipolar Avalanche Transistors** **p. 127**

M. Lany and R. Popovic

Single-electron bipolar avalanche transistors (SEBATs) enable current sensing by electron counting at room temperature. Here, differential SEBAT circuits combining the functions of amplification and analog-to-digital (A/D) conversion are proposed and characterized for two applications: Low-current A/D conversion and differential voltage A/D conversion.

Wednesday, October 14, 2009

9. Emerging Technologies

(9.1) 8:30–9:10 AM **Ultra-Thin Chip Fabrication for Next-Generation Silicon Processes (Invited)** **p. 131**

J. Burghartz

Extremely thin silicon chip layers are expected to enable emerging 3D IC, system-in-foil, power and other technologies. The Chipfilm-technology presented and discussed in this talk utilizes local porous silicon formation, sintering and epitaxial overgrowth to manufacture wafer substrates with buried cavities for an a priori definition of the chip's thickness, which has been demonstrated down to 6 µm. Chipfilm complements the established wafer back-thinning techniques in particular where such extremely small chip thickness and excellent mechanical stability is required.

(9.2) 9:10–9:50 AM **3D Integration Technologies for MEMS/IC Systems (Invited)** **p. 138**

P. Ramm

3D integration is a key solution to the predicted performance problems of future ICs, and offers extreme miniaturization and cost-effective fabrication of so-called More-than-Moore products (e.g., MEMS + IC systems). Through-Silicon-Via (TSV) technologies enable high interconnect performance at relatively high fabrication cost compared to 3D packaging. In general, there is no single 3D integration technology suitable for the fabrication of the large variety of envisioned 3D integrated systems. Moreover, even one single product may need several different technologies for a cost-effective fabrication. Wireless sensor systems (e.g., e-CUBES®) are an excellent example of this need for a suitable mixture, as will be described.

(9.3) 9:50–10:30 AM **Nano-tera.ch: Nano-Technologies for Tera-Scale Problems (Invited)** **p. 142**

G. De Micheli

This talk will address the aim and scope of the nano-tera.ch program, a publicly-funded research program focusing on the applications of nano-technologies to distributed embedded systems. In particular, some projects address nanoelectronic design with silicon nanowires and carbon nanotubes, as well as the integration of sensors and MEMS. The use of these technologies offers unprecedented opportunities in the areas of biosensing for health and environmental management.

(9.4) 10:30–11:10 AM **Gallium Nitride (GaN) High Power Devices for Advanced Commercial and Military Applications (Invited)** **p. 146**

J. Shealy

Next generation commercial and military systems require high power amplifiers (HPAs) with superior performance such as higher efficiency, improved thermal performance, wider bandwidth and higher output power. Using a 0.5 µm, 48 V GaN-on-SiC process, a family power GaN amplifiers (from 8 W to 300 W) have been developed for applications in the frequency range of 30 MHz to 4 GHz. Such devices clearly demonstrate superior

power-bandwidth product of GaN for military applications such as radar, military communications and electronic warfare. For commercial applications, a family of linear amplifiers targeting 3GPP, LTE and WiMax cellular base stations offer high efficiency operation. Finally, amplifier modules for emerging applications, such as RF lighting and CATV distribution, offer differentiated performance using GaN technology.

10. High-Speed Digital

(10.1) 11:30–11:55 AM **A Cable Equalizer with 31 dB of Adjustable Peaking at 52 GHz (Student)** **p. 154**

A. Balteanu and S. Voinigescu

A 70 Gbps equalizer in 0.13 µm SiGe BiCMOS with peak gain of 12.2 dB at 52 GHz and 31 dB of adjustable gain control is presented. Equalization is shown at 70 Gbps for 7.2 dB of channel loss.

(10.2) 11:55–12:20 PM **A SiGe BiCMOS Burst-mode Transimpedance Amplifier Using Fast and Accurate Automatic Offset Compensation Technique for 1G/10G Dual-rate Transceiver** **p. 158**

S. Nishihara, M. Nakamura, T. Ito, T. Kurosaki, Y. Ohtomo, and A. Okada

This paper describes a SiGe BiCMOS burst-mode transimpedance amplifier featuring fast gain switching and accurate automatic offset compensation with feed-forward configuration, to constitute a 1G/10G dual-rate optical receiver for next-generation optical access systems.

(10.3) 12:20–12:45 PM **High-Speed, Low-Power Phase Accumulators for DDS Applications in SiGe Bipolar Technology (Student)** **p. 162**

B. Laemmle, C. Wagner, H. Knapp, L. Maurer, and R. Weigel

Two phase accumulators for use in direct digital synthesis (DDS), with 10 and 8 bit resolution, 7 and 15 GHz maximum clock rate, and power dissipation of 237 W and 303 mW, respectively, are presented. The accumulators are designed to retain phase coherence while a frequency switch is performed and integrated in a DDS to simplify measurement.

11. SiGe BiCMOS Platforms and Devices

(11.1) 11:30–11:55 AM **A 0.13 µm SiGe BiCMOS Technology Featuring f_T/ f_{MAX} of 240 / 330 GHz and Gate Delays Below 3 ps** **p. 166**

H. Rücker, B. Heinemann, W. Winkler, R. Barth, J. Borngräber, J. Drews, G. Fischer, A. Fox, T. Grabolla, U. Haak, D. Knoll, F. Korndörfer, A. Mai, S. Marschmeyer, D. Schmidt, J. Schmidt, K. Schulz, B. Tillack, D. Wolansky, and Y. Yamamoto

A 0.13 µm SiGe BiCMOS technology is presented, featuring high-speed SiGe

HBTs along with high-voltage SiGe HBTs. Ring oscillator gate delays of 2.9 ps, low-noise amplifiers operating at 122 GHz, and LC oscillators above 200 GHz, are demonstrated.

(11.2) 11:55–12:20 PM **Integration of SiGe NPN Devices with Tunable Collector Profiles Using a Single Mask** **p. 170**

P. Hurwitz, E. Preisler, and M. Racanelli

An alternate local collector masking scheme is demonstrated in 0.18 μm SiGe BiCMOS technology to create a set of tunable breakdown devices with a single mask. The method relies on a resist post in the emitter window.

(11.3) 12:20–12:45 PM **SiGe HBT npn Device Optimization for RF Power Amplifier Applications** **p. 174**

A. Joseph, M. McPartlin, L. Hughes, J. Forsyth, P. Candra, R. Previti-Kelly, and M. Doherty

This paper describes the optimization approach of npn SiGe HBTs for RF power amplifier performance. Minimizing the collector resistance and barrier effects in a power device are important for optimization of RF characteristics. We demonstrate that a PA with 66.5% PAE, 14.1 dB of gain, 14.1 P_{1dB}, and 15.4 dBm output power can be achieved in SiGe.

12. mmW BiCMOS Circuits

(12.1) 2:20–2:45 PM **A 140 GHz Double-Sideband Transceiver with Amplitude and Frequency Modulation Operating Over a Few Meters (Student)** **p. 178**

E. Laskin, P. Chevalier, B. Sautreuil, and S. Voinigescu

A 140 GHz double-sideband transceiver with amplitude and frequency modulation is demonstrated in SiGe BiCMOS technology. The first Doppler experiment above 100 GHz is described, and data transmission at 4 Gb/s over air is shown at 140 GHz. An amplifier with 21 dB of gain at 160 GHz in SiGe HBT is also presented.

(12.2) 2:45–3:10 PM **A 122 GHz Receiver in SiGe Technology** **p. 182**

K. Schmalz, W. Winkler, J. Borngräber, W. Debski, B. Heinemann, and C. Scheytt

A 122 GHz sub-harmonic receiver for imaging and sensing applications has been realized, which consists of a single-ended LNA, a push-push VCO with 1/32 divider, a polyphase filter, and a subharmonic mixer. The down-conversion gain of the receiver is 25 dB at 127 GHz, and the corresponding noise figure is 11 dB. The 3-dB bandwidth reaches from 125 GHz to 129 GHz. The input 1-dB compression point is at -40 dBm. The receiver consumes 139 mA at a supply voltage of 3.3 V.

(12.3) 3:10–3:35 PM **A 77 GHz 3.3 V Three-Channel Transceiver** **p. 186**

S. Trotta, B. Dehlink, A. Ghazinour, D. Morgan, and J. John

We present a 77 GHz three channel transceiver for automotive radar application designed in a 200 GHz SiGe BiCMOS technology. The chip

features a Tx channel, a prescaler by 1536, and three Rx channels. The Rx channels show a typical conversion gain of 19 dB while the NFssb lower than 13 dB at 100 kHz. The phase noise is 74 dBc/Hz at 100 kHz offset. The output power is 9 dBm. At a 3.3 V supply, the chip consumes 533 mA.

(12.4) 3:35–4:00 PM **168 GHz Dynamic Frequency Divider in SiGe:C Bipolar Technology** **p. 190**

H. Knapp, T.F. Meister, W. Liebl, K. Aufinger, H. Schaefer, J. Boeck, S. Boguth, and R. Lachner

This paper presents a SiGe bipolar dynamic frequency divider operating up to a maximum frequency of 168 GHz. The circuit is based on a first regenerative divider stage which is followed by a static divider and an output buffer and consumes 320 mW.

(12.5) 4:00–4:25 PM **High-Q Passives for mm-Wave SiGe Applications** **p. 194**

M. Kaynak, C. Wipf, R. Scholz, B. Tillack, W.-G. Lee, Y.S. Kim, J.J. Yoo, and J.W. Kim

Backside deep-silicon etching technique is used for achieving high-Q inductors in a standard 0.25 µm SiGe process. Inductors with different values were designed and evaluated. For low value inductances, a significant increase of the quality factor and self-resonance frequency are observed.

13. Trends in Si And SiC Power Devices

(13.1) 2:20–3:10 PM **An Overview of the Recent Developments in High-Voltage Power Semiconductor MOS-Controlled Bipolar Devices (Invited)** **p. 198**

L. Ngwendson, M.R. Sweet, and E.M. Sankara Narayanan

Electricity is the most common form of energy used in all walks of life, and energy consumption is growing at a rate of 2.6% worldwide. MOS-Bipolar power semiconductor devices are essential control elements used in electricity generation, transmission and delivery. Worldwide, extensive research is underway to develop technologies based on MOS-Bipolar devices (e.g., IGBTs, CSTBTs, IEGTs and CIGBTs) in silicon and wide bandgap semiconductors to achieve ultra-low power losses. This paper will be provide an overview of developments in silicon-based power device technologies and will attempt to provide a wider perspective and identify the challenges for the future.

(13.2) 3:10–3:35 PM **Deep Trench Isolation Integrated in a 0.13 µm BiCD Process Technology for Analog Power ICs** **p. 206**

H. Kitahara, T. Tsukihara, M. Sakai, J. Morioka, K. Deguchi, K. Yonemura, K. Watanabe, T. Kikuchi, S. Onoue, K. Shirai, and K. Kimura

Deep trench isolation (DTI) is successfully integrated in a 0.13 µm BiCD process. The DTI technology contributes to increased density of high voltage devices and reduced parasitic bipolar action.

(13.3) 3:35–4:00 PM **Numerical Simulations of Al Implanted 4H-SiC Diodes and** **p. 210**

Modeling an Explicit Carrier Trap Effect Due to the Non-substitutional Doping Concentration
F. Pezzimenti, F. Della Corte, and R. Nipoti
The experimental characteristics of Al implanted 4H-SiC p-i-n diodes are interpreted through numerical simulations focused on a deep defects profile related to the non-substitutional Al doping and the Al acceptor energy level within the material.

(13.4) 4:00–4:25 PM **Analytical Model for the Forward Current in Al-Implanted 4H-SiC p-i-n Diodes Over a Wide Range of Temperatures** **p. 214**
F. Pezzimenti, L.F. Albanese, S. Bellone, and F. Della Corte
The forward J-V characteristics of 4H-SiC p-i-n diodes are studied in a wide range of currents and temperatures by means of an analytical model which describes in detail the role of the various physical parameters.

Author Index