

# **2009 IEEE International High Level Design Validation and Test Workshop**

**(HLDVT 2009)**

**San Francisco, California, USA  
4 – 6 November 2009**



**IEEE Catalog Number: CFP09HLD-PRT  
ISBN: 978-1-4244-4824-1**

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## Session 4: Panel—SystemC Why: To Design or to Verify?

Moderator: Sandeep Shukla—Virginia Tech, U.S.A.

Panelists: John Sanguinetti—Forte Design Systems; Brian Bailey—Industry Verification Guru; Andres Takach—Mentor Graphics; Chad Spackmana—Cebatech; Ajit Dingankar—Intel; Hireen Patel—University of Waterloo, Canada

**Abstract:** The panelists will debate whether SystemC is going to become a de facto design language or will it remain a verification and performance modeling language. It will result in an inspiring debate on the recent trends from the makers of SystemC based synthesis tools, users of SystemC for design and verification, and academic researchers.

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