

# **2009 IEEE International Behavioral Modeling and Simulation Conference**

**(BMAS 2009)**

**San Jose, California, USA  
17-18 September 2009**



IEEE Catalog Number: CFP09238-PRT  
ISBN: 978-1-4244-5358-0

# Table of Contents

## Organizers

## Technical Program Committee

### Session 1: Applications Other Than Electronics

- |     |  |    |
|-----|--|----|
| 1.1 | Behavioral Modeling of Solute Tracking in Microfluidics<br><i>Yi Zeng, Farouk Azizi and Carlos Mastrangelo</i>   | 1  |
| 1.2 | Virtual Skin: A Behavioral Approach Helps Verification<br><i>Benjamin Nicolle, Arnaud Legendre, Louis Ferrero and Leonhard Zastrow</i>                                 | 7  |
| 1.3 | VHDL-AMS Modeling of Adaptive Electrostatic Harvester of Vibration Energy With Dual-Output DC-DC Converter<br><i>Andrii Dudka, Dimitri Galayko and Philippe Basset</i> | 13 |
| 1.4 | VHDL-AMS Behavioural Modelling of a CMUT Element<br><i>Samuel Frew, Hadi Najar and Edmond Cretu</i>  | 19 |

### Session 2: Analog Behavioral Modeling

- |     |   |    |
|-----|---|----|
| 2.1 | Event Driven Analog Modeling for the Verification of PLL Frequency Synthesizers<br><i>Yifan Wang, Christoph Van-Meersbergen, Hans-Werner Groh and Stefan Heinen</i>                             | 25 |
| 2.2 | Analog Behavior Refinement in System Centric Modeling<br><i>Yaseen Zaidi, Christoph Grimm and Jan Haase</i>   | 31 |
| 2.3 | System Level Modeling of Smart Power Switches Using SystemC-AMS for Digital Protection Concept Verification<br><i>Hans-Peter Kreuter, Vladimir Kosel, Michael Glavanovics and Robert Illing</i> | 37 |
| 2.4 | Simulation-Based Hierarchical Sizing and Biasing of Analog Firm IPs<br><i>Farakh Javid, Ramy Iskander and Marie-Minerve Louerat</i>   | 43 |

## **Session 3: Posters and Vendor Exhibits**

3.1	AMS Static Voltage Level Check <i>Marcelo Silva</i>	49
3.2	An Enhanced Macromodeling Approach For Differential Output Drivers <i>Ting Zhu and Paul D Franzon</i>	54
3.3	Analysis and Extraction of Parametric Variation Effects on Microelectronics-Based Biochips <i>Bao Liu</i>	60
3.4	Mixed Signal System Design Verification Accelerated With Detector-Based Diagnostic Method <i>Dirk Dammers, Christian Domingues, Daniel Schollan, and Lars Michael Vosskamper</i>	66
3.5	Powering Embedded CMOS Logic on MEMS-Based Micro-Robots <i>Jung Cho and Mark Arnold</i>	73

## **Session 4: System and Full Chip Behavioral Modeling**

4.1	Mixed-Signal Test Development Using Open Standard Modeling and Description Language <i>Ping Lu, Daniel Glaser, Guerkan Uygur, Susanne Weichslgartner and Klaus Helmreich</i>	78
4.2	Full System Verification of CAN Network at High Speed Transmission Rate Using VHDL-AMS <i>Thang Nguyen, Martin Duregger and Georg Pelz</i>	84
4.3	Fast and Waveform Independent Characterization of Current Source Models <i>Christoph Knoth, Veit B. Kleeberger, Petra Nordholz and Ulf Schlichtmann</i>	90
4.4	A Modeling Methodology for Verifying Functionality of a Wireless Chip <i>Jesse Chen</i>	96

## Session 5: Methods and Models

5.1	Prediction Of Harmonic Distortion in ADCs Using Dynamic Integral Non-Linearity Model <i>Hamza Fraz, Niclas Bjorsell, Stevenson J. Kenney and Roland Sperlich</i>	102
5.2	Supporting Dimensional Analysis in SystemC-AMS <i>Torsten Maehne and Alain Vachoux</i>	108
5.3	VHDL-AMS Statistical Analysis for Marginal Probabilities <i>Haase Joachim</i>	114
5.4	The PRAISE Approach for Accelerated Transient Analysis Applied to Wire Models <i>Daniel Zaum, Stefan Hoelldampf, Ingmar Neumann, Sebastian Schmidt, Markus Olbrich and Erich Barke</i>	120