2009 Asian Test Symposium

(ATS 2009)

Taichung, Taiwan
23-26 November 2009

IEEE Catalog Number: CFP09067-PRT
ISBN: 978-1-4244-5129-6

2009 Asian Test Symposium

ATS 2009

Table of Contents

Foreword
Organizing Committee
Steering Committee
Program Committee
Reviewers
Tutorials
Keynotes
Best Paper Award of ATS 2008
Call for Papers of ATS 2010

Session 3A: Built-In Self-Test

CA Based Built-In Self-Test Structure for SoC 3
Sukanta Das and Biplab K. Sikdar

A Random Jitter RMS Estimation Technique for BIST Applications 9
Jae Wook Lee, Ji Hwan Chun, and Jacob A. Abraham

A Novel Seed Selection Algorithm for Test Time Reduction in BIST 15
Rupsa Chakraborty and Dipanwita Roy Chowdhury

Logic BIST Architecture for System-Level Test and Diagnosis 21
Jun Qian, Xingang Wang, Qinfu Yang, Fei Zhuang, Junbo Jia, Xiangfeng Li, Yuan Zuo, Jayanth Mekkoth, Jinsong Liu, Hao-Jan Chao, Shianling Wu, Huafeng Yang, Lizhen Yu, FeiFei Zhao, and Laung-Terng Wang

Session 3B: Fault Diagnosis

Fault Diagnosis under Transparent-Scan 29
Irith Pomeranz and Sudhakar M. Reddy

Scan Chain Diagnosis by Adaptive Signal Profiling with Manufacturing ATPG Patterns 35
Yu Huang, Wu-Tung Cheng, Ruifeng Guo, Ting-Pu Tai, Feng-Ming Kuo, and Yuan-Shih Chen

On Improving Diagnostic Test Generation for Scan Chain Failures 41
Xun Tang, Ruifeng Guo, Wu-Tung Cheng, Sudhakar M. Reddy, and Yu Huang
On Scan Chain Diagnosis for Intermittent Faults 47
Dan Adolfsson, Joanna Siew, Erik Jan Marinissen, and Erik Larsson

Session 3C: Analog and Mixed-Signal Testing I

Design-for-Test Circuit for the Reduced Code Based Linearity Test Method in Pipelined ADCs with Digital Error Correction Technique 57
Jin-Fu Lin, Soon-Jyh Chang, and Chih-Hao Huang
Multi-tone Testing of Linear and Nonlinear Analog Circuits Using Polynomial Coefficients 63
Suraj Sindia, Virendra Singh, and Vishwani D. Agrawal
Low Cost Dynamic Test Methodology for High Precision ΣΔ ADCs....69
S. Kook, Hyun Choi, Vishwanath Natarajan, Abhijit Chatterjee, Alfred Gomes, Shalahb Goyal, and Le Jin
Very-Low-Voltage Testing of Amorphous Silicon TFT Circuits 75
Shiue-Tsung Shen, Wei-Hsiao Liu, En-Hua Ma, James Chien-Mo Li, and I-Chun Cheng

Session 4A: Industrial Session

Scan Compression Implementation in Industrial Design - Case Study 83
Dragon Hsu and Ron Press
Calibration as a Functional Test: An ADC Case Study 85
Hsiu-Ming Chang, Kuan-Yu Lin, and Kwang-Ting Cheng
Customized Algorithms for High Performance Memory Test in Advanced Technology Node 87
Shomo Chen, Ning Huang, Ting-Pu Tai, and Actel Niu
A Practical DFT Approach for Complex Low Power Designs 90
Augusli Kifli, Y.W. Chen, Y.W. Tsay, and K.C. Wu
DFT Challenges in Next Generation Multi-media IP 92
Mukund Mittal, Subrangshu Das, and S. Vishwanath
Yield Ramp up by Scan Chain Diagnosis 94
Feng-Ming Kuo and Yuan-Shih Chhen

Session 4B: Low-Power Testing

CAT: A Critical-Area-Targeted Test Set Modification Scheme for Reducing Launch Switching Activity in At-Speed Scan Testing 99
K. Enokimoto, X. Wen, Y. Yamato, K. Miyase, H. Sone, S. Kajihara, M. Aso, and H. Furukawa
New Scheme of Reducing Shift and Capture Power Using the X-Filling Methodology 105
Tsung-Tang Chen, Wei-Lin Li, Po-Han Wu, and Jiann-Chyi Rau

Deterministic Built-In Self-Test Using Multiple Linear Feedback Shift Registers for Low-Power Scan Testing 111
Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, and Chi-Wei Yu

Session 4C: On-Line Testing and Silicon Debug

Low Overhead Time-Multiplexed Online Checking: A Case Study of An H.264 Decoder 119
Ming Gao and Kwang-Ting Cheng

A FPGA-Based Reconfigurable Software Architecture for Highly Dependable Systems 125
Stefano Di Carlo, Paolo Prinetto, and Alberto Scionti

Using Non-trivial Logic Implications for Trace Buffer-Based Silicon Debug 131
Sandesh Prabhakar and Michael Hsiao

A Post-Silicon Debug Support Using High-Level Design Description 137
Yeonbok Lee, Tasuku Nishihara, Takeshi Matsumoto, and Masahiro Fujita

Session 5A: Delay Testing

A Low Overhead On-Chip Path Delay Measurement Circuit 145
Songwei Pei, Huawei Li, and Xiaowei Li

An Adaptive Test for Parametric Faults Based on Statistical Timing Information 151
Michihiro Shintani, Takumi Uezono, Tomoyuki Takahashi, Hiroyuki Ueyama, Takashi Sato, Kazumi Hatayama, Takashi Aikyo, and Kazuya Masu

A Delay Measurement Technique Using Signature Registers 157
Kentaroh Katoh, Toru Tanabe, Haque Md Zahidul, Kazuteru Namba, and Hideo Ito

Functional Built-In Delay Binning and Calibration Mechanism for On-Chip at-Speed Self Test 163
Chen-I Chung, Jyun-Sian Jhou, Ching-Hwa Cheng, and Sih-Yan Li

Session 5B: Test Generation I

A Practical Approach to Threshold Test Generation for Error Tolerant Circuits 171
Hideyuki Ichihara, Kenta Sutoh, Yuki Yoshikawa, and Tomoo Inoue

Speeding up SAT-Based ATPG Using Dynamic Clause Activation 177
Stephan Eggersglüß, Daniel Tille, and Rolf Drechsler

N-distinguishing Tests for Enhanced Defect Diagnosis 183
Gang Chen, Janusz Rajski, Sudhakar Reddy, and Irith Pomeranz

Dynamic Compaction in SAT-Based ATPG 187
Alexander Czutro, Ilia Polian, Piet Engelke, Sudhakar M. Reddy, and Bernd Becker

Session 5C: System Test

SIRUP: Switch Insertion in RedUndant Pipeline Structures for Yield and Yield/Area Improvement 193
Mohammad Mirza-Aghatabar, Melvin A. Breuer, and Sandeep K. Gupta

Transaction Level Modeling and Design Space Exploration for SOC Test Architectures 200
Chin-Yao Chang, Chih-Yuan Hsiao, Kuen-Jong Lee, and Alan P. Su

Efficient Software-Based Self-Test Methods for Embedded Digital Signal Processors 206
Jun-Jie Zhu, Wen-Ching Lin, Jheng-Hao Ye, and Ming-Der Shieh

Session 6A: Panel Session I

Is Low Power Testing Necessary? What does the Test Industry Truly Need? 215
Anis Uzzaman

Session 6B: DFT

A Scalable Scan Architecture for Godson-3 Multicore Microprocessor 219
Zichu Qi, Hui Liu, Xiangku Li, Da Wang, Yinhe Han, Huawei Li, and Weiwu Hu

Kiss the Scan Goodbye: A Non-scan Architecture for High Coverage, Low Test Data Volume and Low Test Application Time 225
Michael S. Hsiao and Mainak Banga

Multiple Scan Trees Synthesis for Test Time/Data and Routing Length Reduction under Output Constraint 231
Katherine Shu-Min Li, Yu-Chen Hung, and Jr-Yang Huang

Leveraging Partially Enhanced Scan for Improved Observability in Delay Fault Testing 237
Deepak K.G., Robinson Reyna, Virendra Singh, and Adit D. Singh

Session 6C: RF and Analog Testing

BIST Driven Power Conscious Post-Manufacture Tuning of Wireless Transceiver Systems Using Hardware-Iterated Gradient Search 243
Vishwanath Natarajan, Shyam Kumar Devarakond, Shreyas Sen, and Abhijit Chatterjee

Self-Calibrating Embedded RF Down-Conversion Mixers 249
Abhilash Goyal, Madhavan Swaminathan, and Abhijit Chatterjee

A BIST Solution for the Functional Characterization of RF Systems Based on Envelope Response Analysis 255
Manuel J. Barragán, Rafaella Fiorelli, Diego Vázquez, Adoración Rueda, and José L. Huertas

Exploiting Zero-Crossing for the Analysis of FM Modulated Analog/RF Signals Using Digital ATE 261
Nicolas Pous, Florence Azaïs, Laurent Latorre, Pascal Nouet, and Jochen Rivoir

Session 7A: SoC Test

IEEE 1500 Compatible Interconnect Test with Maximal Test Concurrency 269
Katherine Shu-Min Li, Yi-Yu Liao, Yuo-Wen Liu, and Jr-Yang Huang
Multiple-Core under Test Architecture for HOY Wireless Testing Platform 275
Sung-Yu Chen, Ying-Yen Chen, Chun-Yu Yang, and Jing-Jia Liou
Partition Based SoC Test Scheduling with Thermal and Power Constraints
under Deep Submicron Technologies 281
Chunhua Yao, Kewal K. Saluja, and Parameswaran Ramanathan
Test Integration for SOC Supporting Very Low-Cost Testers 287
Chun-Chuan Chi, Chih-Yen Lo, Te-Wen Ko, and Cheng-Wen Wu

Session 7B: Test Generation II

Why is Conventional ATPG Not Sufficient for Advanced Low Power
Designs? 295
Krishna Chakravadhanula, Vivek Chickermane, Brion Keller, Patrick Gallagher, and Anis Uzzaman
New Class of Tests for Open Faults with Considering Adjacent Lines 301
Hiroshi Takahashi, Yoshinobu Higami, Yuzo Takamatsu, Koji Yamazaki, Toshiyuki Tsutsumi, Hiroyuki Yotsuyanagi, and Masaki Hashizume
Test Pattern Selection and Customization Targeting Reduced Dynamic
and Leakage Power Consumption 307
Subhadip Kundu, Krishna Kumar S., and Santanu Chattopadhyay
Deterministic Algorithms for ATPG under Leakage Constraints 313
Görschwin Fey

Session 7C: Test Data Compression

Extended Selective Encoding of Scan Slices for Reducing Test Data and Test
Power 319
Jun Liu, Yinhe Han, and Xiaowei Li
A Multi-dimensional Pattern Run-Length Method for Test Data Compression 325
Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, and Chen-Lun Lee
Bit-Operation-Based Seed Augmentation for LFSR Reseeding with High
Defect Coverage 331
Hongxia Fang, Krishnendu Chakrabarty, and Rubin Parekhji

Session 8A: Panel Session II

Testing Embedded Memories in the Nano-Era: Will the Existing Approaches
Survive? 339
Said Hamdioui

Session 8B: Fault Modeling & Diagnosis

A Non-Intrusive and Accurate Inspection Method for Segment Delay Variabilities 343
Ying-Yen Chen and Jing-Jia Liou

Bridging Fault Diagnosis to Identify the Layer of Systematic Defects 349
Po-Juei Chen, James Chien-Mo Li, and Hsing Jasmine Chao

Delay Fault Diagnosis in Sequential Circuits 355
Youssef Benabboud, Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, and Olivia Riewer

A Partially-Exhaustive Gate Transition Fault Model 361
Brion Keller, Dale Meehl, Anis Uzzaman, and Richard Billings

Session 8C: Analog and Mixed-Signal Testing II

An On-Chip Integrator Leakage Characterization Technique and Its Application to Switched Capacitor Circuits Testing 367
Chen-Yuan Yang, Xuan-Lun Huang, and Jiun-Lang Huang

LFSR-Based Performance Characterization of Nonlinear Analog and Mixed-Signal Circuits 373
Joonsung Park, Jaeyong Chung, and Jacob A. Abraham

A Jitter Characterizing BIST with Pulse-Amplifying Technique 379
An-Sheng Chao and Soon-Jyh Chang

A Low-Cost Output Response Analyzer for the Built-in-Self-Test Σ-Δ Modulator Based on the Controlled Sine Wave Fitting Method 385
Shao-Feng Hung, Hao-Chiao Hong, and Sheng-Chuan Liang

Session 9A: Memory Test

New Algorithms for Address Decoder Delay Faults and Bit Line Imbalance Faults 391
Ad J. van de Goor, Said Hamdioui, Georgi N. Gaydadjiev, and Zaid Al-Ars

Testability Exploration of 3-D RAMs and CAMs 397
Yu-Jen Huang and Jin-Fu Li

Fault Diagnosis Using Test Primitives in Random Access Memories 403
Zaid Al-Ars and Said Hamdioui

Session 9B: Test Generation III

Test Generation for Designs with On-Chip Clock Generators 411
Xijiang Lin and Mark Kassab

On the Generation of Functional Test Programs for the Cache Replacement Logic 418
W.J. Perez H., D. Ravotto, E. Sanchez, M. Sonza Reorda, and A. Tonda

Compact Test Generation for Small-Delay Defects Using Testable-Path Information 424
Dong Xiang, Boxue Yin, and Krishendu Chakrabarty
At-Speed Scan Test Method for the Timing Optimization and Calibration 430
Kun-Han Tsai, Ruifeng Guo, and Wu-Tung Cheng

Session 9C: Defect-Based Testing

M-IVC: Using Multiple Input Vectors to Minimize Aging-Induced Delay 437
Song Jin, Yinhe Han, Lei Zhang, Huawei Li, Xiaowei Li, and Guihai Yan
Analysis of Resistive Bridging Defects in a Synchronizer 443
Hyoung-Kook Kim, Wen-Ben Jone, Laung-Terng Wang, and Shianling Wu
On-Chip TSV Testing for 3D IC before Bonding Using Sense Amplification 450
Po-Yuan Chen, Cheng-Wen Wu, and Ding-Ming Kwai
Test Pattern Selection for Potentially Harmful Open Defects in Power Distribution Networks 456
Yubin Zhang, Lin Huang, Feng Yuan, and Qiang Xu

Author Index