

2009 24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems

(DFT 2009)

**Chicago, Illinois, USA
7 – 9 October 2009**



**IEEE Catalog Number: CFP09078-PRT
ISBN: 978-1-4244-5298-9**

2009 24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems

DFT 2009

Table of Contents

Message from the Symposium Chairs
Organizing Committee
Program Committee
In Memoriam: Professor Susumu Horiguchi
TTTC: Test Technology Technical Council

Keynote Talk

The Future of Test—Product Integration and its Impact on Test3
Michael Campbell

Keynote Talk

Low DPM: Why Do We Need it and What Does it Cost!7
Sandeep P. Kumar

Session 1—BIST and On-chip Test Generation

Automated Generation of Built-In Self-Test and Measurement Circuitry
for Mixed-Signal Circuits and Systems11
*George J. Starr, Jie Qin, Bradley F. Dutton, Charles E. Stroud, F. Foster Dai,
and Victor P. Nelson*

Reducing Test Point Area for BIST through Greater Use of Functional
Flip-Flops to Drive Control Points20
Joon-Sung Yang, Benoit Nadeau-Dostie, and Nur A. Touba

Soft Core Embedded Processor Based Built-In Self-Test of FPGAs29
Bradley F. Dutton and Charles E. Stroud

On-chip Generation of the Second Primary Input Vectors of Broadside Tests38
Irith Pomeranz and Sudhakar M. Reddy

Session 2— Design for Fault Tolerance I

Flip-Flop Hardening and Selection for Soft Error and Delay Fault Resilience	49
<i>Mingjing Chen and Alex Orailoglu</i>	
A Novel Hardened Design of a CMOS Memory Cell at 32nm	58
<i>Sheng Lin, Yong-Bin Kim, and Fabrizio Lombardi</i>	
Novel High Speed Robust Latch	65
<i>Martin Omaña, Daniele Rossi, and Cecilia Metra</i>	

Invited Talk

Are Robust Circuits Really Robust?	77
<i>Sybille Hellebrand and Marc Hunger</i>	

Invited Talk

Challenges in Delay Testing of Integrated Circuits	81
<i>D.M.H. Walker</i>	

Session 3—Emerging Technologies

Using RRNS Codes for Cluster Faults Tolerance in Hybrid Memories	85
<i>Nor Zaidi Haron and Said Hamdioui</i>	
Controlling Magnetic Circuits: How Clock Structure Implementation will Impact Logical Correctness and Power	94
<i>Aaron Dingle, M. Jafar Siddiq, Michael Niemier, X. Sharon Hu, M. Tanvir Alam, Gary Bernstein, and Wolfgang Porod</i>	
Coded DNA Self-Assembly for Error Detection/Location	103
<i>Zahra Mashreghian Arani, Masoud Hashempour, and Fabrizio Lombardi</i>	
Errors in DNA Self-Assembly by Synthesized Tile Sets	112
<i>Xiaojun Ma, Masoud Hashempour, Yong-Bin Kim, and Fabrizio Lombardi</i>	

Invited Talk

Dreams, Plans, and Journey of Reaching Perfect Predictability and Reliability in ASICs	123
<i>Naveed Sherwani</i>	

Session 4—Error Detection

Concurrent Detection of Faults Affecting Energy Harvesting Circuits of Self-Powered Wearable Sensors	127
<i>Martin Omaña, Marcin Marzencki, Roberto Specchia, Cecilia Metra, and Bozena Kaminska</i>	
SNR-Aware Error Detection for Low-Power Discrete Wavelet Lifting Transform in JPEG 2000	136
<i>Shih-Hsin Hu, Tung-Yeh Wu, and Jacob A. Abraham</i>	

Reduced Precision Checking for a Floating Point Adder	145
<i>Patrick J. Eibl, Andrew D. Cook, and Daniel J. Sorin</i>	

Session 5—Yield Analysis and Dependability

Characterization of Gain Enhanced In-Field Defects in Digital Imagers	155
<i>Jenny Leung, Glenn H. Chapman, Israel Koren, and Zahava Koren</i>	
Analysis of Resistive Open Defects in a Synchronizer	164
<i>Hyoun-Kook Kim, Wen-Ben Jone, and Laung-Terng Wang</i>	
A Fault Analysis and Classifier Framework for Reliability-Aware SRAM-Based FPGA Systems	173
<i>Cristiana Bolchini, Fabrizio Castro, and Antonio Miele</i>	
On the Functional Qualification of a Platform Model	182
<i>Giuseppe Di Guglielmo, Franco Fummi, Graziano Pravadelli, Mark Hampton, and Florian Letombe</i>	

Session 6—Design for Fault Tolerance II

A Sensor to Detect Normal or Reverse Temperature Dependence in Nanoscale CMOS Circuits	193
<i>David Wolpert and Paul Ampadu</i>	
A Reconfigurable ADC Circuit with Online-Testing Capability and Enhanced Fault Tolerance	202
<i>Yueran Gao and Haibo Wang</i>	
Improving Memory Repair by Selective Row Partitioning	211
<i>Muhammad Tauseef Rab, Asad Amin Bawa, and Nur A. Touba</i>	

Invited Talk

Software-Based Hardware Fault Tolerance for Many-Core Architectures	223
<i>Hans-Joachim Wunderlich</i>	
Can Functional Test Achieve Low-cost Full Coverage of NoC Faults?	224
<i>Marcelo Lubaszewski</i>	

Session 7—Posters

Testing of Switch Blocks in Three-Dimensional FPGA	227
<i>Takumi Hoshi, Kazuteru Namba, and Hideo Ito</i>	
A Study of Side-Channel Effects in Reliability-Enhancing Techniques	236
<i>Jianwei Dai and Lei Wang</i>	
Reliability and Performance Analysis of FPGA-Based Fault Tolerant System	245
<i>Ryoji Noji, Satoshi Fujie, Yuki Yoshikawa, Hideyuki Ichihara, and Tomoo Inoue</i>	
An On-board Data-Handling Computer for Deep-Space Exploration Built Using Commercial-Off-the-Shelf SRAM-Based FPGAs	254
<i>Matteo Sonza Reorda, Massimo Violante, Cristina Meinhardt, and Ricardo Reis</i>	

Minimizing Observation Points for Fault Location	263
<i>Snehal Udar and Dimitri Kagaris</i>	
Optimizing Parametric BIST Using Bio-inspired Computing Algorithms	268
<i>Nastaran Nemati, Amirhossein Simjour, Amirali Ghofrani, and Zainalabedin Navabi</i>	
Analyzing Formal Verification and Testing Efforts of Different Fault Tolerance Mechanisms	277
<i>Meng Zhang, Anita Lungu, and Daniel J. Sorin</i>	
System Level Testing via TLM 2.0 Debug Transport Interface	286
<i>Stefano Di Carlo, Nadereh Hatami, Paolo Prinetto, and Alessandro Savino</i>	
Improving the Effectiveness of XOR-based Decompressors through Horizontal/Vertical Move of Stimulus Fragments	295
<i>Nader Alawadhi and Ozgur Sinanoglu</i>	
Transient Error Detection and Recovery in Processor Pipelines	304
<i>Syed Zafar Shazli and Mehdi Baradaran Tahoori</i>	
Fault-Tolerant Routing Algorithm for Network on Chip without Virtual Channels	313
<i>Yusuke Fukushima, Masaru Fukushi, and Susumu Horiguchi</i>	
Defect-Tolerant Logic Mapping on Nanoscale Crossbar Architectures and Yield Analysis	322
<i>Yehua Su and Wenjing Rao</i>	
Complementary Formal Approaches for Dependability Analysis	331
<i>Souheib Baarir, Cécile Braunstein, Renaud Clavel, Emmanuelle Encrenaz, Jean-Michel Ilié, Régis Leveugle, Isabelle Mounier, Laurence Pierre, and Denis Poitrenaud</i>	
Optimization of Nanoelectronic Systems Reliability Under Massive Defect Density Using Distributed R-fold Modular Redundancy (DRMR)	340
<i>Milos Stanisavljevic, Alexandre Schmid, and Yusuf Leblebici</i>	
An ILP formulation to Unify Power Efficiency and Fault Detection at Register-Transfer Level	349
<i>Yu Liu and Kaijie Wu</i>	
Hazard-Based Detection Conditions for Improved Transition Fault Coverage of Functional Test Sequences	358
<i>Irith Pomeranz and Sudhakar M. Reddy</i>	
Error Control Coding for Multilevel Cell Flash Memories Using Nonbinary Low-Density Parity-Check Codes	367
<i>Yuu Maeda and Haruhiko Kaneko</i>	

Keynote Talk

Resilience Challenges for Exascale Systems	379
<i>Norman Paul Jouppi</i>	

Session 8—Testing and Design for Test

Improving the Detectability of Resistive Open Faults in Scan Cells	383
<i>Fan Yang, Sreejit Chakravarty, Narendra Devta-Prasanna, Sudhakar M. Reddy, and Irith Pomeranz</i>	
An Incremental Approach to Functional Diagnosis	392
<i>Luca Amati, Cristiana Bolchini, Laura Frigerio, Fabio Salice, William Eklow, Arnold Suvatne, Eugenio Brambilla, Federico Franzoso, and Michele Martin</i>	
Generating Diverse Test Sets for Multiple Fault Detections Based on Fault Cone Partitioning	401
<i>Stelios Neophytou, Maria K. Michael, and Kyriakos Christou</i>	
Thermal Driven Test Access Routing in Hyper-interconnected Three-Dimensional System-on-Chip	410
<i>Unni Chandran and Dan Zhao</i>	

Invited Talk

Workload-Cognizant Impact Analysis and its Applications in Error Detection and Tolerance in Modern Microprocessors	421
<i>Yiorgos Makris</i>	
A Defect Tolerant and Performance Tunable Gate Architecture for End-of-Roadmap CMOS	422
<i>Adit D. Singh</i>	

Session 9—Error Detection and Correction

Error Correction Codes for SEU and SEFI Tolerant Memory Systems	425
<i>S. Pontarelli, G.C. Cardarilli, M. Re, and A. Salsano</i>	
Dual-Layer Cooperative Error Control for Reliable Nanoscale Networks-on-Chip	431
<i>Qiaoyan Yu and Paul Ampadu</i>	
Burst Error Detection Hybrid ARQ with Crosstalk-Delay Reduction for Reliable On-chip Interconnects	440
<i>Bo Fu and Paul Ampadu</i>	

Invited Talk

Data Learning Techniques for Functional/System Fmax Prediction	451
<i>Li-C. Wang</i>	

Author Index