

2009 International Conference on Reconfigurable Computing and FPGAs

(ReConFig 2009)

**Cancun, Mexico
9 – 11 December 2009**



IEEE Catalog Number: CFP09389-PRT
ISBN: 978-1-4244-5293-4

2009 International Conference on Reconfigurable Computing and FPGAs

ReConFig 2009

Table of Contents

Message from the Chairs
Organizing Committee
Program Committee
Additional Reviewers

General Sessions

A Novel High-Density Single-Event Upset Hardened Configurable SRAM Applied to FPGA	1
<i>Lei Wang, Lei Chen, Zhiping Wen, Huabo Sun, and Shuo Wang</i>	
FPGA Implementation of a Decimal Floating-Point Accurate Scalar Product Unit with a Parallel Fixed-Point Multiplier	6
<i>Malte Baesler and Thomas Teufel</i>	
Prevention of Hot Spot Development on Coarse-Grained Dynamically Reconfigurable Architectures	12
<i>Sven Eisenhardt, Thomas Schweizer, Andreas Bernauer, Tommy Kuhn, and Wolfgang Rosenstiel</i>	
MRAM Based eFPGAs: Programming and Silicon Flows, Exploration Environments, MRAM Current State in Industry and Its Unique Potentials for FPGAs	18
<i>Yoann Guilleminet, Syed Zahid Ahmed, Lionel Torres, Alexandre Martheley, Julien Eydoux, Jean-Baptiste Cuelle, Laurent Rougé, and Gilles Sassatelli</i>	
Floating Point Hardware for Embedded Processors in FPGAs: Design Space Exploration for Performance and Area	24
<i>Taciano A. Rodolfo, Ney L. V. Calazans, and Fernando G. Moraes</i>	
A 10 Gbps OTN Framer Implementation Targeting FPGA Devices	30
<i>Guilherme Guindani, Frederico Ferlini, Jeferson Oliveira, Ney Calazans, Daniel Pigatto, and Fernando Moraes</i>	
FPGA Implementations of BCD Multipliers	36
<i>G. Sutter, E. Todorovich, G. Bioul, M. Vazquez, and J-P. Deschamps</i>	

Decimal Adders/Subtractors in FPGA: Efficient 6-input LUT Implementations	42
<i>M. Vazquez, G. Sutter, G. Bioul, and J. P. Deschamps</i>	
Matrix Multiplication Based on Scalable Macro-Pipelined FPGA Accelerator Architecture	48
<i>Jiang Jiang, Vincent Mirian, Kam Pui Tang, Paul Chow, and Zuocheng Xing</i>	
PCIREX: A Fast Prototyping Platform for TMR Dynamically Reconfigurable Systems	54
<i>Armando Astarloa, Jesús Lázaro, Unai Bidarte, Aitzol Zuloaga, and Jaime Jiménez</i>	
A FPGA IEEE-754-2008 Decimal64 Floating-Point Multiplier	59
<i>Carlos Minchola and Gustavo Sutter</i>	
Speeding up Fault Injection for Asynchronous Logic by FPGA-Based Emulation	65
<i>Marcus Jeitler and Jakob Lechner</i>	
Runtime Memory Allocation in a Heterogeneous Reconfigurable Platform	71
<i>Vlad-Mihai Sima and Koen Bertels</i>	
A Systolic Array Based Architecture for Implementing Multivariate Polynomial Interpolation Tasks	77
<i>Rafael A. Arce-Nazario, Edusmildo Orozco, and Dorothy Bollman</i>	
A New CLB Architecture for Tolerating SEU in SRAM-Based FPGAs	83
<i>Alireza Rohani and Hamid R. Zarandi</i>	
Hotspot Mitigation Using Dynamic Partial Reconfiguration for Improved Performance	89
<i>Adwait Gupte and Phillip Jones</i>	
Base-Calling in DNA Pyrosequencing with Reconfigurable Bayesian Network	95
<i>Mingjie Lin and Yaling Ma</i>	
High Performance Reconfigurable Computing	
FPGA-Based Online Induction Motor Multiple-Fault Detection with Fused FFT and Wavelet Analysis	101
<i>E. Cabal-Yepez, R. A. Osornio-Rios, R. J. Romero-Troncoso, J. R. Razo-Hernandez, and R. Lopez-Garcia</i>	
A Scalable Architecture for Multivariate Polynomial Evaluation on FPGA	107
<i>Mathieu Allard, Patrick Grogan, and Jean-Pierre David</i>	
An FPGA-Based Custom High Performance Interconnection Network	113
<i>Mondrian Nüssle, Benjamin Geib, Holger Fröning, and Ulrich Brüning</i>	
Communication Performance Characterization for Reconfigurable Accelerator Design on the XD1000	119
<i>Tobias Schumacher, Tim Süß, Christian Plessl, and Marco Platzner</i>	
A Modular Approach to Heterogeneous Biochemical Model Simulation on an FPGA	125
<i>Hideki Yamada, Yasunori Osana, Tomoya Ishimori, Tomonori Ooya, Masato Yoshimi, Yuri Nishikawa, Akira Funahashi, Noriko Hiroi, Hideharu Amano, Yuichiro Shibata, and Kiyoshi Oguri</i>	
Scalability Studies of the BLASTn Scan and Ungapped Extension Functions	131
<i>Siddhartha Datta and Ron Sass</i>	
Low Power RTL Exploration Mechanism Based on the Cache Parameters	137
<i>A. G. Silva-Filho, S. M. L. Lima, and F. C. L. Cox</i>	

A Traversal Cache Framework for FPGA Acceleration of Pointer Data Structures: A Case Study on Barnes-Hut N-body Simulation	143
<i>James Coole, John Wernsing, and Greg Stitt</i>	
Low Power, Reconfigurable Computing Platform for Spacecraft	149
<i>Guillermo Conde, Gregory W. Donohoe, and Siva Maheswaran</i>	
Hardware Accelerator for Full-Text Search (HAFTS) with Succinct Data Structure	155
<i>Naoki Tanida, Mary Inaba, Kei Hiraki, and Takeshi Yoshino</i>	
Triple Line-Based Payout for Go - An Accelerator for Monte Carlo Go	161
<i>Kenichi Koizumi, Mary Inaba, Kei Hiraki, Yasuo Ishii, Takefumi Miyoshi, and Kazuki Yoshizoe</i>	
Acceleration of Fractal Image Compression Using the Hardware-Software Co-design Methodology	167
<i>Oscar Alvarado Nava and Arturo Díaz Pérez</i>	
FPGA Implementation of the Generalized Hough Transform	172
<i>Sergio Rubén Geninatti, José Ignacio Benavides Benítez, Manuel Hernández Calviño, Nicolás Guil Mata, and Juan Gómez Luna</i>	
An Optimized System for Multiple Sequence Alignment	178
<i>Caglar Yılmaz and Mustafa Gök</i>	
Reconfigurable Computing for Security and Cryptography	
Protecting the NOEKEON Cipher against SCARE Attacks in FPGAs by Using Dynamic Implementations	183
<i>Julien Bringer, Hervé Chabanne, and Jean-Luc Danger</i>	
Proof-Carrying Hardware: Towards Runtime Verification of Reconfigurable Modules	189
<i>Stephanie Drzevitzky, Uwe Kastens, and Marco Platzner</i>	
Tailoring a Reconfigurable Platform to SHA-256 and HMAC through Custom Instructions and Peripherals	195
<i>Marcio Juliato and Catherine Gebotys</i>	
Improving the Security of Dual Rail Logic in FPGA Using Controlled Placement and Routing	201
<i>Emna Amouri, Hayder Mrabet, Zied MARRAKCHI, and Habib Mehrez</i>	
Implementing a Protected Zone in a Reconfigurable Processor for Isolated Execution of Cryptographic Algorithms	207
<i>A. Onur Durahim, Erkan Savaş, and Kazim Yumbul</i>	
Combined SCA and DFA Countermeasures Integrable in a FPGA Design Flow	213
<i>Shivam Bhasin, Jean-Luc Danger, Florent Flament, Tarik Graba, Sylvain Guilley, Yves Mathieu, Maxime Nassar, Laurent Sauvage, and Nidhal Selmane</i>	
Efficient Technique for the FPGA Implementation of the AES MixColumns Transformation	219
<i>Solmaz Ghaznavi, Catherine Gebotys, and Reouven Elbaz</i>	
Lightweight Cryptography for FPGAs	225
<i>Panasayya Yalla and Jens-Peter Kaps</i>	

Accelerating Cryptographic Applications Using Dynamically Reconfigurable Functional Units	231
<i>Antoine Trouvé, Lovic Gauthier, Takayuki Kando, Benoît Ryder, Sébastien Pouzols, Pradeep Rao, Norifumi Yoshimatsu, and Kazuaki Murakami</i>	
Observing the Randomness in RO-Based TRNG	237
<i>Nathalie Bochard, Florent Bernard, and Viktor Fischer</i>	
DPL on Stratix II FPGA: What to Expect?	243
<i>Laurent Sauvage, Maxime Nassar, Sylvain Guilley, Florent Flament, Jean-Luc Danger, and Yves Mathieu</i>	
FPGA Implementation of an Elliptic Curve Processor Using the GLV Method	249
<i>Mark Hamilton and William P. Marnane</i>	
Reconfigurable Hardware Implementation of Arithmetic Modulo Minimal Redundancy Cyclotomic Primes for ECC	255
<i>Brian Baldwin, William P. Marnane, and Robert Granger</i>	
Realizing Arbitrary-Precision Modular Multiplication with a Fixed-Precision Multiplier Datapath	261
<i>Johann Großschädl, Erkay Savaş, and Kazim Yumbul</i>	
Multiprocessor Systems and Networks on Chip	
A Framework for 2.5D NoC Exploration Using Homogeneous Networks over Heterogeneous Floorplans	267
<i>Vitor de Paulo and Cristinel Ababei</i>	
Overview of FPGA-Based Multiprocessor Systems	273
<i>Taho Dorta, Jaime Jiménez, José Luis Martín, Unai Bidarte, and Armando Astarloa</i>	
Symmetric Multiprocessor Systems on FPGA	279
<i>Pablo Huerta, Javier Castillo, Cesar Pedraza, Javier Cano, and Jose Ignacio Martinez</i>	
A Fault-Tolerant Layer for Dynamically Reconfigurable Multi-processor System-on-Chip	284
<i>Hung-Manh Pham, Sebastien Pillement, and Didier Demigny</i>	
Modeling and Analyzing of Blocking Time Effects on Power Consumption in Network-on-Chips	290
<i>Arghavan Asad, Amir Ehsani Zonouz, Mehrdad Seyrafi, Mohsen Soryani, and Mahmood Fathy</i>	
Self-Adaptive Network Interface (SANI): Local Component of a NoC Configuration Manager	296
<i>R. Dafali and J-Ph. Diguët</i>	
High-Level FPGA Programming through Mapping Process Networks to FPGA Resources	302
<i>Fritz Mayer-Lindenberg</i>	

Reconfigurable Computing for DSP and Communications

Efficient PGA LFSR Implementation Whitens Pseudorandom Numbers	308
<i>Leonard Colavito and Dennis Silage</i>	
Composite Look-Up Table Gaussian Pseudo-Random Number Generator	314
<i>Leonard Colavito and Dennis Silage</i>	
Design and Implementation of a Configurable Interleaver/Deinterleaver for Turbo Codes in 3GPP Standard	320
<i>Héctor Borrayo-Sandoval, R. Parra-Michel, Luis F. González-Pérez, Fernando Landeros Printzen, and Claudia Feregrino-Uribe</i>	
High Efficiency Space-Based Software Radio Architectures: A Minimum Size, Weight, and Power TeraOps Processor	326
<i>Mark E. Dunham, Zachary Baker, Matthew Stettler, Michael Pigue, Paul Graham, Eric N. Schmierer, and John Power</i>	
A Dynamically Reconfigurable Platform for Fixed-Point FIR Filters	332
<i>Daniel Llamocca, Marios Pattichis, and G. Alonzo Vera</i>	
Design of Coarse-Grained Dynamically Reconfigurable Architecture for DSP Applications	338
<i>Chenxin Zhang, Thomas Lenart, Henrik Svensson, and Viktor Öwall</i>	
A New Approach to Implement Discrete Wavelet Transform Using Collaboration of Reconfigurable Elements	344
<i>Asadollah Shahbahrani, Mahmood Ahmadi, Stephan Wong, and Koen Bertels</i>	
Enhancing the Productivity of Radio Designers with RapidRadio	350
<i>Jorge A. Suris, Adolfo Recio, and Peter Athanas</i>	
Signal Processing Domain Application Mapping on the Brick Reconfigurable Array	356
<i>Juan Fernando Eusse Giraldo and Ricardo Pezzuol Jacobi</i>	

Reconfigurable Techniques

Multiprocessor Task Migration Implementation in a Reconfigurable Platform	362
<i>L. Gantel, S. Layouni, M. E. A. Benkhelifa, F. Verdier, and S. Chauvet</i>	
Virtualization of Computing Resources in RCS for Multi-task Stream Applications	368
<i>L. Kirischian, V. Dumitriu, and P. W. Chun</i>	
Runtime Temporal Partitioning Assembly to Reduce FPGA Reconfiguration Time	374
<i>Abelardo Jara-Berrocal and Ann Gordon-Ross</i>	
Composable and Persistent-State Application Swapping on FPGAs Using Hardwired Network on Chip	380
<i>Muhammad Aqeel Wahlah and Kees Goossens</i>	
New OPBHWICAP Interface for Realtime Partial Reconfiguration of FPGA	386
<i>Julien Delorme, Amor Nafkha, Pierre Leray, and Christophe Moy</i>	
Design and Performance of a Grid of Asynchronously Clocked Run-Time Reconfigurable Modules on a FPGA	392
<i>Jochen Strunk, Toni Volkmer, Wolfgang Rehm, and Heiko Schick</i>	

Reconfigurable Computing for Robotics

Parallax-Docking and Reconfiguration of Field Programmable Robot Arrays Using an Intermittently-Powered One-Hot Controller	398
<i>Mark G. Arnold and Jung H. Cho</i>	
A Reconfigurable Architecture for Stereo-Assisted Detection of Point-Features for Robot Mapping	404
<i>John Kalomiros and John Lygouras</i>	
Fuzzy Control for Cyclist Robot Stability Using FPGAs	410
<i>Yesid E. Castro C., Carlos H. Llanos, Walter de Britto Vidal Filho, and Leandro dos Santos Coelho</i>	
FPGA Implementation for Direct Kinematics of a Spherical Robot Manipulator	416
<i>Diego F. Sánchez, Daniel M. Muñoz, Carlos H. Llanos, and José M. Motta</i>	
On the Implementation of Central Pattern Generators for Periodic Rhythmic Locomotion	422
<i>Cesar Torres-Huitzil</i>	

Bioinspired and Self-Adaptive Computing

Bio-inspired Self-Testing and Self-Organizing Bit Slice Processors	427
<i>André Stauffer and Joël Rossier</i>	
Effects of Simplistic Online Synthesis for AMIDAR Processors	433
<i>Stefan Döbrich and Christian Hochberger</i>	
A Reconfigurable Design Framework for FPGA Adaptive Computing	439
<i>Ming Liu, Zhonghai Lu, Wolfgang Kuehn, Shuo Yang, and Axel Jantsch</i>	
Implementation of a Dynamic Fault-Tolerance Scaling Technique on a Self-Adaptive Hardware Architecture	445
<i>Soto Vargas J., Moreno J. M., Madrenas J., and Cabestany J.</i>	
FPGA Implementation of Izhikevich Spiking Neural Networks for Character Recognition	451
<i>Kenneth L. Rice, Mohammad A. Bhuiyan, Tarek M. Taha, Christopher N. Vutsinas, and Melissa C. Smith</i>	

Author Index