2009 International SoC Design Conference

(ISOCC 2009)

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Contents

ISOCC2009

Oral Session

I S O C C 2 0 0 9

Session 1

Low-voltage Low-power RF CMOS Integrated Circuits and De-embedding Techniques

13:30 – 15:00 Monday, November 23, 2009 Room 201

Special Session

Organizer: Kiat Seng Yeo, Nanyang Technological University, Singapore

Chair: Kiat Seng Yeo, Nanyang Technological University, Singapore

Overview

With the rapid evolution of nanometer radio frequency (RF) CMOS technologies, it is no longer impossible to have exceptionally compact, high-performance and low-cost RF integrated circuits and systems. This special session focuses on a new architecture and some innovative circuit and de-embedding techniques to realize low-voltage low-power RF CMOS transceivers for ultra-wideband (UWB), IEEE 802.16 and IEEE 802.15.3c applications. It consists of six contributing papers. Paper [S1.1] presents a novel 24/36-GHz double conversion heterodyne architecture for IEEE 802.15.3c standard. Paper [S1.2] proposes a technique to simultaneously cancel the thermal noise in UWB low-noise amplifiers while paper [S1.3] describes a direct conversion UWB receiver with a pulse detector. Its low-noise amplifier has a variable gain optimized for low-power consumption. A fully-integrated CMOS power amplifier for 3.5GHz mobile WiMAX (IEEE 802.16 standard) is demonstrated in paper [S1.4]. Paper [S1.5] introduces a low-power all-digital pulse generator and modulator for FCC UWB low frequency band (3.1-4.5GHz) spectral mask specifications. Finally, Paper [S1.6] proposes a new de-embedding technique based on general fixture model to accurate de-embed test fixture parasitic for characterization of RF CMOS at very high frequency.

Session 2 Design Automation Techniques for SoC Design

13:30 – 15:00 Monday, November 23, 2009 Room 202

Special session

Organizer: Kyu-Myung Choi, Samsung Electronics, Korea

Chair: Byeong Min, Samsung Electronics, Korea

Overview

This special session shows Samsung's approaches to produce a competitive SoC design with 45nm process or below. The first paper presents an effective way of fixing lithography hotspots. In the design technologies with 45nm process or below, there is no practical solution to detect the lithography hotspots and remove them in full chip level within a reasonable range of design time and accuracy. This solution can effectively decrease systematic defects with the accuracy of timing closure within a reasonable design time. The second paper shows how to enhance design productivity in RTL design activities. It shows an idea of implementing automatic RTL generator with a user defined specifications. The solution can help RTL designers who are suffering from frequent changes of design specification. The third paper shows a fully automated clock jitter analysis which can handle clock network with a clock divider and state dependency. Thereby, it can handle odd-numbered divider network as well as worst case clock jitter analysis. The last paper shows the body bias and gate-length bias techniques to improve parametric yield. As the variation of process increases, these techniques become important more and more for mass production.

Session 3 H.264 Video Compression Architecture and Design

13:30 – 14:45 Monday, November 23, 2009 Room 203

Special Session

Organizer: Satoshi Goto, Waseda University, Japan and Jongwha Chong, Hanyang University, Korea

Chair: Satoshi Goto, Waseda University, Japan

Co-Chair: Jongwha Chong, Hanyang University, Korea

Overview

H.264 Video coding is now commonly used in the broadcasting or video camera product in the real life. But, there still need new technologies to realize the low complexity, low power or less hardware. This session is focused on these subjects to have better performance of H.264 video coding.

Session 4 Bio & Medical Devices

13:30 – 15:00 Monday, November 23, 2009 Room 204

Chair: Shiho Kim, Chungbuk National University, Korea

Session 5 RF Circuits

16:15 – 17:30 Monday, November 23, 2009 Room 201

Chair: Jinwook Burm, Sogang University, Korea

Session 6 Testing and Verification

16:15 – 17:45 Monday, November 23, 2009 Room 202

Chair: Jae-Kyung Wee, Soongsil University, Korea

Session 7 Design Techniques for Multi-core and Embedded Systems

16:15 – 18:00 Monday, November 23, 2009 Room 203
Special Session

Organizer: Hyunchul Shin, Hanyang University, Korea

Chair: Hyunchul Shin, Hanyang University, Korea

Overview

This special session focuses on the design methodologies and techniques for multi-core and embedded systems, including automatic design methodologies for MPSOC and prototyping on multi-FPGA platforms in [S7.1], real-time power management for a multi-performance processor in [S7.2], effective memory access optimization by memory delay modeling, memory allocation, and buffer allocation in [S7.3].

Session 8

Advanced Design Methodologies and Characterization Strategies for Future Integrated Systems

16:15 – 17:45 Monday, November 23, 2009 Room 204

Special Session

Organizer: Kursun Volkan, Hong Kong University of Science and Technology, Hong Kong

Chair: Kursun Volkan, Hong Kong University of Science and Technology, Hong Kong

Overview

This special session focuses on the advanced design methodologies and characterization techniques for near-future SoC, including skew Analysis and design methodologies to improve performance of resonant Clocking in [S8.1], compressive acquisition CMOS Image Sensor with on-line sorting scheme in [S8.2], practical battery charge/discharge simulator for future embedded systems in [S8.3], custom digital cell generation flow for 65nm processes in [S8.4], strategy to detect bug in pre-silicon phase in [S8.5], and a novel architecture for tunable heterodyne filters in [S8.6].

Session 9 Sensors and/for SoCs

09:30 – 10:45 Tuesday, November 24, 2009 Room 201

Special Session

Organizer: Makoto Ikeda, University of Tokyo, Japan

Chair: Tetsuya Iizuka, University of Tokyo, Japan

Overview

Sensing is becoming one of the most important topics in many areas such like bio-interfaces, monitoring the operation of SoCs. Also to achieve low-power and versatile sensor-net nodes, single chip sensor node SoCs are essential. This special session covers this wide diversity of technical areas to overlook the state-of-the art techniques and future perspectives.

In the first presentation "CMOS image sensor for recording of intrinsic-optical signal of the brain," S. Shishido and his colleagues of Nara Institute of Science and Technology (NAIST) describe an image sensor to capture and record of brain activities such like Intrinsic Optical Signal (IOS) and EEG and so on.

The 2nd presentation "Cascaded Time Difference Amplifier using Differential Logic Delay Cell," S. Mandai and his colleagues of the University of Tokyo describe a time difference amplifier with the gain error below 5.5% over +-250ps input range in 0.18um CMOS for Time-to-digital Converters (TDCs) and sensors for precise time-domain signal capture, such like TOFs.

The 3rd presentation "On-Chip Power Noise Measurements of High-Frequency CMOS Digital Circuits," T. Matsuno and M. Nagata of Kobe University describe an on-chip power and substrate noise measurements ranging from 100MHz to 1.2GHz using in 90nm CMOS.

The 4th presentation "A Single-Chip Sensor Node LSI with Synchronous MAC Protocol and Divided Data-Buffer SRAM," T. Takeuchi and his colleagues of Kobe University describe an ultra-low-power single-chip sensor-node VLSI with a synchronous MAC protocol and divided data-buffer SRAM achieving only 6uW power consumption in 0.18um CMOS.

The last presentation "An SoC Platform with On-Chip Web Interface for In-Field Monitoring," T. Iizuka and his colleagues of the University of Tokyo describe an SoC platform which enables in-field LSI testing and an easy access to the on-chip LSI monitoring circuits through on-chip web interface.

Session 10 Power Gating and Low-Power SoC Design

09:30 – 11:00 Tuesday, November 24, 2009 Room 202

Special Session

Organizer: Kursun Volkan, Hong Kong University of Science and Technology, Hong Kong

Chair: Kursun Volkan, Hong Kong University of Science and Technology, Hong Kong

Overview

This special session focuses on the low power management techniques of SoC through various levels and methodologies which include power-gated circuit techniques in [S10.1], sleep transistor forward body bias method in [S10.2], SoC power off-noise analysis in [S10.3], SRAM Core Modeling in [S10.4], Statistical Approach to Low Power in [S10.5], and Incremental Register Placement techniques in [S10.6].

Session 11 Embedded SW & Embedded Memory

09:30 – 10:45 Tuesday, November 24, 2009 Room 203

Chair: Sungjoo Yoo, POSTECH, Korea

Session 12 Design Techniques of SoC for Telecommunication

09:30 – 11:00 Tuesday, November 24, 2009 Room 204

Special session

Organizer: Jun Ma, Shanghai Jiao Tong University, China

Chair: Jun Ma, Shanghai Jiao Tong University, China

Overview

In the system-on-chip (SoC) design for telecommunication applications, it is vital to conduct joint optimizations among RF, analog, and digital baseband. The imperfections caused by RF and analog blocks can usually be relaxed and/or compensated by the digital circuits in the baseband. In this special session, two papers namely [S12.2] and [S12.3] are presented to address these issues such as I/Q imbalance and phase noise compensations in an OFDM based wireless communication environment. The VLSI architectures are also investigated for the phase noise compensation based on decision feedback algorithm using MMSE equalization technique. Two other papers, namely [S12.1] and [S12.4] in this special session are presented to address the symbol timing synchronization issue and digital automatic gain control (DAGC) function block for the ultra-wideband (UWB) wireless communications and digital mobile TV applications, respectively. Due to the very high sampling rate requirement in the UWB system, a symbol-rate timing recovery approach based on digital adaptive interpolation using LMS algorithm is proposed for the purpose of power consumption reduction in paper [S12.1]. In paper [S12.4], detailed finite-word-length (FWL) analysis are conducted on the VLSI architecture of the DAGC function block for

the purpose of efficient FWL design, which is an essential step from the system to the digital logic design. The proposed FWL analysis approaches are also applicable to other digital feedback systems.

Session 13 CAD

11:15 – 12:15 Tuesday, November 24, 2009 Room 202

Chair: Yungseon Eo, Hanyang University, Korea

Session 14 Analog & Mixed Signal 1

11:15 – 12:15 Tuesday, November 24, 2009 Room 203

Chair: Jae-Yoon Sim, POSTECH, Korea

Session 15 Data Converters

13:45 – 15:00 Tuesday, November 24, 2009 Room 201

Chair: Kwang-Hyun Baek, Chung-Ang University, Korea

Session 16 Design Methodology

13:45 – 15:00 Tuesday, November 24, 2009 Room 202

Chair: Sang-Bock Cho, Ulsan University, Korea

Session 17 SoC for Multimedia

13:45 – 15:00 Tuesday, November 24, 2009 Room 203

Chair: Jinsang Kim, Kyung Hee University, Korea

Session 18 Platforms and Design Tools for Automotive Systems

13:45 – 14:45 Tuesday, November 24, 2009 Room 204

Special session

Organizer: Hiroyuki Tomiyama, Nagoya University, Japan

Chair: Hiroyuki Tomiyama, Nagoya University, Japan

Overview

From a viewpoint of computer engineering, a modern luxury automotive vehicle is a parallel and distributed computing machine with more than one hundred ECUs (Electronic Control Units) and millions of lines of software. Automotive systems are an emerging application domain for SOC industry. This special session focuses on platforms and design tools for embedded systems for automotive applications. The first paper describes a software platform which is a key technology to efficiently develop ever growing automotive software. The second paper presents a toolkit for efficient hardware/software co-simulation of CAN-based automotive network systems. The third paper proposes a two-level hierarchical scheduling framework with a split interrupt routine, which enables multiple automotive applications to be integrated on a single ECU with keeping real-time constraints. The last paper presents a new challenge to apply dynamic reconfiguration technology to the next-generation ECU design.

Session 19 Analog & Mixed Signal 2 (High Speed Signal Interface)

15:15 – 17:00 Tuesday, November 24, 2009 Room 201

Chair: Young-Chan Jang, Kumoh National Institute of Technology, Korea

Session 20 DC/DC Converters, Signal Integrity

15:15 – 16:45 Tuesday, November 24, 2009 Room 202

Chair: Jae-Yoon Sim, POSTECH, Korea

Co-Chair: Taewhan Kim, Seoul National University, Korea

Session 21 Communication SoCs

15:15 – 17:00 Tuesday, November 24, 2009 Room 203

Chair: Hanho Lee, Inha University, Korea

Session 22 Low Power Design Techniques

15:15 – 16:45 Tuesday, November 24, 2009 Room 204

Chair: Sang-Hoon Hong, Kyung Hee University, Korea

Poster Session

I S O C C 2 0 0 9

09:30 – 11:00 Tuesday, November 24, 2009 2nd Floor Lobby

Chair: Jinsang Kim, Kyung Hee University, Korea