

# **2010 IEEE International Solid-State Circuits Conference**

## **(ISSCE 2010)**

**San Francisco, California, USA  
7 - 11 February 2010**



**IEEE Catalog Number: CFP10ISS-PRT**  
**ISBN: 978-1-4244-6033-5**

# TABLE OF CONTENTS

## SESSION 1: PLENARY SESSIONS

<b>Overview</b> .....	1
<b>MEMS for Automotive and Consumer Electronics</b> .....	4
<i>J. Marek</i>	
<b>Harnessing Technology to Advance the Next-generation Mobile User-experience</b> .....	13
<i>G. Delagi</i>	
<b>Challenges of Image-sensor Development</b> .....	20
<i>T. Suzuki</i>	
<b>2009 Lewis Winner Award for Outstanding Paper</b> .....	24
<b>Nanoelectronics in Retrospect, Prospect and Principle</b> .....	26
<i>J. Meindl, A. Naeemi, M. Bakir, R. Murali</i>	

## SESSION 2: MM-WAVE BEAMFORMING & RF BUILDING BLOCKS

<b>Overview</b> .....	31
<b>A True Time-delay-based Bandpass Multi-beam Array at mm-Waves Supporting Instantaneously Wide Bandwidths</b> .....	33
<i>T. S. Chu, H. Hashemi</i>	
<b>A Wideband Beamformer for a Phased-array 60GHz Receiver in 40nm Digital CMOS</b> .....	36
<i>K. Racezkowski, W. Raedt, B. Nauwelaers, P. Wambacq</i>	
<b>A 60GHz-band 2x2 Phased-array Transmitter in 65nm CMOS</b> .....	39
<i>W. L. Chan, J. R. Long, M. Spirito, J. J. Pekarik</i>	
<b>A 5.2-to-13GHz Class-AB CMOS Power Amplifier with a 25.2dBm Peak Output Power at 21.6% PAE</b> .....	42
<i>H. Wang, C. Sideris, A. Hajimiri</i>	
<b>A Passive-mixer-first Receiver with Baseband-controlled RF Impedance Matching, &lt; 6dB NF, and &gt; 27dBm Wideband IIP3</b> .....	45
<i>C. Andrews, A. C. Molnar</i>	
<b>3.3GHz DCO with a Frequency Resolution of 150Hz for all-digital PLL</b> .....	48
<i>L. Fanori, A. Liscidini, R. Castello</i>	
<b>Suppression of Flicker Noise Upconversion in a 65nm CMOS VCO in the 3.0-to-3.6GHz Band</b> .....	51
<i>S. Levantino, M. Zanuso, C. Samori, A. Lacaita</i>	
<b>A 9.2µA Gen 2 Compatible UHF RFID Sensing Tag with -12dBm Sensitivity and 1.25µV<sub>rms</sub> Input-referred Noise Floor</b> .....	54
<i>D. Yeager, F. Zhang, A. Zarrasvand, B. P. Otis</i>	

## SESSION 3: CELLULAR TECHNIQUES

<b>Overview</b> .....	57
<b>A Quad-band Class-39 RF CMOS Receiver for Evolved EDGE</b> .....	59
<i>T. Dellsperger, D. Tschopp, J. Rogin, Y. Chen, T. Burger, Q. Huang</i>	
<b>A 0.8mm<sup>2</sup> All-digital SAW-less Polar Transmitter in 65nm EDGE SoC</b> .....	62
<i>J. Mehta, R. B. Staszewski, O. Eliezer, S. Rezeq, K. Waheed, M. Entezari, G. Feygin, S. Vemulapalli, V. Zoicas, C. M. Hung, N. Barton, I. Bashir, K. Maggio, M. Frechette, M. C. Lee, J. Wallberg, P. Cruise, N. Yanduru</i>	
<b>A Tri-band SAW-less WCDMA/HSPA RF CMOS Transceiver with On-chip DC-DC Converter Connectable to Battery</b> .....	65
<i>Q. Huang, J. Rogin, X. Chen, D. Tschopp, T. Burger, T. Christen, D. Papadopoulos, L. Kouchev, C. Martelli, T. Dellsperger</i>	
<b>A 45nm WCDMA Transmitter Using Direct Quadrature Voltage Modulator with High Oversampling Digital Front-end</b> .....	68
<i>X. He, J. Van-Sinderen, R. Rutten</i>	
<b>A 900MHz Direct <math>\Delta\Sigma</math> Receiver in 65nm CMOS</b> .....	71
<i>K. Koli, J. Jussila, P. Sivonen, S. Kallioinen, A. Parssinen</i>	

<b>A 10MHz Signal Bandwidth Cartesian-loop Transmitter Capable of off-chip PA Linearization</b> .....	74
<i>H. Ishihara, M. Hosoya, S. Otaka, O. Watanabe</i>	
<b>a 23Mw fully Integrated GPS Receiver with Robust Interferer Rejection in 65NM CMOS</b> .....	77
<i>H. Moon, S. Lee, S. C. Heo, H. Yu, J. Yu, J. S. Chang, S. Choi, B. H. Park</i>	
<b>A Low-Power Low-Noise Direct-Conversion Front-end with Digitally Assisted IIP2 Background Self Calibration</b> .....	80
<i>Y. Feng, G. Takemura, S. Kawaguchi, N. Itoh, P. Kinget</i>	

## **SESSION 4: ANALOG TECHNIQUES**

<b>Overview</b> .....	83
<b>A Thermal-diffusivity-based Frequency Reference in Standard CMOS with an Absolute Inaccuracy of <math>\pm 0.1\%</math> from <math>-55^{\circ}\text{C}</math> to <math>125^{\circ}\text{C}</math></b> .....	85
<i>M. Kashmiri, M. Pertijs, K. Makinwa</i>	
<b>A Micropower Chopped-correlated Double-sampling Amplifier with <math>2\mu\text{V}</math> Standard Offset and <math>37\text{nV}/\sqrt{\text{Hz}}</math> Input Noise Density</b> .....	88
<i>M. Belloni, E. Bonizzoni, A. Fornasari, F. Maloberti</i>	
<b>A Single-trim CMOS Bandgap Reference with a <math>3\sigma</math> Inaccuracy of <math>\pm 0.15\%</math> from <math>-40^{\circ}\text{C}</math> to <math>125^{\circ}\text{C}</math></b> .....	91
<i>G. Ge, C. Zhang, G. Hoogzaad, K. Makinwa</i>	
<b>A <math>21\text{nV}/\text{Hz}</math> Chopper-Stabilized Multipath Current-Feedback Instrumentation Amplifier with <math>2\mu\text{V}</math> Offset</b> .....	94
<i>Q. Fan, J. H. Huijsing, K. Makinwa</i>	
<b>A <math>10\text{mW}</math> Stereo Audio CODEC in <math>0.13\mu\text{m}</math> CMOS</b> .....	97
<i>X. Jiang, J. Song, T. L. Brooks, J. Chen, V. Chandrasekar, F. Cheung, S. Galal, D. Cheung, G. C. Ahn, M. Bonu</i>	
<b>Class-G Headphone Driver in <math>65\text{nm}</math> CMOS Technology</b> .....	100
<i>A. Lollo, G. Bollati, R. Castello</i>	
<b><math>45\text{nm}</math> CMOS <math>8\Omega</math> Class-D Audio Driver with <math>79\%</math> Efficiency and <math>100\text{dB}</math> SNR</b> .....	103
<i>S. Samala, V. Mishra, K. C. Chakravarthi</i>	
<b>A <math>105\text{dB}</math>-gain <math>500\text{MHz}</math>-bandwidth <math>0.1\Omega</math> -output-impedance Amplifier for an Amplitude Modulator in <math>65\text{nm}</math> CMOS</b> .....	106
<i>C. Kim, C. S. Chae, Y. S. Yuk, Y. G. Kim, J. K. Kwon, G. H. Cho</i>	
<b>A <math>3.2\text{GHz}</math>-sample-rate <math>800\text{MHz}</math> Bandwidth Highly Reconfigurable Analog FIR Filter in <math>45\text{nm}</math> CMOS</b> .....	109
<i>E. O'Hannaidh, E. Rouat, S. Verhaeren, S. Tual, C. Garnier</i>	
<b>A <math>34\text{dB}</math> SNDR Instantaneously-companding Baseband SC Filter for <math>802.11\text{a/g}</math> WLAN Receivers</b> .....	112
<i>V. Maheshwari, W. A. Serdijn, J. R. Long, J. J. Pekarik</i>	

## **SESSION 5: PROCESSORS**

<b>Overview</b> .....	115
<b>Westmere: A Family of <math>32\text{nm}</math> IA Processors</b> .....	117
<i>N. A. Kurd, S. Bhamidipati, C. Mozak, J. L. Miller, T. M. Wilson, M. Nemani, M. Chowdhury</i>	
<b>A <math>40\text{nm}</math> 16-core 128-thread CMT SPARC SoC Processor</b> .....	120
<i>J. L. Shin, K. Tam, D. Huang, B. Petrick, H. Pham, C. Hwang, H. Li, A. Smith, T. Johnson, F. Schumacher, D. Greenhill, A. S. Leon, A. Strong</i>	
<b>A <math>45\text{nm}</math> <math>37.3\text{GOPS/W}</math> Heterogeneous Multi-Core SoC</b> .....	122
<i>Y. Yuyama, M. Ito, Y. Kiyoshige, Y. Nitta, S. Matsui, O. Nishii, A. Hasegawa, M. Ishikawa, T. Yamada, J. Miyakoshi, K. Terada, T. Nojiri, M. Satoh, H. Mizuno, K. Uchiyama, Y. Wada, K. Kimura, H. Kasahara, H. Maejima</i>	
<b>The Implementation of POWER7™: A Highly Parallel and Scalable Multi-core High-end Server Processor</b> .....	125
<i>D. Wendel, R. Kalla, R. Cargoni, J. Clables, J. Friedrich, R. Frech, J. Kahle, B. Sinharoy, W. Starke, S. Taylor, S. Weitzel, S. G. Chu, S. Islam, V. Zyuban</i>	
<b>A Wire-Speed Power™ Processor: <math>2.3\text{GHz}</math> <math>45\text{nm}</math> SOI with 16 Cores and 64 Threads</b> .....	128
<i>C. Johnson, D. H. Allen, J. Brown, S. Vanderwiel, R. Hoover, H. Achilles, C. Y. Cher, G. A. May, H. Franke, J. Xenedis, C. Basso</i>	
<b>An <math>x86-64</math> Core Implemented in <math>32\text{nm}</math> SOI CMOS</b> .....	131
<i>R. Jotwani, S. Sundaram, S. Kosonocky, A. Schaefer, V. Andrade, G. Constant, A. Novak, S. Naffziger</i>	
<b>A <math>48\text{-core}</math> IA-32 Message-passing Processor with DVFS in <math>45\text{nm}</math> CMOS</b> .....	133
<i>J. Howard, S. Dighe, Y. Hoskote, S. Vangal, D. Finan, G. Ruhl, D. Jenkins, H. Wilson, N. Borkar, G. Schrom, F. Paillet, S. Jain, T. Jacob, S. Yada, S. Marella, P. Salihundam</i>	

<b>A 4.1Tb/s Bisection-Bandwidth 560Gb/s/W Streaming Circuit-Switched 8x8 Mesh Network-on-Chip in 4nm CMOS</b> .....	136
<i>M. A. Anders, H. Kaul, S. K. Hsu, A. Agarwal, S. K. Mathew, F. Sheikh, R. K. Krishnamurthy, S. Borkar</i>	

## **SESSION 6: DISPLAY & BIOMEDICAL DEVICES**

<b>Overview</b> .....	139
<b>A Mobile-display-driver IC Embedding a Capacitive- touch-screen Controller System</b> .....	141
<i>H. R. Kim, Y. K. Choi, S. H. Byun, S. W. Kim, K. H. Choi, H. Y. Ahn, J. K. Park, D. Y. Lee, Z. Y. Wu, H. D. Kwon, Y. Y. Choi, C. J. Lee, H. H. Cho, J. S. Yu, M. Lee</i>	
<b>A Double-loop Control LED Backlight Driver IC for Medium-sized LCDs</b> .....	144
<i>S. Hong, J. W. Han, D. H. Kim, O. K. Kwon</i>	
<b>Stable RGBW AMOLED Display with OLED Degradation Compensation Using Electrical Feedback</b> .....	147
<i>G. R. Chaji, S. Alexander, J. M. Dionne, Y. Azizi, C. Church, J. Hamer, J. Spindler, A. Nathan</i>	
<b>An Inductively Powered Scalable 32-channel Wireless Neural Recording System-on-a-chip for Neuroscience Applications</b> .....	150
<i>S. B. Lee, H. M. Lee, M. Kiani, U. M. Jow, M. Ghovanloo</i>	
<b>A 20<math>\mu</math>W Neural Recording Tag with Supply-current-modulated AFE in 0.13<math>\mu</math>m CMOS</b> .....	153
<i>Z. Xiao, C. M. Tang, C. M. Dougherty, R. Bashirullah</i>	
<b>A 30<math>\mu</math>W Analog Signal Processor ASIC for Biomedical Signal Monitoring</b> .....	156
<i>R. F. Yazicioglu, S. Kim, T. Torfs, P. Merken, C. Van-Hoof</i>	
<b>A 1V 22<math>\mu</math>W 32-channel Implantable EEG Recording IC</b> .....	159
<i>X. Zou, W. S. Liew, L. Yao, Y. Lian</i>	
<b>A Timing Controlled AC-DC Converter for Biomedical implants</b> .....	162
<i>K. F. E. Lee</i>	
<b>A CMOS Electrochemical Impedance Spectroscopy Biosensor Array for Label-Free Biomolecular Detection</b> .....	165
<i>A. Manickam, A. Chevalier, M. McDermott, A. D. Ellington, A. Hassibi</i>	

## **SESSION 7: DESIGNING IN EMERGING TECHNOLOGIES**

<b>Overview</b> .....	168
<b>A 3V 6b Successive-Approximation ADC Using Complementary Organic Thin-Film Transistors on Glass</b> .....	170
<i>W. Xiong, U. Zschieschang, H. Klauk, B. Murmann</i>	
<b>An Analog Organic First-Order CT <math>\Delta\Sigma</math> ADC on a Flexible Plastic Substrate with 26.5dB Precision</b> .....	172
<i>H. Marien, M. Steyaert, N. Van-Aerle, P. Heremans</i>	
<b>User Customizable Logic Paper (UCLP) with Organic Sea-of-Transmission-Gates (SOTG) Architecture and Ink-jet Printed Interconnects</b> .....	175
<i>K. Ishida, N. Masunaga, R. Takahashi, T. Sekitani, S. Shino, U. Zschieschang, H. Klauk, M. Takamiya, T. Someya, T. Sakurai</i>	
<b>Robust Digital Design in Organic Electronics by Dual-Gate Technology</b> .....	178
<i>K. Myny, M. J. Beenhakkers, N. A. J. M. Van-Aerle, G. H. Gelinck, J. Genoe, W. Dehaene, P. Heremans</i>	
<b>An Integrated Organic Circuit Array for Flexible Large-Area Temperature Sensing</b> .....	181
<i>D. He, I. A. Nausieda, K. K. Ryu, A. I. Akinwande, V. Bulovic, C. G. Sodini</i>	
<b>Capacitively Coupled Non-Contact Probing Circuits for Membrane-based Wafer-level Simultaneous Testing</b> .....	184
<i>M. Daito, Y. Nakata, S. Sasaki, H. Gomyo, H. Kusamitsu, Y. Komoto, K. Lizuka, K. Ikeuchi, G. S. Kim, M. Takamiya, T. Sakurai</i>	
<b>A Wafer-level Heterogeneous Technology Integration for Flexible Pseudo-SoC</b> .....	187
<i>H. Yamada, Y. Onozuka, A. Lida, K. Itaya, H. Funaki</i>	
<b>Design Issues and Considerations for Low-cost 3D TSV IC Technology</b> .....	190
<i>G. Van-Der-Plas, P. Limaye, A. Mercha, H. Oprins, C. Torregiani, S. Thijs, D. Linten, M. Stucchi, K. Guruprasad, D. Velenis, D. Shinichi, V. Cherman, B. Vandeveldde, V. Simons, I. Wolf, R. Labie, D. Perry, S. Bronckers, N. Minas, M. Cupac, W. Ruythooren, J. Van-Olmen</i>	
<b>Demonstration of Integrated Micro-electro-Mechanical Switch Circuits for VLSI Applications</b> .....	193
<i>F. Chen, M. Spencer, R. Nathanael, C. Wang, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T. J. K. Liu, D. Markovic, V. Stojanovic, E. Alon</i>	

<b>Fully Depleted Extremely Thin SOI for Mainstream 20nm Low-Power Technology and Beyond</b> .....	196
<i>A. Khakifirooz, K. Cheng, B. Jagannathan, P. Kulkarni, J. W. Sleight, D. Shahrjerdi, J. B. Chang, S. Lee, J. Li, H. Bu, R. Gauthier, B. Doris, G. Shahidi</i>	

## **SESSION 8: HIGH-SPEED WIRELINE TRANSCEIVERS**

<b>Overview</b> .....	198
<b>A 47x10Gb/s 1.4mW/(Gb/s) Parallel Interface in 45nm CMOS</b> .....	200
<i>R. O'Mahony, J. Kennedy, J. E. Jaussi, G. Balamurugan, M. Mansuri, C. Roberts, S. Shekhar, R. Mooney, B. Casper</i>	
<b>A 6.8mW 7.4Gb/s Clock-Forwarded Receiver with up to 300MHz Jitter Tracking in 65nm CMOS</b> .....	203
<i>M. Hossain, A. C. Carusone</i>	
<b>A 4.5mW/Gb/s 6.4Gb/s 22+1-Lane Source-synchronous Link RX Core with Optional Cleanup PLL in 65nm CMOS</b> .....	206
<i>R. Reutemann, M. Ruegg, F. Keyser, J. Bergkvist, D. Dreps, T. Toifl, M. Schmatz</i>	
<b>A 16Gb/s 1<sup>st</sup> - Tap FFE and 3-Tap DFE in 90nm CMOS</b> .....	209
<i>H. Sugita, K. Sunaga, K. Yamaguchi, M. Mizuno</i>	
<b>A 12Gb/s 39dB Loss-recovery Unclocked-DFE Receiver with Bi-dimensional Equalization</b> .....	212
<i>M. Pozzoni, S. Erba, D. Sanzogni, M. Ganzerli, P. Viola, D. Baldi, M. Reposs, G. Spelgatti, F. Svelto</i>	
<b>A Fractional-sampling-rate ADC-based CDR with Feedforward Architecture in 65nm CMOS</b> .....	215
<i>O. Tyshchenko, A. Sheikholeslami, H. Tamura, Y. Tomita, H. Yamaguchi, M. Kibune, T. Yamamoto</i>	
<b>A 5Gb/s Transeiver with an ADC-based Feedforward CDR and CMA Adaptive Equalizer in 65nm CMOS</b> .....	218
<i>H. Yamaguchi, H. Tamura, Y. Doi, Y. Tomita, T. Hamada, M. Kibune, S. Ohmoto, K. Tateishi, O. Tyshchenko, A. Sheikholeslami, T. Higuchi, J. Ogawa, T. Saito, H. Ishida, K. Gotoh</i>	
<b>A 20Gb/s 40mW Equalizer in 90nm CMOS Technology</b> .....	221
<i>S. A. Ibrahim, B. Razavi</i>	

## **SESSION 9: DIGITAL CIRCUITS & SENSORS**

<b>Overview</b> .....	224
<b>Within-die Variation-aware Dynamic-voltage-frequency Scaling Core Mapping and Thread Hopping for an 80-core Processor</b> .....	226
<i>S. Dighe, S. Vangal, P. Aseron, S. Kumar, T. Jacob, K. Bowman, J. Howard, J. Tschanz, V. Erraguntla, N. Borkar, V. De, S. Borkar</i>	
<b>Low-skew Clock Distribution Using Zero-phase-Clock-buffer DLLs</b> .....	229
<i>T. Wu, F. Aryanfar, H. C. Lee, J. Shen, T. Chin, C. Werner, K. Chang</i>	
<b>POWER7™ Local Clocking and Clocked Storage Elements</b> .....	232
<i>J. Warnock, L. Sigal, D. Wendel, K. P. Muller, J. Friedrich, V. Zyuban, E. Cannon, A. J. KleinOowski</i>	
<b>A 1.2 TB/s On-chip Ring Interconnect for 45nm 8-Core Enterprise Xeon® Processor</b> .....	234
<i>C. Park, R. Badeau, L. Biro, J. Chang, T. Singh, J. Vash, B. Wang, T. Wang</i>	
<b>High-bandwidth and Low-energy on-chip Signaling with Adaptive Pre-emphasis in 90nm CMOS</b> .....	237
<i>J. S. Seo, R. Ho, J. Lexau, M. Dayringer, D. Sylvester, D. Blaauw</i>	
<b>A Microcontroller-based PVT Control System for a 65nm 72Mb Synchronous SRAM</b> .....	240
<i>S. T. Eid, M. Whately, S. Krishnegowda</i>	
<b>Accurate Characterization of Random Process Variations Using a Robust Low-voltage High-Sensitivity Sensor Featuring Replica-bias Circuit</b> .....	243
<i>M. Meterelliyoz, A. Goel, J. P. Kulkarni, K. Roy</i>	
<b>In Situ Delay-Slack Monitor for High-performance Processors Using an All-digital Self-calibrating 5ps Resolution Time-to-digital Converter</b> .....	246
<i>D. Fick, N. Liu, Z. Foo, M. Fojtik, J. S. Seo, D. Sylvester, D. Blaauw</i>	
<b>Early Detection of Oxide Breakdown Through in Situ Degradation Sensing</b> .....	249
<i>P. Singh, Z. Foo, M. Wieckowski, S. Hanson, M. Fojtik, D. Blaauw, D. Sylvester</i>	
<b>A Precise-tracking NBTI-Degradation Monitor Independent of NBTI Recovery Effect</b> .....	252
<i>E. Saneyoshi, K. Nose, M. Mizuno</i>	

## **SESSION 10: DC-DC POWER CONVERSION**

<b>Overview</b> .....	255
-----------------------	-----

<b>A Two-phase Switching Hybrid Supply Modulator for Polar Transmitters with 9% Efficiency Improvement</b> .....	257
<i>Y. Wu, P. K. T. Mok</i>	
<b>A Robust Digital DC-DC Converter with Rail-to-Rail Output Range in 40nm CMOS</b> .....	260
<i>E. G. Soenen, A. Roth, J. Shi, M. Kinyua, J. Gaither, E. Ortynska</i>	
<b>A PLL-based High-stability Single-Inductor 6-channel Output DC-DC Buck Converter</b> .....	263
<i>K. C. Lee, C. S. Chae, G. H. Cho, G. H. Cho</i>	
<b>A 300mA 14mV-Ripple Digitally Controlled Buck Converter Using Frequency Domain <math>\Delta\Sigma</math> ADC and Hybrid PWM Generator</b> .....	266
<i>H. H. Ahmad, B. Bakkaloglu</i>	
<b>A 10MHz 92.1%-Efficiency Green-mode Automatic Reconfigurable Switching Converter with Adaptively Compensated Single-bound Hysteresis Control</b> .....	269
<i>C. Zheng, D. Ma</i>	
<b>Digitally Assisted Discontinuous Conduction Mode 5V/100MHz and 10V/45MHz DC-DC Boost Converters with Integrated Schottky Diodes in Standard 0.13<math>\mu</math>m CMOS</b> .....	272
<i>P. Li, L. Xue, D. Bhatia, R. Bashirullah</i>	
<b>A 0.16mm<sup>2</sup> Completely On-chip Switched-capacitor DC-DC Converter Using Digital Capacitance Modulation for LDO Replacement in 45nm CMOS</b> .....	275
<i>Y. Ramadass, A. Fayed, B. Haroun, A. Chandrakasan</i>	
<b>A 32nm Fully Integrated Reconfigurable Switched-capacitor DC-DC Converter Delivering 0.55W/mm<sup>2</sup> at 81% Efficiency</b> .....	278
<i>H. P. Le, M. Seeman, S. R. Sanders, V. Sathe, S. Naffziger, E. Alon</i>	

## **SESSION 11: RADAR, MM-WAVE, & LOW-POWER TRANSCEIVERS**

<b>Overview</b> .....	281
<b>A 4-channel 4-beam 24-to-26GHz Spatio-temporal RAKE Radar Transceiver in 90nm CMOS for Vehicular Radar Applications</b> .....	283
<i>H. Krishnaswamy, H. Hashemi</i>	
<b>A Fully Integrated 77GHz FMCW Radar System in 65nm CMOS</b> .....	286
<i>Y. A. Li, M. H. Hung, S. J. Huang, J. Lee</i>	
<b>A SiGe BiCMOS 16-element Phased-array Transmitter for 60GHz Communications</b> .....	289
<i>A. Valdes-Garcia, S. Nicolson, J. W. Lai, A. Natarajan, P. Y. Chen, S. Reynolds, J. H. C. Zhan, B. Floyd</i>	
<b>A Wideband mm-Wave CMOS Receiver for Gb/s Communications Employing Interstage Coupled Resonators</b> .....	292
<i>F. Vecchi, S. Bozzola, M. Pozzoni, D. Guermandi, E. Temporiti, M. Repposi, U. Decanis, A. Mazzanti, F. Svelto</i>	
<b>A 2.4GHz/915MHz 51<math>\mu</math>W Wake-up Receiver with Offset and Noise Suppression</b> .....	295
<i>X. Huang, S. Rampu, X. Wang, G. Dolmans, H. Groot</i>	
<b>A 2.4GHz 830pJ/bit Duty-cycled Wake-up Receiver with -82dBm Sensitivity for Crystal-less Wireless Sensor Nodes</b> .....	298
<i>S. Drago, D. M. W. Leenaerts, F. Sebastiano, L. J. Breems, K. A. A. Makinwa, B. Nauta</i>	
<b>An Ultra-low-power Interference-Robust IR-UWB Transceiver Chipset Using Self-Synchronizing OOK Modulation</b> .....	301
<i>M. Crepaldi, C. Li, K. Dronson, J. Fernandes, P. Kinget</i>	
<b>A Fully Integrated 802.15.4a IR-UWB Transceiver in 0.13<math>\mu</math>m CMOS with Digital RRC Synthesis</b> .....	304
<i>S. Joo, W. H. Chen, T. Y. Choi, M. K. Oh, J. H. Park, J. Y. Kim, B. Jung</i>	
<b>A 0.92/5.3nJ/b UWB Impulse Radio SoC for Communication and Localization</b> .....	307
<i>Y. J. Zheng, S. X. Diao, C. W. Ang, Y. Gao, F. C. Choong, Z. Chen, X. Liu, Y. S. Wang, X. J. Yuan, C. H. Heng</i>	

## **SESSION 12: EMERGING MEDICAL APPLICATIONS**

<b>Overview</b> .....	310
<b>Pain Control on Demand Based on Pulsed Radio-Frequency Stimulation of the Dorsal Root Ganglion Using a Batteryless Implantable CMOS SoC</b> .....	312
<i>C. W. Lin, H. W. Chiu, M. L. Lin, C. H. Chang, I. S. Ho, P. H. Fang, Y. C. Li, C. L. Wang, Y. C. Tsai, Y. R. Wen, W. P. Shih, Y. J. Yang</i>	
<b>Mixed-signal Integrated Circuits for Self-Contained Sub-Cubic Millimeter Biomedical Implants</b> .....	315
<i>E. Y. Chow, S. Charkaborty, W. J. Chappell, P. P. Irazoqui</i>	
<b>An Implantable 5mW/Channel Dual-Wavelength Optogenetic Stimulator for Therapeutic Neuromodulation Research</b> .....	318
<i>K. Paralikar, P. Cong, W. Santa, D. Dinsmoor, B. Hocken, G. Munns, J. Giftakis, T. Denison</i>	

<b>Compact Voltage and Current Stimulation Buffer for High-Density Microelectrode Arrays</b> .....	321
<i>P. Livi, F. Heer, U. Frey, D. J. Bakkum, A. Hierlemann</i>	

### **SESSION 13: FREQUENCY & CLOCK SYNTHESIS**

<b>Overview</b> .....	324
<b>A Low-area Switched-resistor Loop-filter Technique for Fractional-N Synthesizers Applied to a MEMS-based Programmable Oscillator</b> .....	326
<i>M. H. Perrott, S. Pamarti, E. Hoffman, F. S. Lee, S. Mukherjee, C. Lee, V. Tsinker, S. Perumal, B. Soto, N. Arumugam, B. W. Garlepp</i>	
<b>A 45nm SOI-CMOS Dual-PLL Processor Clock System for Multi-Protocol I/O</b> .....	329
<i>D. M. Fischette, A. L. S. Loke, M. M. Oshima, B. A. Doyle, R. Bakalski, R. J. DeSantis, A. Thiruvengadam, C. L. Wang, G. R. Talbot, E. S. Fang</i>	
<b>A 0.3mm<sup>2</sup> 90-to-770MHz Fractional-N Synthesizer for a Digital TV Tuner</b> .....	332
<i>M. Kondou, A. Matsuda, H. Yamazaki, O. Kobayashi</i>	
<b>A Low-Noise Frequency Synthesizer for Infrastructure Applications</b> .....	335
<i>S. Farahvash, W. Roberts, J. Easter, R. Wei, D. Stegmeir</i>	
<b>A 17.5-to-20.94GHz and 35-to-41.88GHz PLL in 65nm CMOS for Wireless HD Applications</b> .....	338
<i>O. Richard, A. Siligaris, F. Badets, C. Dehos, C. Dufis, P. Busson, P. Vincent, D. Belot, P. Urard</i>	

### **SESSION 14: NON-VOLATILE MEMORY**

<b>Overview</b> .....	341
<b>Negative-Resistance Read and Write Schemes for STT-MRAM in 0.13µm CMOS</b> .....	343
<i>D. Halupka, S. Huda, W. Song, A. Sheikholeslami, K. Tsumoda, C. Yoshida, M. Aoki</i>	
<b>A 64Mb MRAM with Clamped-reference and Adequate-reference Schemes</b> .....	346
<i>K. Tsuchida, T. Inaba, K. Fujita, Y. Ueda, T. Shimizu, Y. Asao, T. Kajiyama, M. Iwayama, K. Sugiura, S. Ikegawa, T. Kishi, T. Kai, M. Amano</i>	
<b>A 0.13µm 64Mb Multi-Layered Conductive Metal-oxide memory</b> .....	349
<i>C. J. Chevallier, C. H. Siau, S. F. Lim, S. R. Namala, M. Matsuoka, B. L. Bateman, D. Rinerson</i>	
<b>A Scalable Shield-bitline-overdrive Technique for 1.3V Chain FeRAM</b> .....	351
<i>D. Takashima, H. Shiga, D. Hashimoto, T. Miyakawa, S. Shiratake, K. Hoya, R. Ogiwara, R. Takizawa, S. Doumae, R. Fukuda, Y. Watanabe, S. Fujii, T. Ozaki, H. Kanaya</i>	
<b>A 2.5Gb/s/ch 4PAM Inductive-coupling Transceiver for Non-contact Memory Card</b> .....	354
<i>S. Kawai, H. Ishikuro, T. Kuroda</i>	
<b>A 0.29V Embedded NAND-ROM in 90nm CMOS for Ultra-low-voltage Applications</b> .....	357
<i>M. F. Chang, S. M. Yang, C. W. Liang, C. C. Chiang, P. F. Chiu, K. F. Lin, Y. H. Chu, W. C. Wu, H. Yamauchi</i>	
<b>A 90nm 4Mb Embedded Phase-Change Memory with 1.2V 12ns Read Access Time and 1MB/s Write Throughput</b> .....	360
<i>G. Sandre, L. Bettini, A. Pirola, L. Marmonier, M. Pasotti, M. Borghi, P. Mattavelli, P. Zuliani, L. Scotti, G. Mastracchio, F. Bedeschi, R. Gastaldi, R. Bez</i>	
<b>A 45nm 1Gb 1.8V Phase-Change Memory</b> .....	363
<i>C. Villa, D. Mills, G. Barkley, H. Giduturi, S. Schippers, D. Vimercati</i>	

### **SESSION 15: LOW-POWER PROCESSORS & COMMUNICATION**

<b>Overview</b> .....	365
<b>A 390Mb/s 3.57mm<sup>2</sup> 3GPP-LTE Turbo Decoder ASIC in 0.13µm CMOS</b> .....	367
<i>C. Studer, C. Benkeser, S. Belfanti, Q. Huang</i>	
<b>A 4.5mW Digital baseband Receiver for Level-A Evolved EDGE</b> .....	370
<i>C. Benkeser, A. Bubenhofer, Q. Huang</i>	
<b>A 477mW NoC-BASed Digital Baseband for MIMO 4G SDR</b> .....	373
<i>F. Clermidy, C. Bernard, R. Lemaire, J. Martin, I. Miro-Panades, Y. Thonnart, P. Volet, N. Wehn</i>	
<b>A 2Gb/s Network Processor with a 24mW IPsec Offload for Residential Gateways</b> .....	376
<i>Y. Nishida, K. Kawai, K. Koike</i>	
<b>A 45nm Resilient and Adaptive Microprocessor Core for Dynamic Variation Tolerance</b> .....	379
<i>J. Tschanz, K. Bowman, S. L. Lu, P. Aseron, M. Khellah, A. Raychowdhury, B. Geuskens, C. Tokunaga, C. Wilkerson, T. Karnik</i>	

<b>A Power-efficient 32b ARM ISA Processor Using Timing-error Detection and Correction for Transient-error Tolerance and Adaptation to PVT Variation</b> .....	382
<i>D. Bull, S. Das, K. Shivshankar, G. Dasika, K. Flautner, D. Blaauw</i>	
<b>A 45nm CMOS 13-Port 64-word 41b Fully Associative Content-addressable Register File</b> .....	385
<i>G. Burda, Y. Kolla, J. Dieffenderfer, F. Hamdan</i>	
<b>Millimeter-scale Nearly Perpetual Sensor System with Stacked Battery and Solar Cells</b> .....	387
<i>G. Chen, M. Fojtik, D. Kim, D. Fick, J. Park, M. Seok, M. T. Chen, Z. Foo, D. Sylvester, D. Blaauw</i>	

## **SESSION 16: HIGH-PERFORMANCE DATA CONVERTERS**

<b>Overview</b> .....	390
<b>A 16b 250MS/s IF-sampling Pipelined A/D Converter with Background Calibration</b> .....	392
<i>A M. A. Ali, A. Morgan, C. Dillion, G. Patterson, S. Puckett, M. Hensley, R. Stop, P. Boraskar, S. Bardsley, D. Lattimore, J. Bray, C. Speir, R. Sneed</i>	
<b>A 16b 100-to-160MS/s SiGe BiCMOS Pipelined ADC with 100dBFS SFDR</b> .....	395
<i>R. Payne, M. Corsi, D. Smith, S. Kaylor, D. Hsieh</i>	
<b>A 2.6mW 6b 2.2GS/s 4-times Interleaved Fully Dynamic Pipelined ADC in 40nm Digital CMOS</b> .....	398
<i>B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, G. Van-Der-Plas</i>	
<b>A Mostly Digital Variable-rate Continuous-time ADC <math>\Delta\Sigma</math> Modulator</b> .....	401
<i>G. Taylor, I. Galton</i>	
<b>A 10b 100MS/s 4.5mW Pipelined ADC with a Time Sharing Technique</b> .....	404
<i>Y. C. Huang, T. C. Lee</i>	
<b>A 1.4V Signal Swing Hybrid CLS-opamp/ZCBC Pipelined ADC Using a 300mV Output Swing Opamp</b> .....	407
<i>B. P. Hershberg, S. T. Weaver, U. K. Moon</i>	
<b>A 110dB SNR and 0.5mW Current-Steering Audio DAC Implemented in 45nm CMOS</b> .....	410
<i>R. Hezar, L. Risbo, H. Kiper, M. Fares, B. Haroun, G. Burra, G. Gomez</i>	

## **SESSION 17: SENSORS & MEMS**

<b>Overview</b> .....	413
<b>A System-on-chip EPC Gen-2 Passive UHF RFID Tag with Embedded Temperature Sensor</b> .....	415
<i>J. Yin, J. Yi, M. K. Law, Y. Ling, M. C. Lee, K. P. Ng, B. Gao, H. C. Luong, A. Bermak, M. Chan, W. H. Ki, C. Y. Tsui, M. M. F. Yuen</i>	
<b>A CMOS Temperature Sensor with an Energy-efficient Zoom ADC and an Inaccuracy of <math>\pm 0.25^\circ\text{C}</math> (<math>3\sigma</math>) from <math>-40^\circ\text{C}</math> to <math>125^\circ\text{C}</math></b> .....	418
<i>K. Souri, M. Kashmiri, K. Makinwa</i>	
<b>a 1.2v <math>10\mu\text{W}</math> NPN-based Temperature Sensor in 65nm CMOS with an Inaccuracy of <math>\pm 0.2^\circ\text{C}</math> (<math>3\sigma</math>) from <math>-70^\circ\text{C}</math> to <math>125^\circ\text{C}</math></b> .....	421
<i>F. Sebastiano, L. J. Breems, K. A. A. Makinwa, S. Drago, D. M. W. Leenaerts, B. Nauta</i>	
<b>A Thermal-diffusivity-based Temperature Sensor with an Untrimmed Inaccuracy of <math>\pm 0.2^\circ\text{C}</math> (<math>3\sigma</math>) from <math>-55^\circ\text{C}</math> to <math>125^\circ\text{C}</math></b> .....	424
<i>C. P. L. Van-Vroonhoven, D. D. Aquino, K. A. A. Makinwa</i>	
<b>An In-situ Temperature-sensing Interface Based on a SAR ADC in 45nm LP Digital CMOS for the Frequency-temperature Compensation of Crystal Oscillators</b> .....	427
<i>Z. Wang, R. Lin, E. Gordon, H. Lakdawala, L. R. Carley, J. C. Jensen</i>	
<b>A 76dB<math>\Omega</math> 1.7GHz 0.18<math>\mu\text{m}</math> CMOS Tunable Transimpedance Amplifier Using Broadband Current Pre-amplifier for High Frequency Lateral Micromechanical Oscillators</b> .....	430
<i>H. M. Lavasani, W. Pan, B. Harrington, R. Abdolvand, F. Ayazi</i>	
<b>A Closed-loop SC Interface for a <math>\pm 1.4g</math> Accelerometer with .33% Nonlinearity and <math>2\mu\text{g}/\sqrt{\text{Hz}}</math> Input Noise Density</b> .....	433
<i>M. Yucetas, J. Salomaa, A. Kalanti, L. Aaltonen, K. Halonen</i>	
<b>A 200MHz 300ps 0.5pJ/ns Optical Pulse Generator Array in .35<math>\mu\text{m}</math> CMOS</b> .....	436
<i>B. R. Rae, J. McKendry, Z. Gong, E. Gu, D. Renshaw, M. D. Dawson, R. K. Henderson</i>	

## **SESSION 18: POWER-EFFICIENT MEDIA PROCESSING**

<b>Overview</b> .....	439
-----------------------	-----



<b>A 222mW H.264 Full-HD Decoding Application Processor with x512b Stacked DRAM in 40nm</b> .....	441
<i>Y. Kikuchi, M. Takahashi, T. Maeda, H. Hara, H. Arakida, H. Yamamoto, Y. Hagiwara, T. Fujita, M. Watanabe, T. Shimazawa, Y. Ohara, T. Miyamori, M. Hamada, M. Takahashi, Y. Oowaki</i>	
<b>A 320mV-to-1.2V on-die Fine-grained Reconfigurable Fabric for DSP/Media Accelerators in 32nm CMOS</b> .....	444
<i>A. Agarwal, S. K. Mathew, S. K. Hsu, M. A. Anders, H. Kaul, F. Sheikh, R. Ramanarayanan, S. Srinivasan, R. Krishnamurthy, S. Borkar</i>	
<b>A 59.5mW Scalable/Multi-view Video Decoder Chip for Quad/3D Full HDTV and Video Streaming Applications</b> .....	447
<i>T. D. Chuang, P. K. Tsung, P. C. Lin, L. M. Chang, T. C. Ma, Y. H. Chen, L. G. Chen</i>	
<b>A 345mW Heterogeneous Many-core Processor with an Intelligent Inference Engine for Robust Object Recognition</b> .....	450
<i>S. Lee, J. Oh, M. Kim, J. Park, J. Kwon, H. J. Yoo</i>	
<b>A Scalable Massively Parallel Processor for Real-time Image Processing</b> .....	453
<i>T. Kurafuji, M. Haraguchi, M. Nakajima, T. Gyoten, T. Nishijima, H. Yamasaki, Y. Lmai, M. Lshizaki, T. Kumaki, Y. Okuno, T. Koide, H. J. Mattausch, K. Arimoto</i>	
<b>A Graphics and Vision Unified Processor with 0.89<math>\mu</math>W/fps Pose Estimation Engine for Augmented Reality</b> .....	456
<i>J. S. Yoon, J. H. Kim, H. E. Kim, W. Y. Lee, S. H. Kim, K. Chung, J. S. Park, L. S. Kim</i>	
<b>A Multimedia Semantic Analysis SoC (SASoC) with Machine-Learning Engine</b> .....	459
<i>T. W. Chen, Y. L. Chen, T. Y. Cheng, C. S. Tang, P. K. Tsung, T. D. Chuang, L. G. Chen, S. Y. Chien</i>	

## **SESSION 19: HIGH-PERFORMANCE EMBEDDED MEMORY**

<b>Overview</b> .....	462
<b>A 45nm SOI Embedded DRAM Marco for POWER7™ 32MB On-chip L3 Cache</b> .....	464
<i>J. Barth, D. Plass, E. Nelson, C. Hwang, G. Fredeman, M. Sperling, A. Mathews, W. Reohr, K. Nair, N. Cao</i>	
<b>A 32kB 2R/1W L1 Data Cache in 45nm SOI Technology for the POWER7™ Processor</b> .....	467
<i>J. Pille, D. Wendel, O. Wagner, R. Sautter, W. Penth, T. Froehnel, S. Buettner, O. Torreiter, M. Eckert, J. Paredes, D. Hrusecky, D. Ray</i>	
<b>A 32nm High-K Metal Gate SRAM with Adaptive Dynamic Stability Enhancement for Low-Voltage Operation</b> .....	470
<i>H. Nho, P. Kolar, F. Hamzaoglu, Y. Wang, E. Karl, U. Bhattacharya, K. Zhang</i>	
<b>A Configurable SRAM with Constant-negative-level Write Buffer for Low-voltage Operation with 0.149<math>\mu</math>m<sup>2</sup> Cell in 32nm High-K Metal-gate CMOS</b> .....	473
<i>Y. Fujimura, O. Hirabayashi, T. Sasaki, A. Suzuki, A. Kawasumi, Y. Takeyama, K. Kushida, G. Fukano, A. Katayama, Y. Niki, T. Yabe</i>	
<b>A 512kb 8T SRAM Macro Operating Down to 0.57V with an AC-coupled Sense Amplifier and Embedded Data-retention-voltage Sensor in 45nm SOI CMOS</b> .....	476
<i>M. Qazi, K. Stawiasz, L. Chang, A. Chandrakasan</i>	
<b>PVT-and-Aging Adaptive Worldline Boosting for 8T SRAM Power Reduction</b> .....	479
<i>A. Raychowdhury, B. Geuskens, J. Kulkarni, J. Tschanz, K. Bowman, T. Karnik, S. L. Lu, V. De, M. M. Khellah</i>	
<b>SRAM Stability Characterization Using Tunable Ring Oscillators in 45nm CMOS</b> .....	482
<i>J. Tsai, S. O. Toh, Z. Guo, L. T. Pang, T. J. K. Liu, B. Nikolic</i>	
<b>A 0.5V 100MHz PD-SOI SRAM with Enhanced Read Stability and Write Margin by Asymmetric MOSFET and Forward Body Bias</b> .....	485
<i>K. Nii, M. Yabuuchi, Y. Tsukamoto, Y. Hirano, T. Iwamatsu, Y. Kihara</i>	

## **SESSION 20: NEXT-GENERATION OPTICAL & ELECTRICAL INTERFACES**

<b>Overview</b> .....	488
<b>100b/s 15mW Optical Receiver with Integrated Germanium Photodetector and Hybrid Inductor Peaking in 0.13<math>\mu</math>m SOI CMOS Technology</b> .....	490
<i>D. Kucharski, D. Guckenberger, G. Masini, S. Abdalla, J. Witzens, S. Sahni</i>	
<b>An 8.5Gb/s CMOS OEIC with On-Chip Photodiode for Short-Distance Optical Communications</b> .....	493
<i>D. Lee, J. Han, E. Chang, G. Han, S. M. Park</i>	
<b>A 1.296-to-5.184Gb/s Transceiver with 2.4mW/(Gb/s) Burst-mode CDR using Dual-edge Injection-Locked Oscillator</b> .....	496
<i>K. Maruko, T. Sugioka, H. Hayashi, Z. Zhou, Y. Tsukuda, Y. Yagishita, H. Konishi, T. Ogata, H. Owa, T. Niki, K. Konda, M. Sato, H. Shiroshita, T. Ogura, T. Aoki, H. Kihara, S. Tanaka</i>	

<b>A 78mW 11.8Gb/s Serial Link Transceiver with Adaptive RX Equalization and Baud-rate CDR in 32nm CMOS</b> .....	499
<i>F. Spagna, L. Chen, M. Deshpande, Y. Fan, D. Gambetta, S. Gowder, S. Iyer, R. Kumar, P. Kwok, R. Krishnamurthy, C. C. Lin, R. Mohanavelu, R. Nicholson, J. Ou, M. Pasquarella, K. Prasad, H. Rustam, L. Tong, A. Tran, J. Wu, X. Zhang</i>	
<b>A 12.3mW 12.5Gb/s Complete Transceiver in 65nm CMOS</b> .....	502
<i>K. Fukuda, H. Yamashita, G. Ono, R. Nemoto, E. Suzuki, T. Takemoto, F. Yuki, T. Saito</i>	
<b>A 32mW 7.4Gb/s Protocol-Agile Source-series-terminated Transmitter in 45nm CMOS SOI</b> .....	505
<i>W. D. Dettloff, J. C. Eble, L. Luo, P. Kumar, F. Heaton, T. Stone, B. Daly</i>	
<b>A 5-to-25Gb/s 1.6-to-3.8mW/(Gb/s) Reconfigurable Transceiver in 45nm CMOS</b> .....	508
<i>G. Balamurugan, F. O'Mahony, M. Mansuri, J. E. Jaussi, J. T. Kennedy, B. Casper</i>	
<b>A 2x25Gb/s Deserializer with 2:5 DMUX for 100Gb/s Ethernet Applications</b> .....	511
<i>K. C. Wu, J. Lee</i>	

## **SESSION 21: SUCCESSIVE-APPROXIMATION ADCs**

<b>Overview</b> .....	514
<b>An 18b 12.5MHz ADC with 93dB SNR</b> .....	516
<i>C. P. Hurrell, C. Lyden, D. Laing, D. Hummerston, M. Vickery</i>	
<b>A 12b 22.5/45MS/s 3.0mW 0.059mm<sup>2</sup> CMOS SAR ADC Achieving Over 90dB SFDR</b> .....	519
<i>W. Liu, P. Huang, Y. Chiu</i>	
<b>A 0.06mm<sup>2</sup> 8.9b ENOB 40MS/s Pipelined SAR ADC in 65nm CMOS</b> .....	522
<i>M. Furuta, M. Nozawa, T. Itakura</i>	
<b>A 10b 50MS/s 820μW SAR ADC with On-Chip Digital Calibration</b> .....	525
<i>M. Yoshioka, K. Ishikawa, T. Takayama, S. Tsukamoto</i>	
<b>A 10b 100MS/s 1.13mW SAR ADC with Binary-Scaled Error Compensation</b> .....	528
<i>C. C. Liu, S. J. Chang, G. Y. Huang, Y. Z. Lin, C. M. Huang, C. H. Huang, L. Bu, C. C. Tsai</i>	
<b>A 30fj/Conversion-step 8b 0-to-10MS/s Asynchronous SAR ADC in 90nm CMOS</b> .....	531
<i>P. Harpe, C. Zhou, X. Wang, G. Dolmans, H. Groot</i>	
<b>A 40GS/s 6b ADC in 65nm CMOS</b> .....	534
<i>Y. M. Greshishchev, J. Aguirre, M. Besson, R. Gibbins, C. Falt, P. Flenke, N. Ben-Hamida, D. Pollex, P. Schvan, S. C. Wang</i>	

## **SESSION 22: IMAGE SENSORS**

<b>Overview</b> .....	537
<b>A 2.1Mpixel 120pixel 120frame/s CMOS Image Sensor with Column-parallel <math>\Delta\Sigma</math> ADC Architecture</b> .....	539
<i>Y. Chae, J. Cheon, S. Lim, D. Lee, M. Kwon, K. Yoo, W. Jung, D. H. Lee, S. Ham, G. Han</i>	
<b>A 1.1e Temporal Noise 1/3.2-inch 8Mpixel CMOS Image Sensor Using Pseudo-multiple Sampling</b> .....	542
<i>Y. Lim, K. Koh, K. Kim, H. Yang, J. Kim, Y. Jeong, S. Lee, H. Lee, S. H. Lim, Y. Han, J. Kim, J. Yun, S. Ham, Y. T. Lee</i>	
<b>A 2.7e Temporal Noise 99.7% Shutter Efficiency 92dB Dynamic Range CMOS Image Sensor with Dual Global Shutter Pixels</b> .....	545
<i>K. Yasutomi, S. Itoh, S. Kawahito</i>	
<b>A QVGA 143dB Dynamic Range Asynchronous Address-event PWM Dynamic Image Sensor with Lossless Pixel-Level Video Compression</b> .....	548
<i>C. Posch, D. Matolin, R. Wohlgenannt</i>	
<b>A CMOS Image Sensor for 10Mb/s 70m-Range LED-Based Spatial Optical Communication</b> .....	551
<i>S. Itoh, I. Takai, S. Z. Sarker, M. Hamai, K. Yasutomi, M. Andoh, S. Kawahito</i>	
<b>A 256x256 14k Range Maps/s 3-D Range Finding Image Sensor Using Row-Parallel Embedded Binary Search Tree and Address Encoder</b> .....	554
<i>S. Mandai, M. Ikeda, K. Asada</i>	
<b>An 80x60 Range Image Sensor Based on 10μm 50MHz Lock-in Pixels in 0.18μm CMOS</b> .....	557
<i>D. Stoppa, N. Massari, L. Pancheri, M. Malfatti, M. Perenzoni, L. Gonzo</i>	
<b>A 2.2/3-inch 4K2K CMOS Image Sensor Based on Dual Resolution and Exposure Technique</b> .....	560
<i>T. Azuma, T. Imagawa, S. Ugawa, Y. Okada, H. Komobuchi, M. Ishii, S. Kasuga, Y. Kato</i>	
<b>A 1/2.3-inch 10.3Mpixel 50frame/s Back-Illuminated CMOS Image Sensor</b> .....	563
<i>H. Wakabayashi, K. Yamaguchi, M. Okano, S. Kuramochi, O. Kumagai, S. Sakane, M. Ito, M. Hatano, M. Kikuchi, Y. Yamagata, T. Shikanai, K. Koseki, K. Mabuchi, Y. Maruyama, K. Akiyama, E. Miyata, T. Honda, M. Ohashi, T. Nomoto</i>	

## **SESSION 23: MM-WAVE TRANSCEIVERS, POWER AMPLIFIERS & SOURCES**

<b>Overview</b> .....	566
<b>A Millimeter-wave Intra-Connect Solution</b> .....	568
<i>K. Kawasaki, Y. Akiyama, K. Komori, M. Uno, H. Takeuchi, T. Itagaki, Y. Hino, Y. Kawasaki, K. Ito, A. Hajimiri</i>	
<b>A SiGe Quadrature Transmitter and Receiver Chipset for Emerging High-Frequency Applications at 160GHz</b> .....	571
<i>U. R. Pfeiffer, E. Ojefors, Y. Zhao</i>	
<b>A W-Band 65nm CMOS Transmitter Front-end with 8GHz IF Bandwidth and 20dB IR-Radio</b> .....	574
<i>D. Sandstrom, M. Varonen, M. Karkkainen, K. A. I. Halonen</i>	
<b>A 90GHz-Carrier 30GHz-Bandwidth Hybrid Switching Transmitter with Integrated Antenna</b> .....	577
<i>A. Arbabian, B. Afshar, J. C. Chien, S. Kang, S. Callender, E. Adabi, S. D. Toso, R. Pilard, D. Gloria, A. Niknejad</i>	
<b>A 13.1% Tuning Range 115GHz Frequency Generator Based on an Injection-Locked Frequency Doubler in 65nm CMOS</b> .....	580
<i>A. Mazzanti, E. Monaco, M. Pozzoni, F. Svelto</i>	
<b>A 1V 17.9dBm 60GHz Power Amplifier in Standard 65nm CMOS</b> .....	583
<i>J. W. Lai, A. Valdes-Garcia</i>	
<b>A High-gain 60GHz Power Amplifier with 20dBm Output Power in 90nm CMOS</b> .....	586
<i>C. Y. Law, A. V. Pham</i>	
<b>A 53-to-68GHz 18dBm Power Amplifier with an 8-Way Combiner in Standard 65nm CMOS</b> .....	589
<i>B. Marineau, V. Knoplik, A. Siligaris, F. Giancesello, D. Belot</i>	
<b>A 650GHz SiGe Receiver Front-end for Terahertz Imaging Arrays</b> .....	591
<i>E. Ojefors, U. R. Pfeiffer</i>	

## **SESSION 24: DRAM & FLASH MEMORIES**

<b>Overview</b> .....	594
<b>A 7Gb/s/pin GDDR5 SDRAM with 2.5ns Bank-to-bank Active Time and No Bank-group Restriction</b> .....	596
<i>T. Y. Oh, Y. S. Sohn, S. J. Bae, M. S. Park, J. H. Lim, Y. K. Cho, D. H. Kim, D. M. Kim, H. R. Kim, H. J. Kim, J. H. Kim, J. K. Kim, S. H. Kwak, J. H. Lee, J. Y. Lee, C. H. Shin, Y. S. Yang, B. S. Cho, S. Y. Bang, Y. R. Chol, G. S. Moon, C. G. Park, S. W. Hwang, J. D. Lim, J. S. Chol, Y. H. Jun</i>	
<b>An 8Tb/s 1pJ/b 0.8mm<sup>2</sup>/Tb/s QDR Inductive-coupling interface Between 65nm CMOS GPU and 0.1µm DRAM</b> .....	599
<i>N. Miura, K. Kasuga, M. Saito, T. Kuroda</i>	
<b>A Bitline Sense Amplifier for Offset Compensation</b> .....	602
<i>M. J. Lee, M. Kyung, H. S. Won, M. S. Lee, K. W. Park</i>	
<b>A 2Gb/s 1.8pJ/b/chip Inductive-coupling Through-chip Bus for 128-die NAND-flash Memory Stacking</b> .....	605
<i>M. Saito, N. Miura, T. Kuroda</i>	
<b>A 159mm<sup>2</sup> 32nm 32Gb MLC NAND-flash Memory with 200MB/s Asynchronous DDR interface</b> .....	608
<i>H. Kim, J. H. Park, K. T. Park, P. Kwak, O. Kwon, C. Kim, Y. Lee, S. Park, K. Kim, D. Cho, J. Lee, J. Song, S. Lee, H. Yoo, S. Kim, S. Yu, S. Kim, Y. H. Lim</i>	
<b>A 3bit/Cell 32Gb NAND Flash Memory at 34nm with 6MB/s Program Throughput and with Dynamic 2b.Cel Blocks Configuration Mode for a Program Throughput Increase up to 13MB/s</b> .....	610
<i>G. G. Marotta, A. Macerola, A. D'Alessandro, A. Torsi, C. Cerafogli, C. Lattaro, C. Musilli, D. Rivers, E. Sirizotti, F. Paolini, G. Imondi, G. Naso, G. Santin, L. Botticchio, L. Santis, L. Pilolli, M. L. Gallese, M. Incarnati, M. Tiburzi, P. Conenna, S. Perugini, V. Moschiano, W. Francesco, M. Goldman, C. Hald, D. Cicco, D. Orlandi, F. Rori, M. Rossini, T. Vali, R. Ghodsi, F. Roohparvar</i>	
<b>A 32Gb MLC NAND-flash Memory with V<sub>th</sub>-endurance-enhancing Schemes in 32nm CMOS</b> .....	613
<i>C. Lee, S. K. Lee, S. Ahn, J. Lee, W. Park, Y. Cho, C. Jang, C. Yang, S. Chung, S. Chung, B. Joo, B. Jeong, J. Kim, J. Kwon, H. Jin, Y. Noh, J. Ha, M. Sung, D. Choi, S. Kim, J. Choi, T. Jeon, J. S. Yang, Y. H. Koh</i>	

## **SESSION 25: WIRELESS CONNECTIVITY**

<b>Overview</b> .....	616
<b>A Maximally-Digital Radio Receiver Front-end</b> .....	618
<i>F. Opteynde</i>	
<b>A 65nm CMOS 2.4GHz 31.5dBm Power Amplifier with a Distributed LC Power-Combining Network and Improved Linearization for WLAN Applications</b> .....	620
<i>A. Afsahi, A. Behzad, L. E. Larson</i>	

<b>A MultiStandard, Multiband SoC with Integrated BT, FM, WLAN Radios and Integrated Power Amplifier</b> .....	623
<i>C. P. Lee, A. Behzad, B. Marholev, V. Magoon, I. Bhatti, D. Li, S. Bothra, A. Afsahi, D. Ojo, R. Roufoogaran, T. Li, Y. Chang, K. R. Rao, S. Au, P. Seetharam, K. Carter, J. Rael, M. Macintosh, B. Lee, M. Rofougaran, R. Rofougaran, A. Hadji-Abdolhamid, M. Nariman, S. Khorram, S. Anand, E. Chien, S. Wu, C. Barrett, L. Zhang, A. Zolfaghari, H. Darabi, A. Sarfaraz, B. Ibrahim, M. Gonikberg, M. Forbes, C. Fraser, L. Gutierrez, Y. Gonikberg, M. Hafizi, S. Mak, J. Castaneda, K. Kim, Z. Liu, S. Bouras, K. Chien, V. Chandrasekar, P. Chang, E. Li, Z. Zhao</i>	
<b>A Fully Integrated 2x1 Dual-band Direct-conversion Transceiver with Dual-Mode Fractional Divider and Noise-Shaping TIA for Mobile WiMAX SoC in 65nm CMOS</b> .....	626
<i>J. Deguchi, D. Miyashita, Y. Ogasawara, G. Takemura, M. Iwanaga, K. Sami, R. Ito, J. Wadatsumi, Y. Tsuda, S. Oda, S. Kawaguchi, N. Itoh, M. Hamada</i>	
<b>A 5mm<sup>2</sup> 40nm LP CMOS 0.1-to-3GHz Multistandard Transceiver</b> .....	629
<i>M. Ingels, V. Giannini, J. Borremans, G. Mandal, B. Debaillie, P. Van-Wesemael, T. Sano, T. Yamamoto, D. Hauspie, J. Van-Driessche, J. Craninckx</i>	
<b>A 65nm CMOS Low-power Small-size Multistandard, Multiband Mobile Broadcasting Receiver SoC</b> .....	632
<i>M. Jeong, B. Kim, Y. Cho, Y. Kim, S. Kim, H. Yoo, J. Lee, J. K. Lee, K. S. Jung, J. Lee, J. Lee, H. Yang, G. Taylor, B. E. Kim</i>	
<b>A Multistandard Multiband Mobile TV RF SoC in 65nm CMOS</b> .....	635
<i>J. H. Chang, H. Kim, J. H. Choi, H. Chung, J. Heo, S. Kang, J. D. Bae, H. Oh, Y. Kim, T. W. Kwon, R. Kim, W. Choo, D. Rhee, B. H. Park</i>	
<b>A 1V RF SoC With an 863-to-928MHz 400kb/s Radio and a 32b Dual-MAC DSP Core for Wireless Sensor and Body Networks</b> .....	638
<i>E. Roux, N. Scolari, B. Banerjee, C. Arm, P. Volet, D. Sigg, P. Heim, J. F. Perotto, F. Kaess, N. Raemy, A. Vouilloz, D. Ruffieux, M. Contaldo, F. Giroud, D. Severac, M. Morgan, S. Gyger, C. Monneron, T. C. Le, C. Henzelin, V. Peiris</i>	

## **SESSION 26: HIGH-PERFORMANCE & DIGITAL PLLs**

<b>Overview</b> .....	641
<b>A 3.5GHz Wideband ADPLL with Fractional Spur Suppression Through TDC Dithering and Feedforward Compensation</b> .....	643
<i>C. Weltin-Wu, E. Temporiti, D. Baldi, M. Cusmai, F. Svelto</i>	
<b>A 2.1-to-2.8GHz All-Digital Frequency Synthesizer with a Time-windowed TDC</b> .....	646
<i>T. Tokairin, M. Okada, M. Kitsunozuka, T. Maeda, M. Fukaiishi</i>	
<b>A Calibration-free 800MHz Fractional-N Digital PLL with Embedded TDC</b> .....	649
<i>M. Shuo-Wei, D. Su, S. Mehta</i>	
<b>Spur-Reduction Techniques for PLLs Using Sub-sampling Phase Detection</b> .....	652
<i>X. Gao, A. M. Klumperink, G. Soccì, M. Bohsali, B. Nauta</i>	
<b>A 3MHz-BW 3.6GHz Digital Fractional-N PLL with Sub-gate-delay TDC, Phase-interpolation Divider, and Digital Mismatch Cancellation</b> .....	655
<i>M. Zamuso, S. Levantino, C. Samori, A. Lacaita</i>	
<b>A 1.4ps<sub>rms</sub>-Period-jitter TDC-less Fractional-N Digital PLL with Digitally Controlled Ring Oscillator in 65nm CMOS</b> .....	658
<i>W. Grollitsch, R. Nonis, N. Dalt</i>	
<b>A 86MHz-to-12GHz Digital-intensive Phase-modulated Fractional-N PLL Using a 15pJ/Shot 5ps TDC in 40nm Digital CMOS</b> .....	661
<i>J. Borremans, K. Vengattaramane, V. Giannini, J. Craninckx</i>	
<b>A 1GHz ADPLL with a 1.25ps Minimum-Resolution Sub-Exponent TDC in 0.18µm CMOS</b> .....	664
<i>S. K. Lee, Y. H. Seo, Y. Suh, H. J. Park, J. Y. Sim</i>	

## **SESSION 27: DIRECTIONS IN HEALTH, ENERGY & RF**

<b>Overview</b> .....	667
<b>A Batteryless Thermoelectric Energy-harvesting Interface Circuit with 35mV Startup Voltage</b> .....	669
<i>Y. K. Ramadass, A. P. Chandrakasan</i>	
<b>Palm NMR and One-chip NMR</b> .....	672
<i>N. Sun, T. J. Yoon, H. Lee, W. Andress, V. Demas, P. Prado, R. Weissleder, D. Ham</i>	
<b>A 3.9mW 25-Electrode Reconfigured Thoracic Impedance/ECG SoC with Body-Channel Transponder</b> .....	675
<i>L. Yan, J. Bae, S. Lee, B. Kim, T. Roh, K. Song, H. J. Yoo</i>	

<b>A Multichannel DNA SoC for Rapid Point-of-care Gene Detection</b> .....	678
<i>D. M. Garner, H. Bai, P. Georgiou, T. G. Constandinou, S. Reed, L. M. Shepherd, W. Wong, K. T. Lim, C. Toumazou</i>	
<b>A Single-Inductor AC-DC Piezoelectric Energy-harvester/Battery-charger IC Converting ±(0.35 to 1.2V) to (2.7 to 4.5V)</b> .....	681
<i>D. Kwon, G. A. Rincon-Mora</i>	
<b>A 110µW 10Mb/s eTextiles Transceiver for Body Area Networks with Remote Battery Power</b> .....	684
<i>P. P. Mercier, A. P. Chandrakasan</i>	
<b>A 5.4dBm 42mW 2.4GHz CMOS BAW-based Quasi-direct Conversion Transmitter</b> .....	687
<i>M. Contaldo, D. Ruffieux, C. Enz</i>	
<b>An 8.6GHz 42ps Pulse-width Electrical Mode-locked Oscillator</b> .....	690
<i>M. W. Chen, D. S. Ricketts</i>	
<b>Ultra-low-voltage Circuits for Sensor Applications Powered by Free-space Optics</b> .....	692
<i>T. Kleeburg, J. Loo, N. J. Guilar, E. Fong, R. Amirtharajah</i>	
<b>Nano-watt Power Management and Vibration Sensing on a Dust-size Batteryless Sensor Node for Ambient Intelligence Applications</b> .....	695
<i>T. Shimamura, M. Ugajin, K. Suzuki, K. Ono, N. Sato, K. Kuwabara, H. Morimura, S. Mutoh</i>	

## **SHORT COURSE**

<b>CMOS Phase-Locked Loops for Frequency Synthesis</b> .....	698
--	-----

## **EVENING SESSIONS**

<b>ES1: Beyond CMOS - Emerging Technologies</b> .....	699
<b>ES2: Student Research Preview</b> .....	700
<b>ES3: Energy-Efficient High-Speed Interfaces</b> .....	701
<b>ES4: Fusion of MEMS and Circuits</b> .....	703
<b>EP1: Analog Circuits: Stump the Panel</b> .....	705
<b>ES5: Can RF SoCs (Self) Test Their Own RF?</b> .....	707
<b>ES6: Can we Rebuild Them? Bionics Beyond 2010</b> .....	709
<b>EP2: The Semiconductor Industry in 2025</b> .....	711

## **TUTORIALS**

<b>ISSCC 2010/Tutorials</b> .....	713
<b>F1: Silicon 3D-Integration Technology and Systems</b> .....	715
<b>F2: Reconfigurable RF and Data Converters</b> .....	717
<b>F3: Transceiver Circuits for Optical Communications</b> .....	719
<b>F4: High-Speed Image Sensor Technologies</b> .....	721
<b>F5: Circuits for Portable Medical Electronic Systems</b> .....	723
<b>F6: Signal and Power Integrity for SoCs</b> .....	725

**Author Index**