

2010 VI Southern Programmable Logic Conference

(SPL 2010)

**Ipojuca, Pernambuco, Brazil
24 – 26 March 2010**



**IEEE Catalog Number: CFP1021B-PRT
ISBN: 978-1-4244-6309-1**

TABLE OF CONTENTS

Session 1 - Embedded Processors and IP Cores1

The Supersmall Soft Processor, James Robinson, *University of Toronto, Canada*, Sam Vafae, *University of Toronto, Canada*, Jonathan Scobbie, *University of Toronto, Canada*, Michael Ritche, *University of Toronto, Canada*, Jonathan Rose, *University of Toronto, Canada*3

LIBOR Market Model Simulation on an FPGA Parallel Machine, Xiang Tian, *The University of Edinburgh, United Kingdom*, Khaled Benkrid, *The University of Edinburgh, United Kingdom*9

Protection of Microprocessor-based Cores for FPL Devices, Luis Parrilla, *University of Granada, Spain*, Encarnación Castillo, *University of Granada, Spain*, Antonio García, *University of Granada, Spain*, Daniel González, *University of Granada, Spain*, Antonio Lloris, *University of Granada, Spain*, Elías Todorovich, *Universidad Autónoma de Madrid, Spain*, Eduardo Boemo, *Universidad Autónoma de Madrid, Spain*15

FPGA-Based Smart Sensor Implementation With Precise Frequency to Digital Converter for Flow Measurement, Edval J P Santos, *Universidade Federal de Pernambuco, Brazil*, Leonardo B. M. Silva, *Universidade Federal de Pernambuco, Brazil*.....21

Session 2 - System-on-Chip27

A Genetic Programming Based Approach for Efficiently Exploring Architectural Communication Design Space of MPSOCS, Guilherme Esmeraldo, *Federal University of Pernambuco, Brazil*, Edna Barros, *Federal University of Pernambuco, Brazil*.....29

An Environment for Energy Consumption Analysis of Cache Memories in SOC Platforms, Filipe R. Cordeiro, *UFPE, Brazil*, Abel G. Silva-Filho, *UFPE, Brazil*, Cristiano C. Araújo, *UFPE, Brazil*, Milena Gomes, *UFPE, Brazil*, Edna N. S. Barros, *UFPE, Brazil*, M. E. Lima, *UFPE, Brazil*35

The Development of a Hardware Abstraction Layer Generator for System-on-Chip Functional Verification, Tiago Lins, *Federal University of Pernambuco, Brazil*, Edna Barros, *Federal University of Pernambuco, Brazil*41

A Placement Tool for a NOC-Based Dynamically Reconfigurable System, Mario Raffo, *University of São Paulo, Brazil*, Jonas Gomes Filho, *University of São Paulo, Brazil*, Marius Strum, *University of São Paulo, Brazil*, Wang Jiang Chau, *University of São Paulo, Brazil*47

Session 3 - Computer Arithmetic Chip53

FPGA Based Floating-point Library for CORDIC Algorithms, Daniel M. Muñoz, *University of Brasília, Brazil*, Diego F. Sanchez, *University of Brasília, Brazil*, Carlos LLanos, *University of Brasília, Brazil*, Mauricio Ayala-Rincón, *University of Brasília, Brazil*55

Montgomery Modular Multiplication on Reconfigurable Hardware: Fully Systolic Array vs Parallel Implementation, Guilherme Perin, *Universidade Federal de Santa Maria, Brazil*, Daniel Gomes Mesquita, *Universidade Federal de Santa Maria, Brazil*, Fernando Luis Herrmann, *Universidade Federal de Santa Maria, Brazil*, João Baptista dos Santos Martins, *Universidade Federal de Santa Maria, Brazil*61

Decimal division: algorithms and FPGA implementations, Jean-Pierre Deschamps, *University Rovira i Virgili, Spain*, Gustavo Sutter, *Universidad Autonoma de Madrid, Spain*67

Parallel Decimal Multipliers using Binary Multipliers, Mário P. Véstias, *INESC-ID/ISEL, Portugal*, Horácio C. Neto, *INESC-ID/IST, Portugal*73

Session 4 - Image Processing and Vision79

A High Performance Hardware Architecture for the H.264/AVC Half-Pixel Interpolation Unit, Marcel Corrêa, *Universidade Federal de Pelotas, Brazil*, Mateus Schoenknecht, *Universidade Federal de Pelotas, Brazil*, Robson Dornelles, *Universidade Federal de Pelotas, Brazil*, Luciano Agostini, *Universidade Federal de Pelotas, Brazil*81

FPGA-based Real Time Processing of the Plenoptic Wavefront Sensor for the European Solar Telescope (EST), Yolanda Martin, *Instituto de Astrofísica de Canarias (IAC), Spain*, Luis Fernando Rodríguez-Ramos, *Instituto de Astrofísica de Canarias (IAC), Spain*, Javier García-Jiménez, *Instituto de Astrofísica de Canarias (IAC), Spain*, Jose Javier Diaz-García, *Instituto de Astrofísica de Canarias (IAC), Spain*, Jose Maria Rodriguez-Ramos, *Universidad de La Laguna (ULL), Spain*87

Architecture for Binary Mathematical Morphology Reconfigurable by Genetic Programming, Emerson Carlos Pedrino, *Federal University of São Carlos, Brazil*,

José Hiroki Saito, *Federal University of São Carlos, Brazil*, Valentin Obac Roda, *São Paulo University, Brazil*93

An Optimized Label-Broadcast Parallel Algorithm for Connected Components Labeling, Joao M.X. N. Teixeira, *GRVM - UFPE, Brazil*, Bernardo Reis, *GRVM - UFPE, Brazil*, Veronica Teichrieb, *GRVM - UFPE, Brazil*, Judith Kelner, *GRVM - UFPE, Brazil*99

Session 5.1 - FPGA Architectures for Specific Applications105

A General-Purpose Dynammmically Reconfigurable SVM, Jonas Gomes Filho, *University of São Paulo, Brazil*, Mario Raffo, *University of São Paulo, Brazil*, Marius Strum, *University of São Paulo, Brazil*, Wang Jiang Chau, *University of São Paulo, Brazil*107

FPGA Hierarchical Architecture for a Positron Emission Tomography Scanner, Daniel Sebastián Estryk, *Comisión Nacional de Energía Atómica, Argentina*, Claudio Abel Verrastro, *Comisión Nacional de Energía Atómica, Argentina*, Sebastián Marinsek, *Comisión Nacional de Energía Atómica, Argentina*, Martín Alberto Belzunce, *Comisión Nacional de Energía Atómica, Argentina*, Esteban Venialgo, *Comisión Nacional de Energía Atómica, Argentina*113

An FPGA based architecture for complex rule matching with stateful inspection of multiple TCP connections, Claudio Greco, *University of Rome “Tor Vergata”, Italy*, Enrico Nobile, *University of Rome “Tor Vergata”, Italy*, Salvatore Pontarelli, *University of Rome “Tor Vergata”, Italy*, Simone Teofili, *University of Rome “Tor Vergata”, Italy*119

Session 5.2 - Fault Tolerance, Test & Verification125

Delay Modeling for Power Noise-Aware Design in Spartan-3A FPGAs, Judit Fernandez Freijedo, *University of Vigo, Spain*, Maria D. Valdes, *University of Vigo, Spain*, Maria J. Moure, *University of Vigo, Spain*, Lucia Costas Perez, *University of Vigo, Spain*, Juan J. Rodriguez-Andina, *University of Vigo, Spain*, Jorge Semião, *University of Algarve, Portugal*, Fabian Vargas, *PUCRS, Brazil*, Isabel C. Teixeira, *INESC-ID Portugal*, J. Paulo Teixeira, *INESC-ID, Portugal*127

Ring Oscillators Used as Thermal Sensors in FPGAs: Experiments in Low Voltage, John Jairo León Franco, *Universidad Autónoma de Madrid, Spain*, Eduardo

Boemo Scalvinoni, *Universidad Autónoma de Madrid, Spain*, Encarnación Castillo, *University of Granada, Spain*, Luis Parrilla, *University of Granada, Spain*133

Poster Session139

Design and Implementation of Packet Switching Capabilities on 10GbE MAC Core, Román A. Arenas, *Universidad Nacional de Córdoba, Argentina*, Jorge M. Finochietto, *Universidad Nacional de Córdoba - CONICET, Argentina*, Leonardo M. Rocha, *Universidad Nacional de Córdoba, Argentina*141

Multiprotocol Transceiving, Formatting and Temperature Monitoring FPGA Based Unit, Ricardo de Porras Bernácer, *National Institute for Aerospace Technology (I.N.T.A.), Spain*147

Motion Detection of Vehicles Based on FPGA, Gilliano G. S. Menezes, *UFPE, Brazil*, Abel Silva-Filho, *UFPE, Brazil*151

A Reconfigurable General Framework for Pipelined Image Processing: A Color Mathematical Morphology Application, Emerson Carlos Pedrino, *Federal University of São Carlos, Brazil*, José Hiroki Saito, *Federal University São Carlos, Brazil*, Valentin Obac Roda, *São Paulo University, Brazil*,155

A Full Duplex Implementation of Internet Protocol Version 4 in a FPGA Device, Paulo César Comassetto de Aguirre, *Federal University of Santa Maria, Brazil*, Lucas Teixeira, *Federal University of Santa Maria, Brazil*, Crístian Müller, *Federal University of Santa Maria, Brazil*, Fernando Luís Herrmann, *Federal University of Santa Maria, Brazil*, Leandro Zafalon Pieper, *Federal University of Santa Maria, Brazil*, Josué de Freitas, *Federal University of Santa Maria, Brazil*, Gustavo Dessbesell, *Federal University of Santa Maria, Brazil*, João Batista Martins, *Federal University of Santa Maria, Brazil*159

Using an FPGA Digital Clock Manager to Generate Sub-Nanosecond Phase Shifts for LIDAR Applications, William Gaughan, *Embry-Riddle Aeronautical University, United States*, Brian Butka, *Embry-Riddle Aeronautical University, United States*163

Implementation of Split-Radix Fast Fourier Transform on FPGA, Cynthia Watanabe, *Pontificia Universidad Católica del Perú, Peru*, Carlos Silva, *Pontificia Universidad Católica del Perú, Peru*, Joel Muñoz, *University of São Paulo, Brazil* ..167

Efficiency Evaluation and Architecture Design of SSD Unities for the H.264/AVC Standard, Gustavo Sanchez, *Universidade Federal de Pelotas, Brazil*, Felipe Sampaio, *Universidade Federal de Pelotas, Brazil*, Robson Dornelles, *Universidade Federal de Pelotas, Brazil*, Luciano Agostini, *Universidade Federal de Pelotas, Brazil*171

| | |
|---|-----|
| A Flexible Implementation of a Matrix Laurent Series-based 16-Point Fast Fourier and Hartley Transforms, Raimundo C. de Oliveira, <i>Amazon State University, Brazil</i> , Hélio M. de Oliveira, <i>Federal University of Pernambuco, Brazil</i> , Ricardo C. de Souza, <i>Federal University of Pernambuco, Brazil</i> , Edval J. P. Santos, <i>Federal University of Pernambuco, Brazil</i> | 175 |
| Implementation of a Sigmaboost-Based Ensemble of SVM in a Multiple Processor System on Chip, Danniel C. Lopes, <i>Universidade Federal Rural do Semi Arido - UFRSA, Brazil</i> , Naiyan H. C. Lima, <i>Universidade Federal do Rio Grande do Norte - UFRN, Brazil</i> , Jorge D. de Melo, <i>Universidade Federal do Rio Grande do Norte - UFRN, Brazil</i> , Adriao D. D. Neto, <i>Universidade Federal do Rio Grande do Norte - UFRN, Brazil</i> , | 179 |
| Hardware Design for Fast Intermode Decision and for Residues Generation in a Variable Block Size Motion Estimation Compliant with H.264/AVC Video Coding Standard, Roger Porto, <i>Federal University of Rio Grande do Sul, Brazil</i> , Sergio Bampi, <i>Federal University of Rio Grande do Sul, Brazil</i> , Luciano Agostini, <i>Federal University of Pelotas, Brazil</i> | 183 |
| Rec-Bench: a Tool to Create Benchmark for Reconfigurable Computers, Mahmood Fazlali, <i>Shahid Beheshti University, Iran</i> , Ali Zakerolhosseini, <i>Shahid Beheshti University, Iran</i> | 187 |
| Research and Partial Analysis of Overhead of a Partition Model for a Partially Reconfigurable Hardware in a Data-Driven Machine - ChipCflow, Francisco de Souza Junior, <i>University of São Paulo, Brazil</i> , Jorge Luiz e Silva, <i>University of São Paulo, Brazil</i> , Lucas Sanches, <i>University of São Paulo, Brazil</i> , Vitor Astolfi, <i>University of São Paulo, Brazil</i> | 191 |
| Acceleration of HMM-Based Speech Recognition System by Parallel FPGA Gaussian Calculation, Richard Veitch, <i>Queens University Belfast, Northern Ireland</i> , Louis-Marie Aubert, <i>Queens University Belfast, Northern Ireland</i> , Roger Woods, <i>Queens University Belfast, Northern Ireland</i> , Scott Fischaber, <i>Queens University Belfast, Northern Ireland</i> | 197 |
| Authors Index | 203 |