

5th International Conference on Design & Technology of Integrated Systems in Nanoscale Era

(DTIS 2010)

**Hammamet, Tunisia
23-25 March 2010**



IEEE Catalog Number: CFP1093A-PRT
ISBN: 978-1-4244-6338-1

TABLE OF CONTENTS

POSTER SESSION 1: DESIGN 1

• A 0.35 μm CMOS LC-Tank Injection-Locked Frequency Divider	1
<i>T. Chtioui, D. Ben Issa, A. Fakhfakh, M. Samet</i>	
• An Efficient Zero Length Prefix Algorithm for H.264 CAVLC Decoder on TMS320C64	6
<i>T.Damak, I.Werda, M.A. Ben Ayad, N.Masmoudi</i>	
• Low Power Architecture of Motion Estimation and Efficient Intra Prediction Based on Hardware Design for H.264	10
<i>H. Chaouch, S. Dhahri, A. Zitouni, R. Tourki</i>	
• PI-like Fuzzy Control Implementation using FPGA Technology	16
<i>A. Azzouna, A. Sakly, A. Trimeche, A. Mtibaa, M. Benrejeb</i>	
• An Embedded System for Iris Recognition	22
<i>R. Hentati, M. Bousselmi, M. Abid</i>	
• Electronic Implementation of a Speech Processing System for Auditory Prosthesis	27
<i>L. Bouafif, K. Ouni, N. Ellouze</i>	
• OFDM Modem Design and Implementation for Narrowband Powerline Communication	31
<i>S. Souissi, A. Ben Dhia, F. Tlili, Ch. Rebai</i>	

ISD-1: ANALOG, MIXED SIGNAL AND RF SYSTEMS

• Application of the PSO Technique to the Optimization of CMOS Operational Transconductance Amplifiers	35
<i>S. Bennour, A. Sallem, M. Kotti, E. Gaddour, M. Fakhfakh, M. Loulou</i>	

ISTC-1: DEVICE MODELING, FAILURE ANALYSIS AND RELIABILITY ISSUES

• Surface- Potential- Based Model to Study the Subthreshold Swing Behavior Including Hot-Carrier Effect for Nanoscale GASGAA MOSFETs	40
<i>D. Faycal, A. Djemai, A. M. Amir, B. Toufik</i>	
• A Delay Locked Loop for Fine Time Base Generation in a Positron Emission Tomography Scanner	44
<i>Mouad Abidi, Konin Koua Calliste, Moez Kanoun, S. Panier, L. Arpin, M. A. Tétraul, J. F. Pratte, R. Fontaine</i>	
• An Analytical Subthreshold Swing Model to Study the Scalability Limits of Doublegate MOSFETs Including Bulk Traps Effects	48
<i>M.A. Abdi, F.Djeffal, T. Bendib and D. Arar</i>	
• Computing Symbolic Transfer Functions of CC-based Circuits Using Coates Flow-Graph	54
<i>M. Fakhfakh, M. Pierzchala</i>	
• Using Low Frequency Noise Method to Characterize an AlGaAs/GaAs High Electron Mobility Heterostructure	58
<i>S. Mouetsi, A. El Hdiy</i>	
• Trends and Challenges of SRAM Reliability in the Nano-scale Era	62
<i>S. Khan, S. Hamdioui</i>	
• Reliability Considerations in Dynamic Voltage and Frequency Scheduling Schemes	68
<i>F. Firouzi, E. Salehi, F. Wang, A. Azarpayvand, M. Fakhraie</i>	

SPECIAL SESSION-1: NEURAL-INSPIRED LEARNING WITH NANO-COMPONENTS: FROM MODELING TO APPLICATIONS

• Optically-Gated CNTFET Compact Model Including Source and Drain Schottky Barrier	72
<i>S. Liao, M. Najari, C. Maneux, S. Fregonese, T. Zimmer, H. Mnif, N. Masmoudi</i>	

SPECIAL SESSION-2: SOC DESIGN FOR EMBEDDED CONTROL APPLICATIONS

• A Real-time FPGA-Based Implementation of Target Detection Technique in Non Homogenous Environment	76
<i>R. Djemal</i>	
• Electrical Simulation of Learning Stage in OG-CNTFET Based Neural Crossbar.....	82
<i>J-M. Retrouvey, J.O. Klein, S. Liao, C. Maneux</i>	
• Modelling of Sigma-delta Converters in Systemc for the Electromechanical Systems Control.....	87
<i>R. Saidia, S. Ben Saoud</i>	
• Hight Fault Tolerance in Neural Crossbar.....	94
<i>D. Chabi, J.O. Klein</i>	
• Model Checking Optimization of Safe Control Embedded Components with Refinement	100
<i>A. Gharbi, M. Khalgui, S. Ben Ahmed</i>	
• Neuro-inspired Learning of Low-level Image Processing Tasks for Implementation Based on Nano-devices.....	106
<i>O. Brousse, M. Paindavoine, C. Gamrat</i>	
• High Level Synthesis of Real Time Embedded Emulating System for Motor Controller	110
<i>A. Ben Achballah, S. Ben Othman, S. Ben</i>	

POSTER SESSION 2: DESIGN-11

• Design Optimization in SOI-based High Sensitivity Piezoresistive Cantilever Devices.....	116
<i>Y. Kebabti, M. Boujharhe</i>	
• FPGA Implementation of Vector Directional Distance Filter	121
<i>A. Boudabous, A. Ben Attallah, L. Khriji, P. Kadionik, N. Masmoudi</i>	
• Statistical Modeling for Dysphonic Classification	125
<i>A. Ghelis, M. Guerti, C. Fredouille</i>	
• Performance of Low-Pass Filter based on Non-Uniform Capacitor Sections	129
<i>I. Ouériemi, F. Choubani, I. Huynen, J.P. Raskin</i>	
• Evaluation of Speaker Identification System Using GSMEFR Speech Data.....	134
<i>A. Krobba, M. Debyache, A. Amrouche</i>	
• Design Implementation on FPGA of H.264/AVC Intra Decision Frame	139
<i>H. Loukil, A. Ben Attallah, P. Kadionik, N. Masmoudi</i>	
• GIC: A CAD Tool for IP Integration in SoC Design	143
<i>F. Abbes, N. Benamor, M. Abid, A. Yanguy</i>	

ISD-2: EMBEDDED SYSTEMS AND INNOVATIVE TECHNOLOGIES

• Evaluation Of FIR Filters Implementations For Low Power Multistandard Receivers	147
<i>N. Khouja, K. Grati, A. Ghazel, B. Le</i>	

ISTC-2: MATERIAL CHARACTERIZATION, NEW COMPONENTS AND PROCESS TECHNOLOGY

• Investigation of Deep Levels in AlGaN/GaN HEMTs on Silicon Substrate by Conductance Deep Level Transient Spectroscopy	152
<i>H. Mosbahi, M. Gassoumi, M. Charfeddine, C. Gaquiere, M.A. Zaidi, H. Maaref</i>	
• Techniques for Electromagnetic Attacks Enhancement	155
<i>Y. Souissi, J. Danger, S. Mekki, S. Guillye, M. Nassar</i>	
• RESURF nLDMOSFET in 0.35µm BiCMOS Technology-Characterization and Modeling	161
<i>M.A. Ibrahim, C. Gontrand, A. Zekry</i>	
• Design and FPGA Implementation of Modular Multiplication Methods Using Cellular Automata	166
<i>Z. Guitouni, R. Chotin-Avot, M. Machhout, H. Mehrez, R. Tourki</i>	
• Dopant Free Multi-Gate Silicon Nanowire CMOS-Inverter on SOI Substrate	171
<i>F. Wessely, T. Kraus, R. Endres, U. Schwalke</i>	
• RF MEMS Fluidic Variable Inductor	174
<i>I. El Gmati, R. Fulcrand, P. Calmon, A. Boukabache, P. Pons, H. Boussetta, A. Kallala, K. Besbes</i>	
• a New Geometric Approach to Mobile Position in Wireless LAN Reducing Complex Computations.....	177
<i>M. Zaidi, R. Tourki, R. Ouni</i>	

• Comparing Crossbar-based nano/CMOS Architectures	184
<i>C.Teodorov</i>	

ISD-3: LOW VOLTAGE AND LOW POWER SYSTEMS

• Temperature and Supply Voltage Aware Power Modeling of Analog Functions at System Level.....	190
<i>A.Suissa, O. Romain, J. Denoulet, K. Hachicha, P. Garda</i>	

ISTS-1: TESTING

• Evaluation of RF PA Nonlinearities Based on Cross-correlation Between Current and Output Voltage.....	196
<i>P. Mota, J. M. da Silva, R. Veiga</i>	
• A Mixed Style Architecture for Low Power Multipliers Based on a Bypass Technique	202
<i>G. Economakos, D. Bekiaris, K. Pekmestzi</i>	
• A Method of Unsensitizable Path Identification using High Level Design Information.....	208
<i>S. Ohtake, N. Ikeda, M. Inoue, H. Fujiwara</i>	
• Design of a Low Power 12-Bit ADC.....	214
<i>N. Gueddah, K. Abbes, M. Masmoudi</i>	
• A BIST Architecture for Sigma Delta ADC Testing Based on Embedded NOEB Self-Test and CORDIC Algorithm	221
<i>N. Chouba, L. Bouzaida</i>	
• A Concurrent BIST architecture based on Monitoring Square Windows	228
<i>I. Voyatzis, Th. Hanriotakis, C. Efstathiou, H. Antonopoulou</i>	

SPECIAL SESSION-3: RECONFIGURABLE RADIO SYSTEMS

• Reconfigurable OFDM- MIMO Architecture for 4G Wireless Systems.....	234
<i>Y. Mlayeh, F. Rouissi, F. Tlili, A. Ghazel</i>	

ISD-4: SIMULATION, VALIDATION AND VERIFICATION

• Impact of Inductance and Routing Orientation on Timing Performances of Coupled Interconnect Lines.....	238
<i>D. Deschacht</i>	
• On the Embedded Vector RF Measurements in Frequency Agile and Reconfigurable Front-Ends.....	243
<i>A. B. Kouki, I. Masri, F. Gagnon and C. Thibeault</i>	
• Verification of SystemC Transaction Level Models using an Aspect-Oriented and Generic Approach.....	248
<i>M. Kallel, Y. Lahbib, A. Baganne, R. Tourki</i>	
• RF-MEMS Switchable Inductors for Tunable Bandwidth BAW Filters.....	254
<i>S. Aliouane, A. B. Kouki, R. Aigner</i>	
• High Level Optimization of a MSK Modulator Using Hoke_D4 Experimental Design	260
<i>S. Sahouni, A. Fakhfakh, N. Masmoudi, H. Levi</i>	
• Energy Efficiency in Dynamically Reconfigurable SoC for Data-parallel Applications	264
<i>X. Zhang, A. Nafkha and P. Leray,</i>	

POSTER SESSION 3: TECHNOLOGY AND TESTING

• Optical Properties of $B_xIn_yGa_{1-x-y}As/GaAs$ grown by Metal Organic Chemical Vapor Deposition for Solar cell	269
<i>R. Hamila, F. Saidi, H. Maaref, Ph. Rodriguez, L. Auvray, Y. Monteil</i>	
• A New PSO-based Approach to Study the Nanoscale DG MOSFETs	273
<i>T. Bendib, F. Djeffal, A. Benhaya</i>	
• A New Built-In Self-Test (BIST) for a RF Low-Noise Amplifier (LNA).....	278
<i>R. Ayadi, M. Masmoudi</i>	
• Non Volatile Memory Signatures Extraction for Defects Diagnosis Purpose.....	283
<i>H. Aziza, J. Plantier, J.-M. Portal</i>	

- **Data Acquisition Test Platform for Non Uniformly Controlled ADC** 288
A.Maalej, M. Ben-Romdhane, P. Desgrey, P. Loumeau, Ch. Rebai, A. Ghazel

ISD-5: MULTIPROCESSOR SYSTEMS AND NETWORK ON CHIP

- **A Statistical Application Model for Fast MPSoC Simulation** 292
E. Azarkhish, O. Fatemi

ISD-6: SOC, SIP DESIGN AND WIRELESS SYSTEMS

- **Modeling SW to HW Task Migration for MPSOC Performance Analysis** 298
I.Benouar, D. Sebai, A. Jemai
- **An MDE Approach for Modeling Network on Chip Topologies** 304
M. Elhaji, P. Boulet, S. Meftali, A. Zitouni, J. Dekeyser, R. Tourki
- **A Timing Constraints Control Technique for Embedded Real Time Systems** 310
M. Ben Saïd, K. Loukil, N. Ben Amor, M. Abid, J. P. Diguet
- **Multiple Communication-Domains Design in FPGA-Based Systems-on-Chip** 316
M. D. Santambrogio, V. Rana, D. Sciuto, S. Corbetta
- **Concentric Circular Array for DOAs Estimation of Coherent Sources with ESPRIT Algorithm** 322
S.Akkar, F. Harabi, A.Gharsallah
- **Energy/Throughput Trade-off in a Fully Asynchronous NoC for GALSBased MPSoC Architectures** 328
A. Rahimi, M. E. Salehi, S. Mohammadi, S. M. Fahraie, A. Azarpeyvand
- **Adaptive Image Transfer for Wireless Sensor Networks (WSNs)** 334
M. Nasri, A. Helali, H. Sghaier, H. Maaref
- **Design and Implementation of Network Interface Compatible OCP For Packet Based NOC** 341
B. Attia, A. zitouni, R. tourki
- **A Behavioural Study of Nodes to Conserve Energy in Wireless Sensor Networks** 349
W.Charfi, M. Masmoudi, W. Ferchichi, F. Derbel

Author Index