

2010 International Symposium on VLSI Design, Automation and Test

(VLSI-DAT 2010)

Hsin Chu, Taiwan
26-29 April 2010



IEEE Catalog Number: CFP10847-PRT
ISBN: 978-1-4244-5269-9

TABLE of CONTENT

PLENARY SESSION

K1 The Exascale Challenge	
Shekhar Y. Borkar.....	2
K2 The Changing Role of Test in Semiconductor Manufacturing	
Kenneth M. Butler.....	4
K3 Moore's Law in the Era of GPU Computing	
Chien-Ping Lu	5

Joint Session: 3D IC (All Invited)

TJ1 Thermo-Mechanical Stress Characterization of Tungsten-Fill Through-Silicon-Via	
Thuy Dao, Dina H. Triyoso, Rode Mora, Tom Kropewnicki, Brian Griesbach, Doug Booker, Mike Petras, and Vance Adams.....	7
TJ2 3D Integration Technology for Energy Efficient System Design	
Shekhar Borkar	11
TJ3 Verifying Thermal/Thermo-mechanical behavior of a 3D stack – Challenges and Solutions	
Paul Marcha, Geert Van der Plas, Paresh Limaye, Abdelkarim Mercha, Vladimir Cherman, Herman O'Prins, Riet Labie, Bart Vandevelde, Youssef Travaly, and Eric Beyne	15
TJ4 Via Mid Through Silicon Vias – The Manufacturability Outlook	
Sitaram Arkalgud.....	17
TJ5 ThruChip Interface for 3D System Integration	
Tadahiro Kuroda.....	19

Industry Session I: System-level Design

IS11 Real-Time Hierarchical Bus System with Static Arbitration Using Timer-Controlled Priority Allocator for a Multi-Media SoC	
Ryohei Higuchi, Eiichi Teraoka, and Motoki Higashida	21
IS12 Exploring Parallelism during Processor Design Space Exploration	
Anupam Chattopadhyay, Yan Jia, D David Kammler Rainer Leupers, Gerd Ascheid, and Heinrich Meyr	25
IS13 A-Configurable SystemC Virtual Platform for Early Software Development and its Sub-system for Hardware Verification	
Yong-Hua Bu, Zhen-Zhong Tao, and Ming-Ju Lei, Ching-Tung Wu, and Chi-Feng Wu.....	29
IS14 Platform-Based Design Automation-Platform Core Complier	
Ya-Hui Tung, Hung-Cheng Lo, Vince Lo, and Sheng-Jer Kuo	33

Industry Session II: Advanced IP Design

IS21 Efficient LDPC Decoder Implementation for DVB-S2 System

Chung-Jin Tsai and Mu-Chung Chen 37

IS22 Design of a Digital Power IC

Wei-Hsu Chang and Liang-Pin Tai 41

IS23 A Novel Dynamic Over-Drive Scheme for LCD with Dynamic Driving Gamma Curves

Linkai Bu and Shing-Chia Chen 45

IS24 Digitally-Assisted Analog Designs for Submicron CMOS Technology

Fang-shi Lai, Yung-Fu Lin, Adams Weng, Kevin Hsueh, and Fu-Lung Hsueh 49

Session W1: Wireless Biosensor Interfaces

W11 A 400-MHz Super-Regenerative Receiver with a Fast Digital Frequency Calibration

Hui-Hsien Liu, Ching-Jen Tung, Yao-Hong Liu, and Tsung-Hsien Lin 54

W12 Fully Integrated Self-Quenched Super-Regenerative Impulse-FM-UWB Transceiver for WBAN

M. Anis, M. Ortmanns, and N. When 58

W13 Design Challenges for Sense Amplifier and Wireless Link in High-Density Neural Recording Implants.

Mohamed N. Elzeftawi, C. Patrick Yue, and Luke Theogarajan 61

Session W2: Digital Circuits Design

W21 A Wide-Range All-Digital Delay-Locked Loop in 65nm CMOS Technolo

Ching-Che Chung and Chia-Lin Chang 66

W22 Energy Efficient Bootstrapped CMOS Large RC-Load Driver Circuit for Ultra Low-Voltage VLSI

Chien-Yu Lu and Ching-Te Chuang 70

W23 Low-Power FinFET Design Schemes for NOR Address Decoders

Michael A. Turi, José G. Delgado-Frias, and Niraj K. Jha 74

W24 A Low Voltage and Process Variation Tolerant SRAM Cell in 90-nm CMOS

Ali Fazli Yeknami, Martin Hansson, Behzad Mesgarzadeh, and Atila Alvandpour 78

Session W3: Next-Generation Wireless Circuits and Systems

W31 A 65nm CMOS Dual-Band RF Receiver Front-End for DVB-H

Yi-Shing Shih and Ming-Ching Kuo 83

W32 A Wide-locking Range Divide-by-2 LC-tank Injection-Locked Frequency Divider

Sheng-Lyang Jang, Senior Member, IEEE, Cheng-Chen Liu, Ying-Hsiang Liao, and Ren-Kai Yang 87

W33 A 56μW VGA with 5MHz Bandwidth and 47dB Gain-Range in 90nm CMOS

Cui Zhou, Pieter Harpe, Simonetta Rampu, Xiaoyan Wang, Stefano D'Amico, Andrea Baschirotto, Kathleen Philips, Guido Dolmans, and Harmke de Groot 91

W34 Design and Implementation of a Passive UHF RFID-Based Real Time Location System

Ting-wen Xiong, Jun-juan Liu, Yu-qing Yang, Xi Tan, and Hao Min 95

Session W4: Design for Test**W41 Improving Testing and Diagnosis Efficiency for Regular Memory Arrays**

Tsung-Yu Wu, Po-Yuan Chen, Cheng-Wen Wu, and Ding-Ming Kwai 100

W42 Yield-Enhancement Techniques for 3D Random Access Memories

Che-Wei Chou, Yu-Jen Huang, and Jin-Fu Li 104

W43 A Nonlinear PRNG Using Digitized Logistic Map with Self-Reseeding Method

Chung-Yi Li, Tsin-Yuan Chang, and Chien-Chih Huang 108

W44 ATE Assisted Test Response Compaction

J J. M. Howard, S. M. Reddy, and I. Pomeranz 112

Special Session I: Emerging and Portable Medical Electronics**SS11 Circuit Techniques for Wireless Bioelectrical Interfaces (Invited Paper)**

M. Nagaraju, J. Silver, F. Zhang, Y. Liao, J. Pandey, T. Morrison, A. Mishra and D. Yeager, B. Otis 117

SS12 Silicon RF NMR Biomolecular Sensor — Review (Invited Paper)

Nan Sun, Yong Liu, Hakho Lee, Ralph Weissleder, and Donhee Ham 121

Special Session II: MEMS and Circuits**SS21 MEMS Packaging Technologies & Applications (Invited Paper)**

Jiyoung Chang and Liwei Lin 126

SS22 Interface Electronics for MEMS-Based Wireless Sensing Applications (Invited Paper)

Darrin J. Young 130

Session W5: SoC Architecture Analysis & Simulation**W51 Traffic-Thermal Mutual-Coupling Co-Simulation Platform for Three-Dimensional Network-on-Chip**

Kai-Yuan Jheng, Chih-Hao Chao, Hao-Yu Wang, and An-Yeu Wu 135

W52 Cache-Aware Task Scheduling on Multi-Core Architecture

Teng-Feng Yang, Chung-Hsiang Lin, and Chia-Lin Yang 139

W53 Implementation of JVM Tool Interface on Dalvik Virtual Machine

Chien-Wei Chang, Chun-Yu Lin, Chung-Ta King, Yi-Fan Chung, and Shau-Yin Tseng 143

W54 Conditional Threshold Wear-leveling Algorithm for Multi-channel NAND Flash Memory

Wen-Kai Hsieh and Hsi-Pin Ma 147

Session W6: Digital IP Design**W61 A Fast Ranking-based Method for Intra Mode Decision in H.264/AVC Encoder**

Chung-Fu Lin 152

W62 A Variable-Length FFT Processor for 4×4 MIMO-OFDM Systems

Chian-Chang Hung, Po-Lin Chiu, and Yuan-Hao Huang 156

W63 High-Performance NAND Flash Controller Exploiting Parallel Out-of-Order Command Execution

Yu-Hsiang Kao and Juinn-Dar Huang 160

W64 Randomness Enhancement for a Digitalized Modified-Logistic Map Based Pseudo Random Number**Generator**

Shih-Liang Chen, TingTing Hwang, and Wen-Wei Lin 164

Session W7: Logic and Architecture Level Synthesis**W71 Performance-Driven Architectural Synthesis for Distributed Register-File Microarchitecture****Considering Inter-Island Delay**

Juinn-Dar Huang, Chia-I Chen, Wan-Ling Hsu, Yen-Ting Lin, and Jing-Yang Jou 169

W72 An Efficient Hybrid LUT/SOP Reconfigurable Architecture

Ping-Chuan Lu, Po-Yang Hsu, and Yi-Yu Liu 173

W73 Dangling-wire Avoidance Routing for Crossbar Switch Structured ASIC Design Style

Yi-Huang Hung, Hung-Yi Li, Po-Yang Hsu, and Yi-Yu Liu 177

W74 Reachability Analysis of Sequential Circuits

Jung-Tai Tsai, Chun-Yao Wang, and Kuang-Jung Chang 181

Session W8: CMOS Analog-to-Digital Converters**W81 An Integrating Analog-to-Digital Data Converter with Variable Resolution**

I-Hsin Wang and Shen-Iuan Liu 186

W82 A 10-bit Pipelined A/D Converter with Split Calibration and Opamp-Sharing Technique

Li-Han Hung, Yen-Chuan Huang, and Tai-Cheng Lee 190

W83 A 1V 663µW 15-bit Audio ΔΣ Modulator in 0.18µm CMOS

Liyuan Liu, Dongmei Li, Liangdong Chen, Chun Zhang, Shaojun Wei, and Zhihua Wang 194

W84 A 0.6-V Delta-Sigma ADC with 57-dB Dynamic Range

Chun-Hao Wei and Liang-Hung Lu 198

Session T1: SoC Embedded Hardware Design**T11 Inter and Intra Kernel Reuse Analysis Driven Pipelining on Chip-Multiprocessors**

Luis Angel D. Bathen, Yongjin Ahn, and Nikil D. Dutt 203

T12 Run-Time Reconfiguration of Expandable Cache for Embedded Systems

Ang-Chih Hsieh and TingTing Hwang 207

T13 Design of On-Chip Bus with OCP Interface

Chin-Yao Chang, Yi-Jiun Chang, Kuen-Jong Lee, Jen-Chieh Yeh, Shih-Yin Lin, and Jui-Liang Ma 211

T14 A BU-Based Rate Control Design for H.264 and AVS Video Coding with ROI Support

Ping-Tsung Wu, Tzu-Chun Chang, Ching-Lung Su, and Jiun-In Guo 215

Session T2: Performance Testing**T21 Predicting Multi-core System Fmax by Data-learning Methodology**

Janine Chen, Jing Zeng, Li-C. Wang, Michael Mateja, and Jeff Rearick 220

T22 Diagnostic Test Generation for Small Delay Defect Diagnosis

Ruiqing Guo, Wu-Tung Cheng, Takeo Kobayashi, and Kun-Han Tsai 224

T23 A Robust Linear Triangle Wave Generator for ADC Testing

Chun Wei Lin and Yi-Cang Wu 228

T24 Self-Calibrate Two-Step Digital Setup/Hold Time Measurement

Luo Zhihong, Zhang Yihao, and Henry Law 232

Session T3: High Speed Mixed-signal Circuits**T31 A 1.25GHz Fast-Locked All-Digital Phase-Locked Loop with Supply Noise Suppression**

Chao-Ching Hung, I-Fong Chen, and Shen-Iuan Liu 237

T32 Layout Optimization on ESD Diodes for Giga-Hz RF and High-Speed I/O Circuits

Chih-Ting Yeh, Yung-Chih Liang, and Ming-Dou Ker 241

T33 A 35.56GHz All-Digital Phase-Locked Loop with High Resolution Varactors

Chao-Ching Hung and Shen-Iuan Liu 245

T34 Energy-Efficient, Decision Feedback Equalization Using SAR-Like Capacitive Charge Summation

Tao Jiang and Patrick Chiang 249

Session T4: Low-power Design**T41 150mV Sub-Threshold Asynchronous Multiplier for Low-Power Sensor Applications**

Joseph Crop, Scott Fairbanks, Robert Pawlowski, and Patrick Chiang 254

T42 A Mixed Style Multiplier Architecture for Low Dynamic and Leakage Power Dissipation

Dimitris Bekiaris, George Economakos, and Kiamal Pekmestzi 258

T43 Optimum Leakage Dynamic Array Design

Maciej Bajkowski, Giao Pham, and Murali Vepadharalingam 262

T44 Compact Precharging-Transistor-Less Dynamic Circuits For High Noise-Immunity Applications

Chung-Hsun Huang, Tzung-Lin Wu, and Yi-Ming Wang 266

Session T5: Physical Design for Emerging Technologies**T51 Placement of Temperature Sensors Under Process Variations**

Hsien-Te Chen, Wei-Hein Lo, Chieh-Chun Chang, and TingTing Hwang 271

T52 DNA Microarray Placement for Improved Performance and Reliability

Anurag Kumar, Minsik Cho, and David Z. Pan 275

T53 A Temperature-Aware Global Router	Yu-Ting Lee, Yen-Jung Chang, and Ting-Chi Wang	279
T54 Provably All-Convex Optimal Minimum-Error Convex Fitting Algorithm Using Linear Programming	Tsung-Yu Li, Jason Hsieh-Chie Chang, Shih-Pin Hung, and Charlie Chung-Ping Chen.....	283

Session T6: Electronics for Emerging Applications

T61 A One-time Implantable Wireless Power Bidirectional Transmission Spinal Cord Stimulation System	Chua-Chin Wang, Chia-Hao Hsu, Shao-Bin Tseng, and Doron Shmilovitz.....	288
T62 A 0.5mW high dynamic range fast CMOS charge preamplifier	Munir A. Abdalla, Francesco Cannillo, Patrick Merken, and Chris Van Hoof	292
T63 A 1-V Low-Noise Readout Front-End for Biomedical Applications in 0.18-μm CMOS	Chien-Jung Chou, Bing-Jye Kuo, Li-Guang Chen, Po-Yun Hsiao, and Tsung-Hsien Lin	295
T64 A 0.35-1 V 0.2-3 GS/s 4-bit Low-Power Flash ADC for a Solar-Powered Wireless Module	Ying-Zu Lin, Yu-Chang Lien, and Soon-Jyh Chang.....	299

Poster Session

PS 1 Design and Implementation of a FPGA Chip FDP3P7	Fang Wu, Jian Wang, Jinmei Lai, and Liyun Wang	304
PS 2 A Semi-Digital Cascaded CDR with Fast Phase Acquisition and Adaptive Resolution Control	Xueyi Yu, Jian Qiao, Woogeun Rhee, Joon-Young Park, Kyongsu Lee, and Zhihua Wang	307
PS 3 A Low-Area and Short-Time Scan-Based Embedded Delay Measurement Using Signature Registers	Kentaroh Katoh, Kazuteru Namba, and Hideo Ito.....	311
PS 4 A High Performance Binary to BCD Converter for Decimal Multiplication	JJairaj Bhattacharya, Aman Gupta, and Anshul Singh	315
PS 5 A 3-5-GHz LNA and Mixer for an UWB RF Front-end	Xiaoyan Wang, King-Wah Wong, M. Annamalai Arasu, and Wei Khuen Chan.....	319
PS 6 Modelling Stuck-at Faults in Combinational Circuits with Generalized Stochastic Petri Nets	Arthur Liraneto Torres Costa and Lirida Alves de Barros Naviner	323
PS 7 An 8-bit LCD Source Driver with Push- Pull Low - Power Output Buffer Amplifiers	Jia-Hui Wang, Jing-Chuan Qiu, Chien-Hung Tsai, Chin-Tien Chang, and Chen-Yu Wang	327
PS 8 A Peak-current Controlled Single-Inductor Dual-Output DC-DC Buck Converter with a Time-Multiplexing Scheme	Wei-Hsun Chang, Jia-Hui Wang, and Chien-Hung Tsai.....	331
PS 9 LP-Based Multi-Mode Multi-Corner Clock Skew Optimization	Chiao-Ling Lung, Hai-Chi Hsiao, Zi-Yi Zeng, and Shih-Chieh Chang	335

PS10 Lump Devices Mapping between Designer's Schematic and Layout Extracted Schematic in Microwave Frequency	
Hsin-Chia Lu, Heng-Jui Hsing, Shao-Hua Huang, and Yi-Long Chang	339
PS11 Quadruple Filtering Schedule for H.264/AVC Deblocking Filter	
Kuan-Hung Chen and Hsiang-Pin Chen.....	343
PS12 Using the Charge Recycling Technique for Low Power PLA Design	
Chiuan-Tai Xiao and Kai-Cheng Wei.....	347
PS13 Minimizing ECO Routing for FIB	
Yun-Ru Wu, Shu-Yi Kao, and Shih-Arn Hwang	351
PS14 A Polymer-Based Gas Sensor Array and Its Adaptive Interface Circuit	
Ching-Yi Wu and Kea-Tiong Tang	355
PS15 Low-complexity Reed-Solomon Decoder for Blu-ray Disc Applications	
Yung-Kuei Lu and Ming-Der Shieh	359
PS16 An Efficient Parallel VLSI Architecture for H.264/AVC Fractional Motion Estimation	
Zhuo Zhao and Ping Liang	363

Author Index

2010 International Symposium on VLSI Design, Automation and Test Organization