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## Panel–Clock Domain Verification Challenges

Moderator: Prab Varma–Blue Pearl Software, USA
Panelists: Iredamola Olopade–Intel; Pranav Ashar–Real Intent; Harry Foster–Mentor; and Shaker Sarwary–Atrenta

**Abstract:** The As semiconductor manufacturing technologies shift from 65 to 45nm and below, the design of increasingly complex systems on a chip (SoCs) that contain multiple interfaces, with differing frequencies, is enabled. To address concerns such as the minimization of power consumption and clock skew across large chips, the number of asynchronous clocks in SoCs is increasing rapidly. This is resulting in myriad challenges for designers, who are faced with ensuring that metastability, data loss, and data incoherency issues associated with the failure to correctly synchronize data are avoided. Issues such as hazards caused by reconvergence from independent synchronizers can cause intermittent design failure that is very difficult to debug with traditional simulation tools. As a result, such problems often escape to the field - causing expensive design re-spins. In addition, the incorrect specification of clock constraints related to false paths associated with clock domain crossings can result in critical (and costly) problems that are only found after tape-out. Recently static approaches based on structural analysis and formal techniques have been introduced commercially and are increasingly being adopted by the industry. This panel will address some of the issues involved in using these approaches and panelists will address the question of what really works well today and what challenges remain. The panel will also discuss emerging challenges related to 22nm designs, which might force some design teams doing large, high speed chips to abandon classic CDC approaches and adopt NoC design solutions. This panel will also discuss the emerging challenge of verification of purely asynchronous NoC protocols.



## Session 7: Coverage and Constraints



## Session 8: (Special)–Transaction-Level Modeling

## Session 9: Systems and Modeling



## Session 10: (Special)–Verification Challenges at ESL



## Session 11: (Special)–HW-Dependent Software Validation