

# **2008 ACM/IEEE International Symposium on Low Power Electronics and Design**

**(ISLPED 2008)**

**Bangalore, India  
11 – 13 August 2008**



**IEEE Catalog Number: CFP08LOW-PRT  
ISBN: 978-1-4244-8634-2**

# TABLE OF CONTENTS

<b>Keynote Talk: Towards a Green Electronic World: A Collaborative Approach</b> .....	1
<i>J. Ahuja</i>	
<b>Correlation Verification between Transistor Variability Model with Body Biasing and Ring Oscillation Frequency in 90nm Subthreshold Circuits</b> .....	2
<i>H. Fuketa, M. Hashimoto, Y. Mitsuyama, T. Onoye</i>	
<b>Optimal Technology Selection for Minimizing Energy and Variability in Low Voltage Applications</b> .....	8
<i>M. Seok, D. Sylvester, D. Blaauw</i>	
<b>Post-Silicon Programmed Body-Biasing Platform Suppressing Device Variability in 45 nm CMOS Technology</b> .....	14
<i>H. Suzuki, M. Kurimoto, T. Yamanaka, H. Takata, H. Makino, H. Shinohara</i>	
<b>Enhancing Beneficial Jitter Using Phase-Shifted Clock Distribution</b> .....	20
<i>D. Jiao, J. Gu, P. Jain, C.H. Kim</i>	
<b>Dynamic Virtual Ground Voltage Estimation for Power Gating</b> .....	26
<i>H. Xu, R. Vemuri, W. Jone</i>	
<b>A Mathematical Solution to Power Optimal Pipeline Design by Utilizing Soft Edge Flip-Flops</b> .....	32
<i>M. Ghasemazar, B. Amelifard, M. Pedram</i>	
<b>Power-Gating-Aware High-Level Synthesis</b> .....	38
<i>E. Choi, C. Shin, T. Kim, Y. Shin</i>	
<b>A Parallel and Randomized Algorithm for Large-Scale Discrete Dual-Vt Assignment and Continuous Gate Sizing</b> .....	44
<i>T. Wu, L. Xie, A. Davoodi</i>	
<b>Multiple Power-Gating Domain (Multi-VGND) Architecture For Improved Leakage Power Reduction</b> .....	50
<i>A. Sathanur, L. Benini, E. Macii, M. Poncino, A. Macii</i>	
<b>A Multi-Story Power Delivery Technique for 3D Integrated Circuits</b> .....	56
<i>P. Jain, T. Kim, J. Keane, C.H. Kim</i>	
<b>Energy Harvesting Photodiodes with Integrated 2D Diffractive Storage Capacitance</b> .....	62
<i>N.J. Guilar, E.G. Fong, T. Kleeburg, D.R. Yankelevich, R. Amirtharajah</i>	
<b>Reducing Wakeup Latency and Energy of MTCMOS Circuits via Keeper Insertion</b> .....	68
<i>C.J. Akl, M.A. Bayoumi</i>	
<b>Low-Power High-Accuracy Timing Systems for Efficient Duty Cycling</b> .....	73
<i>T. Schmid, J. Friedman, Z. Charbiwala, Y.H. Cho, M.B. Srivastava</i>	
<b>An Expected-Utility Based Approach to Variation Aware VLSI Optimization Under Scarce Information</b> .....	79
<i>U. Gupta, N. Ranganathan</i>	
<b>SRAM Methodology for Yield and Power Efficiency: Per-Element Selectable Supplies and Memory Reconfiguration Schemes</b> .....	85
<i>R. Kanj, R.V. Joshi, Z. Li, J.B. Kuang, H. Ngo, Y. Zhou, W. Shi, S. Nassif</i>	
<b>Row/Column Redundancy to Reduce SRAM Leakage in Presence of Random Within-Die Delay Variation</b> .....	91
<i>M. Goudarzi, T. Ishihara</i>	
<b>Reliability-centric Gate Sizing with Simultaneous Optimization of Soft Error Rate, Delay and Power</b> .....	97
<i>K. Bhattacharya, N. Ranganathan</i>	
<b>Variation-Aware Gate Sizing and Clustering for Post-Silicon Optimized Circuits</b> .....	103
<i>C. Zhuo, D. Blaauw, D. Sylvester</i>	
<b>Error-Resilient Low-Power Viterbi Decoders</b> .....	109
<i>R.A. Abdallah, N.R. Shanbhag</i>	
<b>Increasing Minimum Operating Voltage (<math>V_{DDmin}</math>) with Number of CMOS Logic Gates and Experimental Verification with up to 1Mega-Stage Ring Oscillators</b> .....	115
<i>T. Niiyama, Z. Piao, K. Ishida, M. Murakata, M. Takamiya, T. Sakurai</i>	
<b>Thermal Analysis of 8-T SRAM for Nano-Scaled Technologies</b> .....	121
<i>M. Meterelliyoz, J.P. Kulkarni, K. Roy</i>	
<b>Analyzing Static and Dynamic Write Margin for Nanometer SRAMs</b> .....	127
<i>J. Wang, S. Nalam, B.H. Calhoun</i>	
<b>Power Management Solutions for Computer Systems and Datacenters</b> .....	133
<i>K. Rajamani, C. Lefurgy, J. Rubio, H. Hanson, S. Ghiasi, T. Keller</i>	

<b>ISLPED 2008 Tutorial: Low Power Design Under Parameter Variations</b> .....	134
<i>S. Bhunia, K. Roy</i>	
<b>Power Management from Cores to Datacenters: Where are we going to get the next ten-fold improvements?</b> .....	135
<i>P. Ranganathan</i>	
<b>Caching for Bursts (C-Burst): Let Hard Disks Sleep Well and Work Energetically</b> .....	137
<i>F. Chen, X. Zhang</i>	
<b>3-Tier Dynamically Adaptive Power-Aware Motion Estimator for H.264/AVC Video Encoding</b> .....	143
<i>M. Shafique, L. Bauer, J. Henkel</i>	
<b>Energy Conservation by Adaptive Feature Loading for Mobile Content-Based Image Retrieval</b> .....	149
<i>K. Kumar, Y.I. Nimmagadda, Y. Hong, Y. Lu</i>	
<b>Extending the Lifetime of Media Recorders Constrained by Battery and Flash Memory Size</b> .....	155
<i>Y. Kim, Y. Cho, C. Chakrabarti, N.I. Cho, N. Chang</i>	
<b>Proactive Temperature Management in MPSoCs</b> .....	161
<i>A.K. Coskun, T.S. Rosing, K.C. Gross</i>	
<b>Entry Control in Network-on-Chip for Memory Power Reduction</b> .....	167
<i>D. Lee, S. Yoo, K. Choi</i>	
<b>PowerAntz: Distributed Power Sharing Strategy for Network on Chip</b> .....	173
<i>S.K. Mandal, R.N. Mahapatra</i>	
<b>Plenary Talk: System Implications of Integrated Photonics</b> .....	179
<i>N.P. Jouppi</i>	
<b>Design of Dual Threshold Voltages Asynchronous Circuits</b> .....	180
<i>B. Ghavarni, H. Pedram</i>	
<b>O<sup>2</sup>C: Occasional <u>Two-Cycle</u> Operations for Dynamic Thermal Management in High Performance In-Order Microprocessors</b> .....	184
<i>S. Ghosh, J. Choi, P. Ndai, K. Roy</i>	
<b>Low Power High Bandwidth Amplifier with RC Miller and Gain Enhanced Feedforward Compensation</b> .....	188
<i>S. Bajoria, V.K. Singh, R. Kunde, C.D. Parikh</i>	
<b>Single Stage Static Level Shifter Design for Subthreshold to I/O Voltage Conversion</b> .....	192
<i>Y. Lin, D. Sylvester</i>	
<b>Power Reduction in On-Chip Interconnection Network by Serialization</b> .....	196
<i>M. Arvind, B.S. Amrutur</i>	
<b>A Probabilistic Technique for Full-chip Leakage Estimation</b> .....	200
<i>S. Liu, Q. Qiu, Q. Wu</i>	
<b>Bus Encoding for Simultaneous Delay and Energy Optimization</b> .....	204
<i>J. Zhang, Q. Wu, Q. Qiu</i>	
<b>Frequency Planning for Multi-Core Processors Under Thermal Constraints</b> .....	208
<i>M. Kadin, S. Reda</i>	
<b>Reducing Leakage Power by Accounting for Temperature Inversion Dependence in Dual-Vt Synthesized Circuits</b> .....	212
<i>A. Calimera, E. Macii, M. Poncino, R.I. Bahar</i>	
<b>Variability of Flip-Flop Timing at Sub-Threshold Voltages</b> .....	216
<i>N. Lotze, M. Ortmanms, Y. Manoli</i>	
<b>Low Power Current Mode Receiver With Inductive Input Impedance</b> .....	220
<i>M.V. Dave, M.s. Baghini, D.K. Sharma</i>	
<b>Analytical Results for Design Space Exploration of Multi-core Processors Employing Thread Migration*</b> .....	224
<i>R. Rao, S. Vrudhula, K. Berezowski</i>	
<b>A Physical Level Study and Optimization of CAM-Based Checkpointed Register Alias Table</b> .....	228
<i>E. Safi, A. Moshovos, A. Veneris</i>	
<b>A Tutorial on Test Power</b> .....	232
<i>V.D. Agrawal</i>	
<b>Power Delivery for High Performance Microprocessors</b> .....	233
<i>S. Balasubramanian</i>	
<b>Enhancing Energy Efficiency of Processor-Based Embedded Systems through Post-Fabrication ISA Extension</b> .....	234
<i>H. Noori, F. Mehdipour, K. Inoue, K. Murakami</i>	
<b>Energy-Efficient MESI Cache Coherence with Pro-Active Snoop Filtering for Multicore Microprocessors</b> .....	240
<i>A. Patel, K. Ghose</i>	

<b>A Low Power Layered Decoding Architecture for LDPC Decoder Implementation for IEEE 802.11n LDPC Codes</b> .....	246
<i>J. Jin, C. Tsui</i>	
<b>A Secure and Low-Energy Logic Style Using Charge Recovery Approach</b> .....	252
<i>M. Khatir, A. Moradi, A. Ejlali, M.T.M. Shalmani, M. Salmasizadeh</i>	
<b>Word-Interleaved Cache: An Energy Efficient Data Cache Architecture</b> .....	258
<i>T.V. Kalyan, M. Mutyam</i>	
<b>Optimal Power and Noise Allocation for Analog and Digital Sections of a Low Power Radio Receiver</b> .....	264
<i>K.A. Sankaragomathi, M. Sahoo, S. Dwivedi, B.S. Amrutur, N. Bhat</i>	
<b>Design of Low-Power Short-Distance Opto-Electronic Transceiver Front-Ends with Scalable Supply Voltages and Frequencies</b> .....	270
<i>X. Chen, G. Wei, L. Peh</i>	
<b>On the Power Efficiency of Cascode Compensation over Miller Compensation in Two-Stage Operational Amplifiers</b> .....	276
<i>H. Aminzadeh, K. Mafinezhad</i>	
<b>A 1-V Piecewise Curvature-corrected CMOS Bandgap Reference</b> .....	281
<i>J. Li, Y. Fu, Y. Wang</i>	
<b>A 1.8/2.4-GHz Dual-band CMOS Low Noise Amplifier Using Miller Capacitance Tuning</b> .....	286
<i>D. Balemarthy, R. Paily</i>	
<b>Innovations to Extend CMOS Nano-transistors to the Limit</b> .....	292
<i>T. Ghani</i>	
<b>PANEL: Penalty For Power Reduction – Performance or Schedule or Yield?</b> .....	293
<i>B. Sarker, A. Dutta, J. Lahiri, R. Nair, J. Ahuja, K. Sridhar, D. Srinath</i>	
<b>Invited Talk: SOC Designs in the Energy Conscious Era</b> .....	295
<i>S. Jadcherta</i>	
<b>Clock Gating for Power Optimization in ASIC Design Cycle Theory &amp; Practice</b> .....	296
<i>S. Jairam, M. Rao, J. Srinivas, P. Vishwanath, H. Udayakumar, J. Rao</i>	
<b>Simultaneous Optimization of Battery-Aware Voltage Regulator Scheduling with Dynamic Voltage and Frequency Scaling</b> .....	297
<i>Y. Cho, Y. Kim, Y. Joo, K. Lee, N. Chang</i>	
<b>Expected System Energy Consumption Minimization in Leakage-Aware DVS Systems</b> .....	303
<i>J. Chen, L. Thiele</i>	
<b>Hybrid Dynamic Thermal Management Based on Statistical Characteristics of Multimedia Applications</b> .....	309
<i>I. Yeo, E.J. Kim</i>	
<b>Plenary Talk: Advances in Low-Power Verification</b> .....	315
<i>J. Bergeron</i>	
<b>A Framework for Energy Consumption Based Design Space Exploration for Wireless Sensor Nodes</b> .....	316
<i>S. Chouhan, M. Balakrishnan, R. Bose</i>	
<b>Full-System Chip Multiprocessor Power Evaluations Using FPGA-Based Emulation</b> .....	322
<i>A. Bhattacharjee, G. Contreras, M. Maronosi</i>	
<b>Noninvasive Leakage Power Tomography of Integrated Circuits by Compressive Sensing</b> .....	328
<i>D. Shamsi, P. Boufounos, F. Koushanfar</i>	
<b>Low Power Chips: A Fabless ASIC Perspective</b> .....	334
<i>S. Bhonge, V. Boppana</i>	
<b>On Leakage Currents: Sources and Reduction for Transistors, Gates, Memories and Digital Systems</b> .....	335
<i>W. Nebel, D. Helms</i>	
<b>Impact of Dynamic Voltage Frequency Scaling on the Architectural Vulnerability of GALS Architectures</b> .....	336
<i>N. Soundararajan, N. Vijaykrishnan, A. Sivasubramaniam</i>	
<b>Instruction-Driven Clock Scheduling with Glitch Mitigation</b> .....	342
<i>G. Wei, D. Brooks, A.D. Khan, X. Liang</i>	
<b>Thread Fusion</b> .....	348
<i>J. Gonzalez, Q. Cai, P. Chaparro, G. Magklis, R. Rakvic, A. Gonzalez</i>	
<b>Power-Efficient Clustering via Incomplete Bypassing</b> .....	354
<i>E.P. Villasenor, D. Seo, M.S. Thottethodi</i>	
<b>Lazy Instruction Scheduling: Keeping Performance, Reducing Power</b> .....	360
<i>A. Mahjur, M. Taghizadeh, A.H. Jahangir</i>	
<b>Plenary Talk: On the Rules of Low-Power Design (and How to Break Them)</b> .....	366
<i>T.M. Austin</i>	
<b>Plenary Talk: Next-Generation Power-Aware Design</b> .....	367
<i>T. Sakurai</i>	
<b>Author Index</b>	