2010 Device Research Conference

(DRC 2010)

Notre Dame, Indiana, USA
21-23 June 2010

IEEE Catalog Number: CFP10DRC-PRT
ISBN: 978-1-4244-6562-0

Table of Contents

Session I. PLENARY SESSION 1-8

I.-1 8:50 AM **Microelectronics in the "More than Moore" Era**
K. D. Wise, Center for Wireless Integrated MicroSystems, The University of Michigan, Ann Arbor, Michigan, USA

I.-2 10:10 AM **Computation with Quantum Systems**
D. Wineland, NIST, Boulder, Colorado, USA

I.-3 11:10 AM **Transistors: Past, Present, Future, and Future-er**
S. Natarajan, Director, Intel Corporation, Hillsboro, Oregon, USA

Session II.A. MOSFETs and TFETs 9-30

II.A-1 1:30 PM **Tunnel Field-Effect Transistors - Status and Prospects**
A. Seabaugh University of Notre Dame, Department of Electrical Engineering, Notre Dame, Indiana, USA

II.A-2 2:10 PM **Investigation of the Scalability of Ultra Thin Body (UTB) Double Gate Tunnel FET using Physics based 2D Analytical Model**
L. Liu and S. Datta, Department of Electrical Engineering, The Pennsylvania State University, University Park, Pennsylvania, USA

II.A-3 2:30 PM **Geometry dependent Tunnel FET performance – Dilemma of electrostatics vs. quantum confinement**
Y. Lu[1,2], A. Seabaugh[1,2], P. Fay[1,2], S. J. Koester[3], S. E. Laux[4], W. Haensch[4], and S. O. Koswatta[2,4], [1]Electrical Engineering, University of Notre Dame, Notre Dame,Indiana, USA, [2]Midwest Institute for Nanoelectronics Discovery (MIND), University of Notre Dame, Notre Dame, Indiana, USA [3]Electrical Engineering, University of Minnesota, Minneapolis, Minnesota, USA, and [4]IBM T. J. Watson Research Center, Yorktown Heights, New York, USA

II.A-4 2:50 PM **Revisiting the Impact on Sub-Threshold Regions in Uniaxially-Strained FETs** (Withdrawn)
M. H. Na[1], K. Mcstay[1], and E. J. Nowak[2], [1]IBM Semiconductor Research and Development Center, Hopewell Junction, New York,USA and [2]IBM Semiconductor Research and Development Center, Essex Junction, Vermont, USA

II.A-5 3:30 PM **Work-Function Engineering in Novel High Al Composition $Al_{0.72}Ga_{0.28}N$/AlN/GaN HEMTs**
G. Li, T. Zimmermann, Y. Cao, C. Lian, X. Xing, R. Wang, P. Fay, H. Xing, and D. Jena, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

II.A-6 3:50 PM **Ultra Shallow Junctions with High Dopant Activation and GeO_2 Interfacial Layer for Gate Dielectric in Germanium MOSFETs**
G. Thareja[1], S. Chopra[2], B. Adams[2], N. Patil[1], Y.Ta[2], P. Porshnev[2], Y. Kim[2], S. Moffatt[2], D. Loftis[3], R. Brennan[3], G. Goodman[4], I. Abdelrehim[4], K. Saraswat[1] and Y. Nishi[1], [1]Electrical Engineering, Stanford University, Stanford, California, USA, [2]Applied Materials Inc, Sunnyvale, California, USA, [3]Solecon Laboratories, Reno, Nevada, USA and [4]Evans Analytical Lab, California, USA

II.A-7 4:10 PM **Achieving high-performance Ge MOS devices using high-k gate dielectrics $Ga_2O_3(Gd_2O_3)$ of sub-nm EOT**
L. K. Chu[1], R. L. Chu[1], C. A. Lin[2], T. D. Lin[1], T. H. Chiang[1], J. Kwob[3] and M. Hong[1], [1]Dept. of Mat. Sci. and Eng., [2]Dept. of Phys., Natl. Tsing Hua Univ., HsinChu, Taiwan, ROC and [3]Ctr. for Condensed Matter Sciences, Natl. Taiwan Univ., Taipei, Taiwan, ROC

II.A-8 4:30 PM **Fermi Level Unpinning of GaSb(100) using Plasma Enhanced ALD Al_2O_3 Dielectric**
A. Ali[1], H. S. Madan[1], A. P. Kirk[2], R. M. Wallace[2], D. A. Zhao[1], D. A. Mourey[1], M. Hudait[3], T. N. Jackson[1] B. R. Bennett[4], J. B. Boos[4], and S. Datta[1], [1]Penn State University, University Park, Pennsylvania, USA, [2]The University of Texas at Dallas, Richardson, Texas, USA, [3]Virginia Tech, Blacksburg, Virginia, USA, and [4]Naval Research Laboratory, Washington, District of Columbia, USA

II.A-9 4:50 PM — **All oxide field-effect transistors formed at atomic-layer-deposited $LaAlO_3/SrTiO_3$ interface**
L. Dong[1], M. Xu[1], Y. Q. Liu[2], Y. Q. Wu[1], R. Colby[1], E. A. Stach[1], R. G. Gordon[2], and P. D. Ye[1], [1]School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA and [2]Department of Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts, USA

Session II.B. **Spintronics and Magnetic Memory** 31-44

II.B-1 1:30 PM — **Electric Field Control of Spin Precession in a Spin-Injected Field Effect Transistor**
M. Johnson[1], H. C. Koo[2], J. Eom[2], S. H. Han[2] and J. Chang[2], [1]Naval Research Laboratory, Washington District of Columbia, USA and [2]Center for Spintronics Research, Korea Institute of Science and Technology, Seongbukgu, Seoul, KOREA

II.B-2 2:10 PM — **Switching Probability in All-Perpendicular Spin Valves**
D. Bedau[1], H. Liu[1], M. Klein[1], J. Z. Sun[2], J. A. Katine[3], E. E. Fullerton[4], S. Mangin[5], and A. D. Kent[1], [1]Department of Physics, New York University, New York, New York, USA, [2]IBM T. J. Watson Research Center, Yorktown Heights, New York, USA, [3]San Jose Research Center, Hitachi-GST, San Jose, California, USA, [4]CMRR, University of California, San Diego, La Jolla, California, USA, and [5]IJL, Nancy-Université, UMR CNRS 7198, Vandoeuvre , FRANCE

II.B-3 2:30 PM — **Enhanced Spin Injection into Single Layer Graphene with Atomically Smooth MgO Barrier**
W. Han, K. Pi, K. M. McCreary, Y. Li, and R. K. Kawakami, Department of Physics and Astronomy, University of California, Riverside, California, USA

II.B-4 2:50 PM — **Gate control of a spin transistor vis spin-orbit "focusing" of electron beams**
D. H. Berman and M. E. Flatté, Department of Physics, University of Iowa, Ames, Iowa, USA

II.B-5 3:30 PM — **All-Spin Logic**
B. Behin-Aein[1,2] and S. Datta[1,2], [1]Department of Electrical and Computer Engineering, Purdue University, W. Lafayette, Indiana, USA and [2]NSF Network for Computational Nanotechnology (NCN), Purdue University, W. Lafayette, Indiana, USA

II.B-6 4:10 PM — **Modeling and Analysis of Read (RD) Disturb in 1T-1STT MTJ Memory Bits**
A. Raychowdhury, D. Somasekhar, T. Karnik, and V. K. De, Circuits Research Lab, Intel Corporation, Hillsboro, Oregon, USA

II.B-7 4:30 PM — **Late News**

II.B-8 4:50 PM — **Late News**

Session III. **Poster Session** 45-146

III-1 — **Great reduction of interfacial traps in Al_2O_3/GaAs (100) starting with Ga-rich surface and through systematic thermal annealing**
Y. C. Chang[1,2], C. Merckling[3], J. Penaud[4], C. Y. Lu[2], G. Brammertz[3], W.–E. Wang[3], M. Hong[1], J. Kwo[1], J. Dekoster[3], M. Caymax[3], M. Meuris[3], and M. Heyns[2,3], [1]National Tsing Hua University, Hsinchu, Taiwan, ROC, [2]Katholieke Universiteit Leuven, Leuven, BELGIUM, [3]Interuniversity Microelectronics Center (IMEC), Leuven, BELGIUM, and [4]Riber, Bezons, FRANCE

III-2 — **Tellurium δ-doped 120nm AlSb/InAs HEMTs: towards sub-100mV electronics**
Y. Roelens, A. Olivier, L. Desplanque, A. Noudeviwa, F. Danneville, N. Wichmann, X. Wallart, and S. Bollaert, IEMN, Université de Lille I, Villeneuve d'Ascq, FRANCE

III-3 — **Effects of InP barrier layer thicknesses and different ALD oxides on device performance of $In_{0.7}Ga_{0.3}As$ MOSFETs**
H. Zhao, N. Kong, Y.-T. Chen, Y. Wang, F. Xue, F. Zhou, S. K. Banerjee and J. C. Lee, Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas, USA

III-4 **Comparative Analysis of the Performance of InAs Lateral and Vertical Band-to-Band Tunneling Transistors**
K. Ganapathi, Y. Yoon and S. Salahuddin, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California, USA.

III-5 **Flatband Voltage Tuning and EOT Reduction for SiO_2/HfO_2/TiN Gate Stacks via Lanthanum Oxide Capping Layers using Two Different Lanthanum Precursors**
C. K. Chiang[1,3], H. Y. Huang[1], C. H. Wu[2], J. F. Lin[3], C. C. Liu[3], C. L. Yang[3], J. Y. Wu[3], and S. J. Wang[1], [1]Institute of Microelectronics, Dept. of Electrical Eng., National Cheng Kung Univ., Tainan, Taiwan, ROC, [2]Dept. of Microelectronics Eng., Chung Hua Univ., Hsinchu, Taiwan, ROC, and [3]United Microelectronics Corporation, Science-Based Industrial Park, Hsinchu, Taiwan, ROC

III-6 **Scalability Study of $In_{0.7}Ga_{0.3}As$ HEMTs for 22nm node and beyond Logic Applications**
E. Hwang[1], S. Mookerjea[1], M. K. Hudait[2] and S. Datta[1], [1]The Pennsylvania State University, University Park, Pennsylvania, USA and [2]Virginia Tech University, Blacksburg, Virgina, USA

III-7 **Factors Enhancing $In_{0.7}Ga_{0.3}As$ MOSFETs and Tunneling FETs Device performance**
H. Zhao[1], N. Goel[2], J. Huang[2], Y. Chen[1], J. Yum[1], Y. Wang[1], F. Zhou[1], F. Xue[1], and J. Lee[1], [1]Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas, USA and [2]SEMATECH, Austin, Texas, USA

III-8 **Graphene Based Heterostructure Tunnel-FETs for Low-Voltage/High-Performance ICs**
Y. Khatami, M. Krall, H. Li, C. Xu, and K. Banerjee, Department of Electrical and Computer Engineering, University of California, Santa Barbara, California, USA

III-9 **Non-Hysteretic Ferroelectric Tunnel FET with Improved Conductance at Curie Temperature**
L. Lattanzio, G. A. Salvatore, and A. M. Ionescu, Nanoelectronic Devices Laboratory (Nanolab), Ecole Polytechnique Fédérale de Lausanne, Lausanne, SWITZERLAND

III-10 **Influence of Temperature on High Frequency Performance of Graphene Nano Ribbon Field Effect Transistor**
N. Meng, J. F. Fernandez, D. Vignaud, G. Dambrine, and H. Happy, Institut d'Electronique, de Microélectronique et de Nanotechnologie, UMR-CNRS, Villeneuve d'Ascq, FRANCE

III-11 **Nanowire-mask based fabrication of high mobility and low noise graphene nanoribbon short-channel field-effect transistors**
G. Xu[1], J. Bai[2], C. M. Torres Jr.[1], E. B. Song[1], J. Tang[1], Y. Zhou[1], X. Duan[3], Y. Zhang[4], Y. Huang[2] and K. L. Wang[1], [1]Department of Electrical Engineering, [2]Department of Material Science and Engineering, [3]Department of Chemistry and Biochemistry, University of California at Los Angeles, Los Angeles, California, USA and [4]Molecular Foundry, Lawrence Berkeley National Laboratory, Berkeley, California, USA

III-12 **Mobility and Velocity-Field Relationship in Graphene**
V. Dorgan, M.-H. Bae, and E. Pop, Dept. of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, Illinois, USA and Micro and Nanotechnology Lab, Urbana, Illinois, USA

III-13 **Graphene Nanoribbon Schottky-barrier FETs for End-of-the-roadmap CMOS: Challenges and Opportunities**
Q. Zhang[1,2], Y. Lu[1], G. H. Xing[1], C. A. Richter[2], S. J. Koester[3], and S. O. Koswatta[4], [1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA, [2]National Institute of Standards and Technology, Semiconductor Electronics Div., Gaithersburg, Maryland, USA, [3]Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota, USA, and [4]IBM Research Division, T. J. Watson Research Center, Yorktown Heights, New York, USA

III-14 **Device Characteristics of single-layer Graphene FETs grown on Copper**
K. Tahy[1], M. J. Fleming[2], B. Raynal[1], V. Protasenko[1], S. Koswatta[3], D. Jena[1], H. Xing[1] and M. Kelly[1], [1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA and [2]Department of Chemistry, Saint Mary's College, Notre Dame, Indiana, USA

III-15 **A Computational Study on the Device Performance of Graphene Nanoribbon Heterojunction Tunneling FETs based on Bandgap Engineering**
K.-T. Lam, H. Da, S.-K. Chin, G. Samudra, Y.-C. Yeo and G. Liang, Computational Nanoelectronic and Nano-device Lab, Department of Electrical and Computer Engineering,National University of Singapore, Singapore, REPUBLIC OF SINGAPORE

III-16 **Thickness dependence of carrier mobility in mono- and bi-layer graphene with HfO_2 gate dielectric**
B. Fallahazad[1], S. Kim[1], L. Colombo[2], E. Tutuc[1], [1]Microelectronics Research Center, University of Texas at Austin, Austin, Texas, USA and [2]Texas Instruments, Inc., Dallas, Texas, USA

III-17 **Majority and Minority Carrier Mobility Behavior and Device Modeling of Doped CVD Monolayer Graphene Transistors**
O. M. Nayfeh, S. Kilpatrick, and M. Dubey, United States Army Research Laboratory, Adelphi, Maryland, USA

III-18 **Programmable Nanomagnet-Logic Majority Gate**
E. Varga[1], M. T. Niemier[2], G. H. Bernstein[1], W. Porod[1], and X. S. Hu[2], [1]Dept. of Elec. Eng. And [2]Dept. of Comp. Sci. and Eng., University of Notre Dame, Notre Dame, Indiana, USA

III-19 **Experimental Demonstration of Non-Majority, Nanomagnet Logic Gates**
E. Varga[1], M. Siddiq[1], M.T. Niemier[2], M.T. Alam[1], G.H. Bernstein[1], W. Porod[1], X.S. Hu[2], and A. Orlov[1], [1]Dept. of Elec. Eng. and [2]Dept. of Comp. Sci. and Eng., U. of Notre Dame, Notre Dame, Indiana, USA

III-20 **Nonreciprocal amplification of spin-wave signals**
M. Bao, K. Wong, A. Khitun, and K. L. Wang, Department of Electrical Engineering, University of California, Los Angeles, California, USA

III-21 **Robust path-dependent spin rotation on the nanoscale in a semiconductor quantum well**
B. J. Moehlmann and M. E. Flatté, Department of Physics and Astronomy, University of Iowa, Iowa City, Iowa, USA

III-22 **Spin Torques Estimation and Magnetization Dynamics in Dual Barrier Resonant Tunneling Penta-Layer Magnetic Tunnel Junctions**
N. N. Mojumder[1], C. Augustine[1], D. E. Nikonov[2] and K. Roy[2], [1]School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA and [2]Components Research, Intel Corporation, Santa Clara, California, USA

III-23 **Experimental Demonstration of Fanout for Nanomagnet Logic**
E. Varga[1], S. Liu[2], M. T. Niemier[2], W. Porod[1], X. S. Hu[2], G. H. Bernstein[1], and A. Orlov[1], [1]Dept. of Elec. Eng. and [2]Dept. of Comp. Sci. and Eng., U. of Notre Dame, Notre Dame, Indiana, USA

III-24 **Interface and Oxide Quality of CoFeB/MgO/Si Tunnel Junctions**
J. Shaw[1], H.-W. Tseng[2], S. Rajwade[1], L.-T. Tung[1], R. A. Buhrman[2], and E. C. Kan[1], [1]School of Electrical and Computer Engineering, Cornell University, Ithaca, New York, USA and [2]School of Applied & Engineering Physics, Cornell University, Ithaca, New York, USA.

III-25 **New Phenomena for the Lifetime Prediction of TANOS-based Charge Trap NAND Flash Memory**
J. Kim, C. Kang, S-I. Chang, J. Kim, Y. Jeong, C. Park, J-H. Kang, S-H. Kim, S. Hwang, B-I. Choe, J. Park, J. Chung, Y. Park, J. Choi and C. Chung, Semiconductor R&D Center, Samsung Electronics Co., LTD., Banwol-dong, Hwasung-City, Gyeonggi-Do, KOREA

III-26 **Low Power Loadless 4T SRAM cell based on Degenerately Doped Source (DDS) $In_{0.53}Ga_{0.47}As$ Tunnel FETs**
V. Saripalli, D. K. Mohata, S. Mookerjea, S. Datta and V. Narayanan, The Pennsylvania State University, University Park, Pennsylvania, USA

III-27 **Implications of Record Peak Current Density $In_{0.53}Ga_{0.47}As$ Esaki Tunnel Diode on Tunnel FET Logic Applications**
D. K. Mohata[1], D. Pawlik[2], L. Liu[1], S. Mookerjea[1], V. Saripalli[1], S. Rommel[2] and S. Datta[1], [1]Pennsylvania State University, University Park, Pennsylvania, USA and [2]Rochester Institute of Technology, Rochester, New York, USA

III-28 **Controlled 1.3 – 1.55 µm Coherent Emission from Microbelt-Like Optical Cavities Formed by Rolled-up InAs Quantum Dot Tubes**
F. Li[1], Z. Mia[1] and P. Poole[2], [1]Department of Electrical and Computer Engineering, McGill University, Montreal, Quebec, CANADA and [2]Institute for Microstructural Sciences, National Research Council of Canada, Ottawa, Ontario, CANADA

III-29 **Fast Response of Actuators with Self Assembly Nanoparticle Electrodes and Ionic Liquids**
S. Liu[1], Y. Liu[1], R. Montazami[3], V. Jain[4], J. R. Heflin[5], and Q. Zhang[1,2], [1]Deparment of Electrical Engineering, Penn State, University Park, Pennsylvania, USA, [2]Materials Research Institute, Penn State, University Park, Pennsylvania, USA, [3]Department of Materials Science and Engineering, Virginia Tech, Blacksburg, Virginia, USA, [4]Macromolecular Science and Engineering, Virginia Tech, Blacksburg, Virginia, USA, and [5]Department of Physics, Virginia Tech, Blacksburg, Virginia, USA

III-30 **Substrate effects on metal-oxide single electron transistors electrometer measurements**
H. C. George, A. O. Orlov, and G. L. Snider, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

III-31 **DC and flicker noise models for passivated single-walled carbon nanotube transistors**
L. Yu, S. Kim and S. Mohammadi, Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA

III-32 **CMOS Kink Effect-Induced Instability in Al/AlOx Single Electron Transistors**
A. A. Prager, H. C. George, A. O. Orlov, and G. L. Snider, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

III-33 **Room Temperature Nonlinear Ballistic Nanodevices for Logic Applications**
V. Kaushal, I. Iñiguez-de-la-Torre, and M. Margala, Department of Electrical and Computer Engineering, University of Massachusetts, Lowell, Massachusetts, USA

III-34 **Sub-THz Frequency Analysis in Nano-scale Devices at Room Temperature**
I. Iñiguez-de-la-Torre[1], V. Kaushal[1], M. Margala[1], T. González[2] and J. Mateos[2], [1]Department of Electrical and Computer Engineering, University of Massachusetts, Lowell, Massachusetts, USA and [2]Departamento de Física Aplicada, Universidad de Salamanca, Salamanca, SPAIN

III-35 **Effect of Uniaxial Tensile Strain on Electrical Performance of Amorphous IGZO TFTs and Circuits on Flexible Metal Foils**
S. A. Khan, P.-C. Kuo, A. Jamshidi-Roudbari and M. Hatalis, Department of Electrical Engineering, Lehigh University, Bethlehem, Pennsylvania, USA

III-36 **Amorphous InGaZnO Logic Gates for Transparent Electronics**
H. Luo, P. Wellenius, L. Lunardi and J. F. Muth, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina, USA

III-37 **Solution-processed zinc-tin oxide thin-film transistors with high performance and improved uniformity**
C.-G. Lee and A. Dodabalapur, Microelectronics Research Center, University of Texas at Austin, Texas, USA

III-38 **Reduced Self-heating in AlGaN/GaN HEMTs Using Nanocrystalline Diamond Heat Spreading Films**
M. J. Tadjer[1], T. J. Anderson[2], K. D. Hobart[2], T. I. Feygelson[3], M. A. Mastro[2], J. D. Caldwell[2], J. K. Hite[2], C. R. Eddy, Jr.[2], F. J. Kub[2], J. E. Butler[2], and J. Melngailis[1], [1]University of Maryland, College Park, Maryland, USA and [2]Naval Research Laboratory, Washington, District of Columbia, USA, and [3] SAIC, Inc., Washington, District of Columbia, USA

III-39 **Self-Consistent Electro-Thermal Simulation of AlGaN/GaN HEMTs for Reliability Prediction**
F. Gao[1,2], H.-Y. Lo[2], R. Ram[2], and T. Palacios[2], [1]Department of Materials Science and Engineering and [2]Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts, USA

III-40 **High Performance E-mode InAlN/GaN HEMTs: Interface States from Subthreshold Slopes**
R. Wang[1], X. Xing[1], T. Fang[1], T. Zimmermann[1], C. Lian[1], G. Li[1], P. Saunier[2], X. Gao[3], S. Guo[3], G. Snider[1], P. Fay[1], D. Jena[1], and H. Xing[1], [1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA, [2]Triquint Semiconductor, Richardson, Texas, USA, and [3]IQE RF LLC, Somerset, New Jersey, USA

III-41 **Influence of crystal orientation on the current gain in 4H-SiC BJTs**
R. Ghandi, B. Bouno, M. Domeij, S. Shayestehaminzadeh, C.-M. Zetterling and M. Östling, School of Information and Communication Technology, KTH, Royal Institute of Technology, Stockholm, SWEDEN

III-42 **Room Temperature operation and DC characteristics of InAlN/GaN/AlGaN Hot Electron Transistors with common base transfer ratio, $\alpha = 0.97$**
S. Dasgupta[1], Nidhi[1], A. Raman[1], J. S. Speck[2], and U. K. Mishra[1], [1]Department of Electrical and Computer Engineering, University of California, Santa Barbara, California, USA and [2]Materials Department, University of California, Santa Barbara, California, USA

III-43 **MOCVD grown normally-OFF type AlGaN/GaN HEMTs on 4 inch Si using p-InGaN Cap Layer with High Breakdown**
S. L. Selvaraj, K. Nagai and T. Egawa, Research Center for Nano-Device and System, Nagoya Institute of Technology, Gokiso-cho, Showa-ku, Nagoya, JAPAN

III-44 **Self-aligned Enhancement-mode AlGaN/GaN HEMTs Using 25 keV Fluorine Ion Implantation**
H. Chen, M. Wang, and K. J. Chen, Dept. of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong

III-45 **Effects of Nanoscale Contacts to Silicon Nanowires on Contact Resistance: Characterization and Modeling**
J. T. Smith[1], Y. Zhao[2], C. Yang[2,3], and J. Appenzeller[1], [1]Department of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA, [2]Department of Physics, Purdue University, West Lafayette, Indiana, USA, and [3]Department of Chemistry, Purdue University, West Lafayette, Indiana, USA

III-46 **Characterization of the Metal-Semiconductor and Metal-Insulator-Semiconductor Junctions between Single-walled Carbon Nanotube Films and Si Substrates**
A. Behnam, N. A. Radhakrishna, and A. Ural, Electrical and Computer Engineering, University of Florida, Gainesville, Florida, USA

III-47 **RF NEM Capacitive Switch Based on Dense Horizontal Arrays of CNTs**
D. Acquaviva[1], A. Arun[1], S. Esconjauregui[2], J. Cao[1], R. Smajda[3], D. Buovet[1], A. Magrez[3], L. Forro[3], J. Robertson[2] and A. M. Ionescu[1], [1]Nanolab, [2]Engineering Department, Cambridge University, Cambridge, UK, and [3]LNNME, EPFL, Lausanne, SWITZERLAND

III-48 **Ge-Si_xGe_{1-x} Core-Shell Nanowire Tunneling Field-Effect Transistors**
J. Nah, Y. Kim, E.–S. Liu, K. M. Varahramyan, S. K. Banerjee, and E. Tutuc, Microelectronics Research Center, The University of Texas, Austin, Texas, USA

Session IV.A. **High Speed Devices** 147-168

IV.A-1 8:20 **III-V FET Channel Designs for High Current Densities and Thin Inversion Layers**
M. Rodwell[1], W. Frensley[2], S. Steiger[4], E. Chagarov[3], S. Lee[4], H. Ryu[4], Y. Tan[4], G. Hegde[4], L. Wang[3], J. Law[1], T. Boykin[5], G. Klimek[4], P. Asbeck[3], and A. Kummel[3], [1]ECE Department, University of California, Santa Barbara, California, USA, [2]University of Texas, Dallas, Texas, USA, [3]University of California, San Diego, California, USA, [4]Purdue University, West Lafayette, Indiana, USA, and [5]University of Alabama, Huntsville, Alabama, USA

IV.A-2 9:00 **High performance 110 nm InGaAs/InP DHBTs in dry-etched in-situ refractory emitter contact technology**
V. Jain[1], E. Lobisser[1], A. Baraskar[1], B. J. Thibeault[1], M. Rodwell[1], Z. Griffith[2], M. Urteaga[2], S. T. Bartsch[3], D. Loubychev[4], A. Snyder[4], Y. Wu[4], J. M. Fastenau[4] and W.K. Liu[4], [1]ECE Department, University of California, Santa Barbara, California, USA, [2]Teledyne Scientific & Imaging, Thousand Oaks, California, USA, [3]Nanoelectronics Device Laboratory, Ecole Polytechnique Fédéral de Lausanne (EPFL), Lausanne SWITZERLAND, and [4]IQE Inc., Bethlehem, Pennsylvania, USA

IV.A-3
9:20 AM
T-gate technology for N-polar GaN-based self-aligned MIS-HEMTs with state-of-the-art f_{MAX} of 127 GHz: Pathway towards scaling to 30nm GaN HEMTs
Nidhi[1], S. Dasgupta[1], D. F. Brown[2], S. Keller[1], J. S. Speck[3], and U. K. Mishra[1], [1]Department of Electrical and Computer Engineering, University of California, Santa Barbara, California, USA, [2]Hughes Research Laboratories, Malibu, California, USA and [3]Materials Department, University of California, Santa Barbara, California, USA

IV.A-4
9:40 AM
Depletion-mode Pseudomorphic $In_{0.22}Ga_{0.78}As$-Channel MOSFETs with InAlP Native Oxide Gate Dielectric for RF Applications
X. Xing, W. Yuan, D. Hall and P. Fay, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

IV.A-5
10:20 AM
Vertically scaled GaN/AlN DH-HEMTs with regrown n^+GaN ohmic contacts by MBE
I. Milosavljevic, K. Shinohara, D. Regan, S. Burnham, A. Corrion, P. Hashimoto, D. Wong, M. Hu, C. Butler, A. Schmitz, P.J. Willadsen, and M. Micovic, HRL Laboratories LLC, Malibu, California, USA

IV.A-6
10:40 AM
Gated Tunnel Diode with a Reactive Bias Stabilizing Network for 60 GHz Impulse Radio Implementations
M. Egard[1], M. Ärlelid[2], E. Lind[1], and L.-E. Wernersson[2], [1]Solid State Physics and [2]Electrical and Information Technology, Lund University, Lund, SWEDEN

IV.A-7
11:00 AM
Sub-Micron InGaAs Esaki Diodes With Record High Peak Current Density
D. Pawlik[1], M. Barth[1], P. Thomas[1], S. Kurinec[1], S. Mookerjea[2], D. Mohata[2], S. Datta[2], S. Cohen[3], D. Ritter[3], S. Rommel[1], [1]Department of Electrical and Microelectronic Engineering, Rochester Institute of Technology, Rochester, New York, USA, [2]Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania, USA, and [3]Department of Electrical Engineering, Technion, Haifa, ISRAEL

IV.A-8
11:20 AM
A Quantum Ring Detector for the 1-3 Terahertz Range with Very High Responsivity and Specific Detectivity
S. Bhowmick[1], G. Huang[1], W. Guo[1], C. S. Lee[1], P. Bhattacharya[1], G. Ariyawansa[2] and A. G. U. Perera[2], [1]Solid State Electronics Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan, USA and [2]Department of Physics and Astronomy, Georgia State University, Atlanta, Georgia, USA

IV.A-9
11:40 AM
Enhanced Responsivity in a Novel AlGaN / GaN Plasmon-Resonant Terahertz Detector Using Gate-Dipole Antenna with Parasitic Elements
T. Tanigawa[1], T. Onishi[1], S. Takigawa[1] and T. Otsuji[2], [1]Semiconductor Device Research Center, Semiconductor Company, Panasonic Corporation, Nagaokakyo, Kyoto, JAPAN, and [2]Research Institute of Electrical Communication, Tohoku University, Aoba-Ku, Sendai, JAPAN

Session IV.B. **Thin Film Transistors (I) and MEMS** 169-184

IV.B-1
8:20 AM
Organic transistor technology options for device performance versus technology options for increased circuit reliability and yield on foil
J. Genoe[1,2], K. Myny[1,2,3], S. Steudel[1], S. Smout[1], P. Vicca[1], B. van der Putten[5], A. K. Tripathi[5], N. A. J. M. van Aerle[4] , G. H. Gelinck[5], W. Dehaene[3], P. Heremans[1,3], [1]IMEC, Leuven, BELGIUM, [2]KHLim, Universitaire Campus, Diepenbeek, BELGIUM, [3]ESAT, KULeuven, Leuven, BELGIUM, [4]Polymer Vision, Eindhoven, THE NETHERLANDS, and [5]TNO-Holst Centre, Eindhoven, THE NETHERLANDS

IV.B-2
9:00 AM
Top-Contact Organic Transistors and Complementary Circuits Fabricated using High-Resolution Silicon Stencil Masks
F. Ante[1], F. Letzkus[2], J. Butschke[2], U. Zschieschang[1], J. N. Burghartz[2], K. Kern[1,3], H. Klauk[1], [1]Max Planck Institute for Solid State Research, Stuttgart, GERMANY, [2]Institut für Mikroelektronik/IMS CHIPS, Stuttgart, GERMANY, and [3]Ecole Polytechnique Fédérale de Lausanne, Lausanne, SWITZERLAND

IV.B-3
9:20 AM
Low-Voltage, High-Mobility Organic Thin-Film Transistors with Improved Stability
U. Zschieschang[1], T. Yamamoto[2], K. Takimiya[2], H. Kuwabara[3], M. Ikeda[3], T. Sekitani[3], T. Someya[4] and H. Klauk[1], [1]Max Planck Institute for Solid State Research, Stuttgart, Germany, [2]Hiroshima University, Higashi-Hiroshima, JAPAN, [3]Nippon Kayaku Co., Ltd., Kita-ku, Tokyo, JAPAN, and [4]University of Tokyo, Tokyo, JAPAN

IV.B-4 9:40 AM **High retention-time nonvolatile amorphous silicon TFT memory for static active matrix OLED display without pixel refresh**
Y. Huang, B. Hekmatshoar, S. Wagner and J. C. Sturm, Princeton Institute for the Science and Technology of Materials (PRISM), Department of Elect. Eng.,Princeton University, Princeton, New Jersey, USA

IV.B-5 10:20 AM **Resonant Body Transistors**
A. M. Ionescu, Nanolab, Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, SWITZERLAND

IV.B-6 11:00 AM **Nano-Electro-Mechanical Vibrating Body FET Resonator for High Frequency Integrated Oscillators**
D. Grogg, A. Lovera and A. M. Ionescu, Nanoelectronic Devices Laboratory (NanoLab), Ecole Polytechnique Fédérale de Lausanne, SWITZERLAND

IV.B-7 11:20 AM **Late News**

IV.B-8 11:40 AM **Late News**

Session V.A **Wide Bandgap Devices** 185-202

V.A-1 1:30 PM **Recent Progress in GaN FETs on Silicon Substrate for Switching and RF Power Applications**
H. Miyamoto and H. Shimawaki, Nano Electronics Research Laboratories, NEC Corporation, Otsu, Shiga, JAPAN

V.A-2 2:10 PM **Scalable E-mode N-polar GaN MISFET devices and process with self-aligned source/drain regrowth**
U. Singisetti[1], M. H. Wong[1], Sa. Dasgupta[1], Nidhi[1], B. L. Swenson[1], B. J. Thibeault[1], J. S. Speck[2] and U. K. Mishra[1], [1]ECE and [2]Materials Departments, University of California, Santa Barbara, CA, 93106, USA

V.A-3 2:30 PM **Breakdown Mechanism in AlGaN/GaN HEMTs on Si Substrate**
B. Lu[1], E. L. Piner[2] and T. Palacios[1], [1]Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts, USA and [2]Nitronex Corporation, Durham, North Carolina, USA

V.A-4 2:50 PM **Preliminary reliability at 50 V of State-of-the-Art RF power GaN-on-Si HEMTs**
F. Medjdoub, D. Marcon, J. Das, J. Derluyn, K. Cheng, S. Degroote, M. Germain and S. Decoutere, IMEC, Leuven, BELGIUM

V.A-5 3:30 PM **4H-SiC DMOSFETs for Power Conversion Applications: Successes and Ongoing Challenges**
B. Hull, J. Zhang, M. Das, S.-H. Ryu, C. Jonas, S. Dhar, S. Haney, R. Callanan, and J. Richmond, Cree, Inc., Durham, North Carolina, USA

V.A-6 4:10 PM **Dispersion-free AlGaN/GaN CAVET with low R_{on} achieved with plasma MBE regrown channel with Mg-ion-implanted current blocking layer**
S. Chowdhury, M. H. Wong, B. L. Swenson and U. K. Mishra, Department of Electrical and Computer Engineering University of California, Santa Barbara, California, USA

V.A-7 4:30 PM **Late News**

V.A-8 4:50 PM **Late News**

Session V.B **Graphene Devices and Modeling** 203-218

V.B-1 1:30 PM
Graphene-based fast electronics and optoelectronics
Ph. Avouris, Y.-M. Lin, F. Xia, T. Mueller, D. B. Farmer, C. Dimitrakopoulos, and A. Grill, IBM T.J. Watson Research Center, Yorktown Heights, New York, USA

V.B-2 2:10 PM
Overview of DARPA Carbon Electronics for RF Applications Program (CERA)
J. Albrecht, DARPA MTO Office, Arlington, Virginia, USA

V.B-3 2:50 PM
Self-Aligned Graphene-on-SiC and Graphene-on-Si MOSFETs on 75 mm Wafers
J. S. Moon[1], D. Curtis[1], M. Hu[1], S. Bui, D. Wheeler, T. Marshall, H. Sharifi, D. Wong, D. K. Gaskill[2], P. M. Campbell[2], P. Asbeck[3], G. Jernigan[2], J. Tedesco[2], B. VanMil[2], R. Myers-Ward[2], C. Eddy, Jr.[2], X. Weng[4], J. Robinson[4], and M. Fanton[4], [1]HRL Laboratories, LLC, Malibu, California, USA, [2]Naval Research Laboratories, Washington, District of Columbia, USA , [3]University of California at San Diego, La Jolla, California, USA and [4]Electro-Optics Center, Penn State University, University Park, Pennsylvania, USA

V.B-4 3:30 PM
Modeling Demands for Nanoscale Devices
M. Pourfath, V. Sverdlov, and S. Selberherr, Institute for Microelectronics, TU Wien, Vienna, AUSTRIA

V.B-5 4:10 PM
Structure and doping effects in carbon heterojunction FETs towards barrier-free inter-band tunneling
Y. Yoon and S. Salahuddin, Electrical Engineering and Computer Sciences, University of California, Berkeley, California, USA

V.B-6 4:30 PM
Effects of Edge Chemistry Doping on Graphene Nanoribbon Mobility
Y. Ouyang[1], S. Sanvito[2] and J. Guo[1], [1]Electrical and Computer Engineering, University of Florida, Gainesville, Florida, USA and [2]Department of Physics, Trinity College, Dublin, IRELAND

V.B-7 4:50 PM
Late News

Rump Sessions 219-220

R.1 8:30 PM
Reaching the Quantum Capacitance Limit - Dead End or New Scaling Path?
Session Organizers: Zhihong Chen, IBM and Miguel Urteaga, Teledyne Scientific & Imaging

R.2 8:30 PM
Si, GaN, SiC, ... Who has the (high voltage) power?
Session Organizers: Tomás Palacios, Massachusetts Institute of Technology, Dimitris Pavlidis, Technische Universität Darmstadt, and Mikael Östling, Royal Institute of Technology (KTH)

R.3 8:30 PM
Looking for Extra Cache
Session Organizers: Suman Datta, Penn State University, Eric Pop, University of Illinois, Urbana-Champaign, and Tahir Ghani, Intel Corporation

Joint DRC/EMC Plenary Session 221-222

8:30 AM
Epitaxial Graphene: Designing a New Electronic Material
Walter A. de Heer, Georgia Institute of Technology

Session VI.A **Optoelectronics** 223-232

VI.A-1 10:00 AM
Progress in the Growth, Characterization and Device Performance for Nonpolar and Semipolar GaN-based Materials
J. S. Speck, Materials Department, University of California, Santa Barbara, California, USA

VI.A-2
10:40 AM
Polarization-Engineered N-face III-V Nitride Quantum Well LEDs
J. Verma, J. Simon, V. Protasenko, G. Xing, D. Jena, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

VI.A-3
11:00 AM
InGaN/GaN Nanowire Green Light Emitting Diodes on (001) Si Substrates
M. Zhang, W. Guo, A. Banerjee and P. Bhattacharya, Solid-State Electronics Laboratory, University of Michigan, Ann Arbor, Michigan, USA

VI.A-4
11:20 AM
Temperature Dependence of Ge/Si Avalanche Photodiodes
D. Dai[1], J. E Bowers[1], Z. Lu[2], J. C. Campbell[2] and Y. Kang[3], [1]University of California Santa Barbara, ECE Department, Santa Barbara, California, USA, [2]University of Virgina, ECE Deaprtment, Charlottesville, Virginia, USA and [3]Intel Corporation, Santa Clara, California, USA

VI.A-5
11:40 AM
Late News

Session VI.B **Thin Film Transistors (II)** 233-246

VI.B-1
10:00 AM
High Performance and Low Driving Voltage Amorphous InGaZnO Thin-Film Transistors Using High-k HfSiO Dielectrics
C.-K. Chiang[1], C.-H. Wu[2], and S.-J. Wang[1], [1]Institute of Microelectronics, Dept. of Electr. Eng., National Cheng Kung Univ., Tainan, TAIWAN and [2]Dept. of Microelectronics Eng., Chung Hua Univ., Hsinchu, TAIWAN

VI.B-2
10:20 AM
Backside Gate Thin Film Transistor based on MOCVD Grown ZnO on SiO_2/Si Substrates
J.-P. Biethan[1], B. Bayraktaroglu[2], L. Considine[1] and D. Pavlidis[1], [1]Technische Universität Darmstadt, Department of High Frequency Electronics, Darmstadt, GERMANY and [2]Air Force Research Laboratory, Sensors Directorate, AFRL/RYD, Wright Patterson AFB, Ohio, USA

VI.B-3
10:40 AM
Growth Temperature Influence on Nanocrystalline ZnO Thin Film FET Performance
B. Bayraktaroglu and K. Leedy, Air Force Research Laboratory, Sensors Directorate, Wright Patterson AFB, Ohio, USA

VI.B-4
11:00 AM
Gamma-Ray Irradiation of ZnO Thin Film Transistors and Circuits
D. Zhao[1,2], D. A. Mourey[1,3], and T. N. Jackson[1,2], [1]Center for Thin Film Devices and Materials Research Institute, [2]Department of Electrical Engineering, Penn State University, University Park, Pennsylvania, USA, and [3]Department of Materials and Science Engineering, Penn State University, University Park, Pennsylvania, USA

VI.B-5
11:20 AM
Thermal Effects in Oxide TFTs
D. A. Mourey[1,2], D. A. Zhao[1,3], H. H. R. Fok[1,3], Y. V. Li[1,3], and T. N. Jackson[1,3], [1]Center for Thin Film Devices and Materials Research Institute,[2] Department of Materials and Science Engineering, and [3] Department of Electrical Engineering, Penn State University, University Park, Pennsylvania, USA

VI.B-6
11:40 AM
Performance Improvements in Polysilicon Source-Gated Transistors
R. A. Sporea[1], M. J. Trainor[2], N. D. Young[3], J. M. Shannon[1], and S. R. P. Silva[1], [1]Advanced Technology Institute, FEPS, University of Surrey, Guildford, Surrey, UK, [2]MiPlaza, Philips Research, High Tech Campus 4, Eindhoven, THE NETHERLANDS and [3]Philips Research, Cambridge, UK

Session VII.A **Memory** 247-266

VII.A-1
1:30 PM
Non-volatile Spin-Transfer Torque RAM (STT-RAM)
E. Chen, D. Lottis, A. Driskill-Smith, D. Druist, V. Nikitin, S. Watts, X. Tang, and D. Apalkov, Grandis, Inc., Milpitas, California, USA

VII.A-2 2:10 PM **Ultra-Low Power Phase Change Memory with Carbon Nanotube Interconnects**
F. Xiong[1,2], A. Liao[1,2], D. Estrada[1,2], and E. Pop[1,2,3], [1]Micro & Nanotechnology Laboratory, University of Illinois, Urbana-Champaign, Illinois, USA, [2]Dept. of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, Illinois, USA and [3]Beckman Institute, University of Illinois, Urbana-Champaign, Illinois, USA

VII.A-3 2:30 PM **Kinetic Monte Carlo simulation of resistive switching and filament growth in electrochemical RRAMs**
F. Pan and V. Subramanian, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California, USA

VII.A-4 2:50 PM **A Novel Ferroelectric Memristor Enabling NAND-type Analog Memory Characteristics**
Y. Kaneko[1], H. Tanaka[1], M. Ueda[1], Y. Kato[2], and E. Fujii[1], [1]Advanced Technology Research Laboratories, Panasonic Corporation and [2]Semiconductor Device Research Center, Panasonic Corporation, Soraku-gun, Kyoto, JAPAN

VII.A-5 3:30 PM **Ultra-thin-body PECVD Ge TFT low-voltage flash memory cell with high-k dielectrics for three-dimensional integration**
J. Lee[1,2], J. J. Cha[3], T. Naoi[4], D. A. Muller[3], R. B. van Dover[4], J. T. Shaw[1], and E. C. Kan[1], [1]School of Electrical and Computer Engineering, Cornell University, Ithaca, New York, USA, [2]Flash Core Technology Lab., Semiconductor R&D Center, Samsung Electronics Co., LTD, Gyeonggi-Do, KOREA, [3]School of Applied and Engineering Physics, Cornell University, Ithaca, New York, USA, and [4]Department of Material Science and Engineering, Cornell University, Ithaca, New York, USA

VII.A-6 3:50 PM **A Charge-Trapping Memory Structure Featuring Low-Voltage High-Speed Operation and 250 °C Retention**
C.-Y. Peng[1], W. Q. Zhang[1], X. Sun[1], Z. G. Liu[1], S. Cui[1], T. P. Ma[1], L. Kornblum[2] and M. Eizenberg[2], [1]Department of Electrical Engineering, Yale University, New Haven, Connecticut, USA and [2]Department of Materials Engineering, Technion - Israel Institute of Technology, Haifa, ISRAEL

VII.A-7 4:10 PM **A Novel Multi-bit Non-Uniform Channel Charge Trapping Memory with Virtual-Source NAND Array** (Withdrawn)
H. Gu, L. Pan, P. Zhu, D. Wu, Z. Zhang and J. Xu, Institute of Microelectronics, Tsinghua University, Beijing, PRC

VII.A-8 4:30 PM **Highly Scalable Vertical Bandgap-Engineered NAND Flash Memory**
S. Cho, Y. Kim, W. B. Shim, D. H. Li, J.-H. Lee, H. Shin, and B.-G. Park, Inter-university Semiconductor Research Center (ISRC) and School of Electrical Engineering and Computer Science, Seoul National University, Shillim-dong, Gwanak-gu, Seoul, REPUBLIC OF KOREA

Session VII.B **Nanowire and Nanotube Devices** 267-284

VII.B-1 1:30 PM **Gate-All-Around Silicon Nanowire MOSFETs and Circuits**
J. W. Sleight, S. Bangsaruntip, A. Majumdar, G. M. Cohen, Y. Zhang, S. U. Engelmann, N. C. M. Fuller, L. M. Gignac, S. Mittal, J. S. Newbury, M. M. Frank, J. Chang, and M. Guillorn, IBM T. J. Watson Research Center, Yorktown Heights, New York, USA

VII.B-2 2:10 PM **Fabrication of Axially-Doped Silicon Nanowire Tunnel FETs and Characterization of Tunneling Current**
A. L. Vallett[1], S. Minassian[2], S. Datta[1], J. M. Redwing[1,2] and T. S. Mayer[1,2], [1]Department of Electrical Engineering and [2]Department of Materials Science and Engineering, The Pennsylvania State University, University Park, Pennsylvania, USA

VII.B-3 2:30 PM **Channel and Contact Length Scaling in Carbon Nanotube Transistors**
A. D. Franklin, A. A. Bol, and Z. Chen, IBM T. J. Watson Research Center, Yorktown Heights, New York, USA

VII.B-4
2:50 PM
Interface state density measurements in gated p-i-n silicon nanowires as a function of the nanowire diameter
G. M. Cohen, E. Cartier, S. Bangsaruntip, A. Majumdar, W. Haensch, L. M. Gignac, S. Mittal, and J. W. Sleight, IBM Research Division, T. J. Watson Research Center, Yorktown Heights, New York, USA

VII.B-5
3:30 PM
Fabrication and RF performance of InAs Nanowire FET
W. Prost and F. J. Tegude, Solid State Electronics Department, CeNIDE, University of Duisburg-Essen, Duisburg, GERMANY

VII.B-6
4:10 PM
Improve Variability in Carbon Nanotube FETs by Scaling
Y. Sun, G. Tuleski, S.-J. Han, W. Haensch and Z. Chen, IBM T.J. Watson Research Center, Yorktown Heights, New York, USA

VII.B-7
4:30 PM
Late News

Author Index