2010 Symposium on VLSI Technology

(VLSIT 2010)

Honolulu, Hawaii, USA
15-17 June 2010

IEEE Catalog Number: CFP10VTS-PRT
ISBN: 978-1-4244-5451-8

SESSION 1

Plenary Session

Tuesday, June 15, 8:05 a.m.
TAPA I

Chairpersons: M.R. Lin, GLOBALFOUNDRIES
H. Wakabayashi, Sony Corporation

1.1 – %
The Smart Grid and Key Research Technical Challenges, Michael Rosenfield, IBM TJ Watson Research Center

1.2 – +
SiC Technologies for Future Energy Electronics, Tsunenobu Kimoto, Kyoto University

SESSION 2

Advanced CMOS I

Tuesday, June 15, 10:20 a.m.
TAPA I

Chairpersons: O. Faynot, CEA-LETI
M. Masahara, AIST

2.1 - 1'

Enhanced Performance in SOI FinFETs with Low Series Resistance by Aluminum Implant as a Solution Beyond 22nm Node, I. Ok, C. Young, W.-Y. Loh, T. Ngai, S. Lian, J. Oh, M. Rodgers^, S. Bennett^, H. Stamper^, D. Franca^, S. Lin*, K. Akarvardar**, C. Smith, C. Hobbs, P. Kirsch, R. Jammy, Sematech, ^CNSE, *UMC, **GLOBALFOUNDRIES, USA

2.2 - 1)

A 0.063 μm^2 FinFET SRAM Cell Demonstration with Conventional Lithography Using a Novel Integration Scheme with Aggressively Scaled Fin and Gate Pitch, V. Basker, T. Standaert, H. Kawasaki**, C.-C. Yeh, K. Maitra*, T. Yamashita, J. Faltermeier, H. Adhikari*, H. Jagannathan, J. Wang, H. Sunamura^, S. Kanakasabapathy, S. Schmitz, J. Cummings, A. Inada^, C.-H. Lin, P. Kulkarni, Y. Zhu^^, J. Kuss, T. Yamamoto^, A. Kumar^^, J. Wahl*, A. Yagashita**, L.F. Edge, R.H. Kim*, E. Mclellan, S.J. Holmes, R.C. Johnson, T. Levin, J. Demarest, M. Hane^, M. Takayanagi**, M. Colburn, V.K. Paruchuri, R.J. Miller*, H. Bu, B. Doris, D. McHerron, E. Leobandung and J. O'Neill, IBM Research, *GLOBALFOUNDRIES Inc., **Toshiba America Electronic Components Inc, ^NEC Electronics, ^^IBM T.J. Watson Research Center, USA

2.3 - 1+

Gate-all-around Silicon Nanowire 25-Stage CMOS Ring Oscillators with Diameter Down to 3 nm, S. Bangsaruntip, A. Majumdar, G. Cohen, S. Engelmann, Y. Zhang, M. Guillorn, L. Gignac, S. Mittal, W. Graham, E. Joseph, D. Klaus, J. Chang, E. Cartier, J. Sleight, IBM T.J. Watson Research Center, USA

2.4 - 1-

High Yield Sub-0.1μm^2 6T-SRAM Cells, Featuring High-k/Metal-Gate Finfet Devices, Double Gate Patterning, a Novel Fin Etch Strategy, Full-Field EUV Lithography and Optimized Junction Design & Layout, N. Horiguchi, S. Demuynck, M. Ercken, S. Locorotondo, F. Lazzarino, E. Altamirano, C. Huffman, S. Brus, M. Demand, H. Struyf, J. De Backer, J. Hermans, C. Delvaux, T. Vandeweyer, C. Baerts, G. Mannaert, V. Truffert, J. Verluijs, W. Alaerts, H. Dekkers, P. Ong, N. Heylen, K. Kellens, H. Volders, A. Hikavvy, C. Vrancken, M. Rakowski, S. Verhaegen, G. Vandenberghe, G. Beyer, A. Lauwers, P. Absil, T. Hoffman, K. Ronse, and S. Biesemans, IMEC, Belgium

SESSION 3

Reliability and Stability

Tuesday, June 15, 10:20 a.m.
TAPA II

Chairpersons: J. Cheek, Freescale
S. Chung, National Chiao Tung University

3.1 - &%
Highly Accurate Product-Level Aging Monitoring in 40nm CMOS, K. Hofmann, H. Reisinger, K. Ermisch, C. Schlünder, W. Gustin, T. Pompl, G. Georgakos, K. von Arnim, J. Hatsch, T. Kodytek, T. Baumann, C. Pacha, Infineon Technologies AG, Germany

3.2 - &'
New Insight on V_T Stability of HK/MG Stacks with Scaling in 30nm FDSOI Technology, L. Brunet*, X. Garros, M. Casse, O. Weber, F. Andrieu, C. Fenouillet-Béranger, P. Perreau, F. Martin, M. Charbonnier, D. Lafond, C. Gaumer*, S. Lhostis*, V. Vidal, L. Brévard, L. Tosti, S. Denorme*, S. Barnola, J. Damlencourt, V. Loup, G. Reimbold, F. Boulanger, O. Faynot, Alain Bravaix, CEA-Leti Minatec, *STMicroelectronics, France

3.3 - &)
Suppression of NBTI-Induced V_{MIN} Shifts Using Hafnium Doping to Gate Poly/SiON Interface and Optimized NiPt Process for 40nm Node SRAM Cell, Y.Kitamura, T. Sanuki, K. Matsuo, T. Shimizu, A. Ohta, Y. Arayashiki, H. Fukui, T. Hoshino, Y. Ueki, A. Yasumoto, H. Yoshimura, T. Asami, H. Oyamatsu, Toshiba Corporation, Japan

3.4 - &+
Suppression of Anomalous Threshold Voltage Increase with Area Scaling for Mg- or La-Incorporated High-k/Metal Gate nMISFETs in Deeply Scaled Region, T. Morooka, M. Sato, T. Matsuki, T. Suzuki, K. Shiraishi*, A. Uedono*, S. Miyazaki**, K. Ohmori^, K. Yamada^, T. Nabatame^^, T. Chikyow^^, J. Yugami, K. Ikeda, Y. Ohji, Semiconductor Leading Edge Technologies, Inc, *Tsukuba University, **Hiroshima University, ^Waseda University, ^^National Institute for Material Science, Japan

SESSION 4

Advanced CMOS II

Tuesday, June 15, 1:30 p.m.
TAPA I

Chairpersons: M. Khare, IBM
H. Kurata, Fujitsu Semiconductor Ltd.

4.1 - &
20nm Gate Length Trigate pFETs on Strained SGOI for High Performance CMOS, L. Hutin, M. Cassé, C. Le Royer, J.-F. Damlencourt, A. Pouydebasque, C. Xu, C. Tabone, J.-M. Hartmann, V. Carron, H. Grampeix, V. Mazzocchi, R. Truche, O. Weber, P. Batude, X. Garros, L. Clavelier, M. Vinet, O. Faynot, CEA LETI Minatec, France

4.2 - ' %
SiGe CMOS on (110) Channel Orientation with Mobility Boosters: Surface Orientation, Channel Directions, and Uniaxial Strain, J. Oh, S.-H.Lee*, K.-S. Min, J. Huang, B.G. Min, B. Sassman, K. Jeon**, W.-Y. Loh, J. Barnett, I. Ok, C.-Y. Kang, C. Smith, D.-H. Ko^, P. Kirsch, R. Jammy, SEMATECH, *University of Texas at Austin, **University of California, Berkeley, ^Yonsei University, Seoul Korea

4.3 - ' '
High-Mobility $Si_{1-x}Ge_x$-Channel PFETs: Layout Dependence and Enhanced Scalability, Demonstrating 90% Performance Boost at Narrow Widths, G. Eneman, S. Yamaguchi*, C. Ortolland, S. Takeoka**, L Witters, T. Chiarella, P. Favia, A. Hikavvy, J. Mitard, M. Kobayashi^, R. Krom, H. Bender, J. Tseng^^, W.-E. Wang, W. Vandervorst, R. Loo, P. Absil, S. Biesemans, T. Hoffmann, IMEC, *Sony. **Panasonic, ^Stanford University, ^^TSMC

4.4 - ')
FDSOI CMOS with Dielectrically-Isolated Back Gates and 30nm L_G High-k/Metal Gate, M. Khater, J. Cai, R. Dennard, J.-B. Yau, C. Wang, L. Shi, M. Guillorn, J. Ott, Q. Ouyang, W. Haensch, IBM Research, USA

SESSION 5

MRAM and X-Point RRAM

Tuesday, June 15, 1:30 p.m.
TAPA II

Chairpersons: K. Parekh, Micron
B.H. Lee, Gwangju Institute of Science and Technology

5.1 - ' +
A Multi-Level-Cell Spin-Transfer Torque Memory with Series-Stacked Magnetotunnel Junctions, T. Ishigaki, T. Kawahara, R. Takemura, K. Ono, K. Ito, H. Matsuoka, Hideo Ohno*, Hitachi, Ltd., *Tohoku University, Japan

5.2 - ' -
Highly Scalable STT-MRAM with MTJs of Top-pinned Structure in 1T/1MTJ Cell, Y. M. Lee, C.Yoshida, K. Tsunoda, S. Umehara, M. Aoki, T. Sugii, Fujitsu Laboratories, Ltd, Japan

5.3 - (%
Non-volatile Spin-Transfer Torque RAM (STT-RAM): Data, Analysis and Design Requirements for Thermal Stability, A. Driskill-Smith, S. Watts, Vl. Nikitin, D. Apalkov, D. Druist, R. Kawakami, X. Tang, X. Luo, A. Ong, E. Chen, Grandis Inc., USA

5.4 - ('
Novel Cross-point Resistive Switching Memory with Self-formed Schottky Barrier, M. Jo, D.-J.Seong, S. Kim, J. Lee, W. Lee, J.-B. Park, S. Park, S. Jung, J. Shin, D. Lee, H. Hwang, Gwangju Institute of Science and Technology, Korea

SESSION 6

Ultra Thin Body FDSOI

Tuesday, June 15, 3:35 p.m.
TAPA I

Chairpersons: W. Xiong, Texas Instruments
T. Iwamatsu, Renesas Electronics Corp.

6.1 - ( )
Low Leakage and Low Variability Ultra-Thin Body and Buried Oxide (UT2B) SOI Technology for 20nm Low Power CMOS and Beyond, F. Andrieu, O. Weber, J. Mazurier, O. Thomas, J.-P. Noel, C. Fenouillet-Beranger, J.-P. Mazellier, P. Perreau, T. Poiroux, Y. Morand*, T. Morel, S. Allegret*, V. Loup, S. Barnola, F. Martin, J.-F. Damlencourt, I. Servin, M. Cassé, X. Garros, O. Rozeau, M.-A. Jaud, G. Cibrario, J. Cluzel, A. Toffoli, F. Allain, R. Kies, D. Lafond, V. Delaye, C. Tabone, L. Tosti, L. Brévard, P. Gaud, V. Paruchuri**, K. Bourdelle^, W. Schwarzenbach^, O. Bonnin^, B.-Y. Nguyen^, B. Doris**, F. Boeuf*, T. Skotnicki*, O. Faynot, CEA-LETI Minatec, *STMicroelectronics, **IBM Research, ^SOITEC

6.2 - (+
Hybrid Localized SOI/Bulk Technology for Low Power System-on-Chip, J.-L. Huguenin, S. Monfray, G. Bidal, S. Denorme, P. Perreau**, S. Barnola**, M.-P. Samson, C. Arvet, K. Benotmane**, N. Loubet, Q. Liu, Y. Campidelli, F. Leverd, F. Abbate, L. Clement, C. Borowiak, A. Cros, A. Bajolet, S. Handler, D. Marin-Cudraz, T. Benoist, P. Galy, C. Fenouillet-Beranger**, O. Faynot**, G. Ghibaudo*, F. Boeuf, T. Skotnicki, STMicroelectronics, *IMEP-LAHC, **CEA-LETI Minatec

6.3 - (-
Ultra-Thin-Body and BOX (UTBB) Fully Depleted (FD) Device Integration for 22nm Node and Beyond, Q. Liu, A. Yagishita*, N. Loubet, A. Khakifirooz**, P. Kulkarni**, T. Yamamoto^, K. Cheng**, M. Fujiwara*, J. Cai**, D. Dorman**, S. Mehta**, P. Khare, K. Yako^, Y. Zhu**, S. Mignot, S. Kanakasabapathy**, S. Monfray, F. Boeuf, C. Koburger**, H. Sunamura^, S. Ponoth**, A. Reznicek**, B. Haran**, A. Upham**, R. Johnson**, L.F. Edge**, J. Kuss**, T. Levin**, N. Berliner**, E. Leobandung**, T. Skotnicki, M. Hane^, H. Bu**, K. Ishimaru*, W. Kleemeirer, M. Takayanagi*, B. Doris**, R. Sampson, STMicroelectronics, *Toshiba, **IBM, ^NEC Electronics

6.4 -) %
Scalability Study of Ultra-Thin-Body SOI-MOSFETs Using Full-band and Quantum Mechanical Based Device Simulation, H. Takeda, K. Takeuchi, Y. Hayashi, NEC Electronics Corporation, Japan

6.5 - 5'
Efficient Multi-V_T FDSOI Technology with UTBOX for Low Power Circuit Design, C. Fenouillet-Beranger, O. Thomas, P. Perreau, J.-P. Noel, A. Bajolet*, S. Haendler*, L. Tosti, S. Barnola, R. Beneyton*, C. Perrot*, C. de Buttet, F. Abbate*, F. Baron*, B. Pernet*, Y. Campidelli*, L. Pinzelli*, P. Gouraud*, M. Cassé, C. Borowiak*, O. Weber, F. Andrieu, K. Bourdelle**, F. Boeuf*, O. Faynot, T. Skotnicki*, CEA/LETI, *STMicroelectronics, **Soitec

SESSION 7

Process Technology

Tuesday, June 15, 3:25 p.m.
TAPA II

Chairpersons: C.-P. Chang, Applied Materials, Inc.
S. Hayashi, Panasonic Corporation

7.1 -))
Direct Contact of High-k/Si Gate Stack for EOT below 0.7 nm using LaCe-silicate Layer with V_{fb} Controllability, K. Kakushima, T. Koyanagi, D. Kitayama, M. Kouda, J. Song, T. Kawanago, M. Mamatrishat, K. Tachi, M.K. Bera, P. Ahmet, H. Nohira**, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, K. Yamada*, H. Iwai, Tokyo Institute of Technology, *Waseda University, ** Tokyo City University

7.2 -) +
Minimization of Threshold Voltage Variation to A_{VT}=1.3mVμm in Bulk High-k/Metal Gated Devices by Dopant-Diffusion Control Using Integrated FSP-FLA Technology, S. Kato, T. Aoyama, T. Onizawa, K. Ikeda, Y. Ohji, Semiconductor Leading Edge Technologies, Inc, Japan

7.3 -) -
Laser Annealed Junctions: Pocket Profile Analysis Using an Atomistic Kinetic Monte Carlo Approach, T. Noda, C. Ortolland*, W. Vandervorst*, C. Vrancken*, E. Rosseel*, T. Clarysse*, P. Absil*, S. Biesemans*, T. Hoffmann*, Panasonic Corporation, Japan, *IMEC, Belgium

7.4 - * %
New Methods for the Direct Extraction of Mobility and Series Resistance from a Single Ultra-Scaled Device, J.P. Campbell, K.P.Cheung, L.C. Yu, J.S. Suehle, K. Sheng*, A Oates**, NIST, *Rutgers University, USA, **TSMC, Taiwan

7.5 - * '
Evidence of Correlation Between Surface Roughness and Interface States Generation in Unstrained and Strained-Si MOSFETs, Y. Zhao, M. Takenaka, S. Takagi, The University of Tokyo, Japan

SESSION 8

RRAM

Wednesday, June 16, 8:30 a.m.
TAPA I

Chairpersons: J. Lutze, Sandisk Corp.
S. Ohnishi, Sharp Corp.

8.1 - *)
Novel Ultra-Low Power RRAM with Good Endurance and Retention, C.H. Cheng, A. Chin, F.S. Yeh, National Tsing Hua University, National Chiao-Tung University

8.2 - * +
A New Approach for Improving Operating Margin of Unipolar ReRAM using Local Minimum of Reset Voltage, Y. Sakotsubo, M. Terai, S. Kotsuji, Y. Saito, M. Tada, Y. Yabe, H. Hada, NEC Corporation, Japan

8.3 - * -
A Novel Cu_xSi_yO Resistive Memory in Logic Technology with Excellent Data Retention and Resistance Distribution for Embedded Applications, M. Wang, W. Luo, Y. Wang, L. Yang, W. Zhu, P. Zhou, J. Yang, X. Gong, Y. Lin, R. Huang*, S. Song*, Q. Zou*, H. Wu*, J. Wu*, M. Chi*, Fudan University, *Semiconductor Manufacturing International Corp., China

8.4 - +%
A Novel TiTe Buffered Cu-GeSbTe/SiO_2 Electrochemical Resistive Memory (ReRAM), Y.-Y. Lin, F.-M. Lee, Y.-C. Chen, W.-C. Chien, C.-W. Yeh, K.-Y. Hsieh, C.-Y. Lu, Macronix International Co., Ltd, Taiwan

SESSION 9

Variability

Wednesday, June 16, 10:25 a.m.
TAPA II

Chairpersons: R. Jammy, SEMATECH
S. Yamakawa, Sony Corp.

9.1 - +'
Application of a Statistical Compact Model for Random Telegraph Noise to Scaled-SRAM Vmin Analysis, M. Tanizawa, S. Ohbayashi, T. Okagaki, K. Sonoda, K. Eikyu, Y. Hirano, K. Ishikawa, O. Tsuchiya, Y. Inoue, Renesas Technology Corp., Japan

9.2 - +)
Analysis and Prospect of Local Variability of Drain Current in Scaled MOSFETs by a New Decomposition Method, T. Tsunomura, A. Kumar*, T. Mizutani*, C. Lee*, A. Nishida, K. Takeuchi, S. Inaba, S. Kamohara, K. Terada**, T. Hiramoto, T. Mogami, MIRAI-Selete, *The University of Tokyo, **Hiroshima City University

9.3 - ++
Statistical Evaluation for Trap Energy Level of RTS Characteristics, A. Teramoto, T. Fujisawa, K. Abe, S. Sugawa, T. Ohmi, Tohoku University, Japan

9.4 - +-
On the Gate-Stack Origin Threshold Voltage Variability in Scaled FinFETs and Multi-FinFETs, Y. Liu, K. Endo, S. Ouchi, T. Kamei*, J. Tsukada, H. Yamauchi, Y. Ishikawa, T. Hayashida*, K. Sakamoto, T. Matsukawa, A. Ogura*, M. Masahara, AIST, *Meiji University, Japan

SESSION 10

3D Integration

Wednesday, June 16, 10:25 a.m.
TAPA III

Chairpersons: B. van Schravendijk, Novellus Systems, Inc.
T. Tanaka, Tohoku University

10.1 - , %
Development of Sub 10-µm Ultra-ThinningTechnology Using Device Wafers for 3D Manufacturing of Terabit Memory, N. Maeda, Y.S. Kim*, Y. Hikosaka*, T. Eshita*, H. Kitada, K. Fujimoto**, Y. Mizushima^, K. Suzuki**, T. Nakamura^, A. Kawai^^, K. Arai^^, T. Ohba, The University of Tokyo, *Fujitsu Microelectronics Ltd., **Dai Nippon Printing, ^Fujitsu Laboratories Ltd., ^^DISCO Corporation, Japan

10.2 - , '
Assembly-Stress-Mechanism in Pad Areas on High-k/Metal Gate Transistors, Y. Ota, F. Itoh, K. Ishikawa, K. Hagihara, T. Matsumoto, T. Iwase, Y. Itoh, H. Hirano, Panasonic Corporation, Japan

10.3 - ,)
Impact of Thinning and Through Silicon Via Proximity on High-k / Metal Gate First CMOS Performance, A. Mercha, A. Redolfi, M. Stucchi, N. Minas, J. Van Olmen, S. Thangaraju, D. Velenis, S. Domae*, Y. Yang^^, G. Katti^^, R. Labie, C. Okoro^^, M. Zhao, P. Asimakopoulos, I. De Wolf, T. Chiarella, T. Schram, E. Rohr, A. Van Ammel, A. Jourdain, W. Ruythooren, S. Armini, A. Radisic, H. Philipsen, N. Heylen, M. Kostermans, P. Jaenen, E. Sleeckx, D. Sabuncuoglu Tezcan, I. Debusschere, P. Soussan, D. Perry**, G. Van der Plas, J.H. Cho^, P. Marchal, Y. Travaly, E. Beyne, S. Biesemans, B. Swinnen, IMEC, *Panasonic, ** Qualcomm, ^Samsung, ^^IMEC and KU Leuven, Belgium

10.4 - , +
A Novel TFT with a Laterally Engineered Bandgap for of 3D Logic and Flash Memory, S.-J. Choi, J.-W. Han, S. Kim, D.-I. Moon, M. Jang*, Y.-K. Choi, KAIST, *ETRI, Korea

SESSION 11

Beyond CMOS

Wednesday, June 16, 1:30 p.m.
TAPA II

Chairpersons: A. Seabaugh, Notre Dame University
T. Hiramoto, The University of Tokyo

11.1 - , -
Reliable Solid-Electrolyte Crossbar Switch for Programmable Logic Device, N. Banno, T. Sakamoto, M. Tada, M. Miyamura, Y. Yabe, Y. Saito, S. Ishida, K. Okamoto, H. Hada, N. Kasai, N. Iguchi*, M. Aono*, NEC Corp., *NIMS, Japan

11.2 - - %
Realistic Spin-FET Performance Assessment for Reconfigurable Logic Circuits, Y. Gao, C. Augustine, D. Nikonov*, K. Roy, M. Lundstrom, Purdue University, *Intel, USA

11.3 - - '
Reconfigurable Characteristics of Spintronics-based MOSFETs for Nonvolatile Integrated Circuits, T. Inokuchi, T. Marukame, T. Tanamoto, H. Sugiyama, M. Ishikawa, Y. Saito, Toshiba Corporation, Japan

11.4 - -)
Si Tunnel Transistors with a Novel Silicided Source and 46mV/dec Swing, K. Jeon, W.-Y. Loh*, P. Patel, C.Y. Kang*, J. Oh*, A. Bowonder, C. Park*, C.S. Park*, C. Smith*, P. Majhi*, H.-H. Tseng**, R. Jammy*, T.-J. King Liu, C. Hu, *SEMATECH, **Texas State University The University of California, Berkeley, USA

SESSION 12

NAND Flash Memory

Wednesday, June 16, 1:30 p.m.
TAPA III

Chairpersons: J. Lutze, Sandisk Corp.
J.T. Moon, Samsung Electronics Co., Ltd.

12.1 - - +
32nm 3-Bit 32Gb NAND Flash Memory with DPT (Double Patterning Technology) Process for Mass Production, B.T. Park, J.H. Song, E.S. Cho, S.W. Hong, J.Y. Kim, Y. J. Choi, Y.S. Kim, S.J. Lee, C.K. Lee, D.W. Kang, D.J. Lee, B.T. Kim, Y.J. Choi, W.K. Lee, J.-H. Choi, K.-D. Suh*, T.-S. Jung, Samsung Electronics, *STET, Korea

12.2 - - -
A New Floating Gate Cell Structure with a Silicon-nitride Cap Layer for Sub-20 nm NAND Flash Memory, K.S. Seol, H. Kang, J. Lee, H. Kim, B. Cho, D. Lee, Y.-L. Choi, N.-H. Ju, C. Choi, S. Hur, J. Choi, C. Chung, Samsung Electronics

12.3 - %$%
Novel Dual Layer Floating Gate Structure as Enabler of Fully Planar Flash Memory, P. Blomme, M.Rosmeulen, A. Cacciato, M. Kostermans, C. Vrancken, S. Van Aerde*, T. Schram, I. Debusschere, M. Jurczak, J. Van Houdt, IMEC, *ASM, Belgium

12.4 - %$'
A Highly Scalable 8-Layer 3D Vertical-Gate (VG) TFT NAND Flash Using Junction-Free Buried Channel BE-SONOS Device, H.-T. Lue, T.-H. Hsu, Y.-H. Hsiao, S.P. Hong, M.T. Wu, F.H. Hsu, N.Z. Lien, S.-Y. Wang, J.-Y. Hsieh, L.-W. Yang, T. Yang, K.-C. Chen, K.-Y. Hsieh, C.-Y. Lu, Macronix International Co., Ltd, Taiwan

SESSION 13

Design Enablement I

Wednesday, June 16, 3:35 p.m.
TAPA II

Chairpersons: K. Schruefer, Infineon Technologies
C. Wann, TSMC

13.1 - %$)
A Dual Core Oxide 8T SRAM Cell with Low Vccmin and Dual Voltage Supplies in 45nm Triple Gate Oxide and Multi Vt CMOS for Very High Performance yet Low Leakage Mobile SoC Applications, P. Liu, J. Wang, M. Phan, M. Garg, R. Zhang, A. Cassier, L. Chua-Eoan, B. Andreev, S. Weyland, S. Ekbote, M. Han, J. Fischer, G. Yeap, P.-W. Wang*, Q. Li*, C.S. Hou*, S.B. Lee*, Y.F. Wang*, S.S. Lin*, M. Cao*, Y.J. Mii*, Qualcomm, USA, *TSMC, Taiwan

13.2 - %$+
A 32nm Low Power RF CMOS SOC Technology Featuring High-k/Metal Gate, P. VanDerVoorn, M. Agostinelli, S.-J. Choi, G. Curello, H. Deshpande, M. A. El-Tanani, W. Hafez, U. Jalan, L. Janbay, M. Kang, K.-J. Koh, K. Komeyli, H. Lakdawala, J. Lin, N. Lindert, S. Mudanai, J. Park, K. Phoa, A. Rahman, J. Rizk, L. Rockford, G. Sacks, K. Soumyanath, H. Tashiro, S. Taylor, C. Tsai, H. Xu, J. Xu, L. Yang, I. Young, J.-Y. Yeh, J. Yip, P. Bai, C.-H. Jan, Intel Corporation

13.3 – %$-
Enabling Application-Specific Integrated Circuits on Limited Pattern Constructs (Invited), D. Morris, V. Rovner, L. Pileggi, A. Strojwas, K. Vaidyanathan, Carnegie Mellon University, USA

13.4 – %%%
Novel Circuit Design and Process Technology for Leading-Edge Products (Invited), K. Miyamoto, A. Strojwas*, E. Hosomi, M. Ooida**, H. Ezawa, M. Fukuda, Y. Matsubara and K. Numata, Toshiba Corporation, *PDF Solutions, Inc,- **J-Devices Corporation, Japan

13.5 – %%
Design-Technology Interaction for Post-32 nm Node CMOS Technologies (Invited), G. Shahidi, IBM Thomas J. Watson Research Center, USA

SESSION 14

Heterogeneous Integration

Wednesday, June 16, 3:25 p.m.
TAPA III

Chairpersons: R. Chau, Intel Corp.
K. Shibahara, Hiroshima University

14.1 – %&)
III-V/Ge CMOS Technologies on Si Platform (Invited), S. Takagi and M. Takenaka, The University of Tokyo, Japan

14.2 – %&+
III-V: Replacing Si or More than Moore? (Invited), Y. Sun, IBM Thomas J. Watson Research Center, USA

14.3 – %&
GaN-on-Si: A Scalable Material System to Realize Cost Effective Next-Generation Solid State Lighting and Power Devices (Invited), S. Decoutere, H. Osman, J. Dekoster, B. Dutta, S. Biesemans, IMEC, Belgium

14.4 – %&%
How Can High Mobility Channel Materials Boost or Degrade Performance in Advanced CMOS (Invited), T. Skotnicki and F. Boeuf, STMicroelectronics, France

14.5 – %&'
Classification and Benchmarking of III-V MOSFETs for CMOS (Invited), M. Passlack, G. Doornbos, C. Wann, Y.C. Sun, TSMC, Belgium, Taiwan

SESSION 15

DRAM

Thursday, June 17, 8:30 a.m.
TAPA II

Chairpersons: C. Mazure, Soitec Group
R. Yamada, Hitachi Research Institute

15.1 - %&)
Integration of Back-Gate Doping for 15-nm Node Floating Body Cell (FBC) Memory, I. Ban, U. Avci, D. Kencke, P. Tolchinsky, P. Chang, Intel Corp, USA

15.2 - %&+
A Low-Voltage Biasing Scheme for Aggressively Scaled Bulk FinFET 1T-DRAM Featuring 10s Retention at 85°C, N. Collaert, M. Aoulaiche, B. De Wachter, M. Rakowski, A. Redolfi, S. Brus, A. De Keersgieter, N. Horiguchi, L. Altimime, M. Jurczak, IMEC, Belgium

15.3 - %&-
Vertical Double Gate Z-RAM Technology with Remarkable Low Voltage Operation for DRAM Application, J.-S. Kim, S.-W. Chung, T.-S.Jang, S.-H. Lee, D.-H. Son, S.-J. Chung, S.-M. Hwang, S. Banna*, S. Bhardwaj*, M. Gupta*, J. Kwon*, D. Kim*, G. Popov*, V. Gopinath*, M. van Buskirk*, S.-H. Cho, J.-S. Roh, S.-J. Hong, S.-W. Park, Hynix Semiconductor, Korea, *Innovative Silicon, USA

15.4 - % %
Silicon on Replacement Insulator (SRI) Floating Body Cell (FBC) Memory, S. Kim, R. Tseng, W. Rachmady, B. Jin, U. Shah, I. Ban, U. Avci, P. Chang, Intel Corporation, USA

SESSION 16

Novel Devices

Thursday, June 17, 8:30 a.m.
TAPA III

Chairpersons: C.P. Chang, Applied Materials, Inc.
Y. Mochizuki, NEC Corp.

16.1 - % '
Short-Channel Performance and Mobility Analysis of <110>- and <100>-Oriented Tri-Gate Nanowire MOSFETs with Raised Source/Drain Extensions, M. Saitoh, Y. Nakabayashi, H. Itokawa, M. Murano, I. Mizushima, K. Uchida*, T. Numata, Toshiba Corporation, *Tokyo Institute of Technology, Japan

16.2 - %)
Bistable Resistor (Biristor) – Gateless Silicon Nanowire Memory, J.-W. Han, Y.-K. Choi, KAIST, Korea

16.3 - % +
Highly Reliable Vertical NAND Technology with Biconcave Shaped Storage Layer and Leakage Controllable Offset Structure, W. Cho, S. Shim, J. Jang, H. Kim, J. Choi, C. Chung, H.-S. Cho, B.-K. You, B.-K. Son, K.-S. Kim, J.-J. Shin, C.-M. Park, J.-S. Lim, K.-H. Kim, D.-W. Chung, J.-Y. Lim, H.-C. Moon, S.-M. Huang, H.-S. Lim, Samsung Electronis Co.LTD, Korea

16.4 - % -
Mobility Enhancement over Universal Mobility in (100) Silicon Nanowire Gate-All-Around MOSFETs with Width and Height of Less Than 10nm Range, J. Chen, T. Saraya, T. Hiramoto, University of Tokyo, Japan

SESSION 17

Advanced CMOS III

Thursday, June 17, 10:25 a.m.
TAPA II

Chairpersons: T. Skotnicki, STMicroelectronics
Y. Akasaka, Tokyo Electron Ltd.

17.1 - 1(%
Comprehensive Study and Control of Oxygen Vacancy Induced Effective Work Function Modulation in Gate-First High-k/Metal Inserted Poly-Si Stacks, T. Hosoi, M. Saeki, Y. Oku, H. Arimura, N. Kitano, K. Shiraishi*, K. Yamada**, T. Shimura^, H. Watanabe^, ^Osaka University, *University of Tsukuba, **Waseda University, Japan

17.2 - 1('
8Å Tinv Gate-First Dual Channel Technology Achieving Low-V_t High Performance CMOS, L. Witters, S. Takeoka, S. Yamaguchi, A. Hikavyy, D. Shamiryan, M.J. Cho, T. Chiarella, L.-Å. Ragnarsson, R. Loo, C. Kerner, Y. Crabbe, J. Franco, J. Tseng, W.-E. Wang, E. Rohr, T. Schram, O. Richard, H. Bender, S. Biesemans, P. Absil, T. Hoffmann, IMEC, Belgium

17.3 - 1( )
Dipole Controlled Metal Gate with Hybrid Low Resistivity Cladding for Gate-Last CMOS with Low Vt, C. Hinkle, R. Galatage, R. Chapman, E. Vogel, H. Alshareef*, C. Freeman**, E. Wimmer**, H. Niimi^, A. Li-Fatou^, J. Shaw^, J. Chambers, University of Texas at Dallas, USA, King Abdullah University of Science and Technology, Saudi Arabia, ** Materials Design Inc., USA, ^ Texas Instruments, USA

17.4 - 1(+
Ion-Implantation-Based Low-Cost Hk/MG Process for CMOS Low-Power Application, C. Ortolland, S. Sahhaf, V. Srividya, R. Degraeve, K. Saino, C.-S. Kim^, M. Gilbert, T. Kauerauf, M.J.Cho, M. Dehan, T. Schram, M. Togo, N. Horiguchi, G. Groeseneken, S. Biesemans, P. Absil, W. Vandervorst, D. Gealy, T. Hoffmann, IMEC, Belgium

SESSION 18

Characterization and Modeling

Thursday, June 17, 10:25 a.m.
TAPA III

Chairpersons: E. Kan, Cornell University
E. Morifuji, Toshiba Corp.

18.1 - 1(-
Direct Observation of RTN-induced SRAM Failure by Accelerated Testing and Its Application to Product Reliability Assessment, K. Takeuchi, T. Nagumo, K. Takeda, S. Asayama, S. Yokogawa, K. Imai, Y. Hayashi, NEC Electronics Corporation, Japan

18.2 - 1) %
Direct Measurements, Analysis, and Post-Fabrication Improvement of Noise Margins in SRAM Cells Utilizing DMA SRAM TEG, M. Suzuki, T. Saraya, K. Shimizu, A. Nishida*, S. Kamohara*, K. Takeuchi*, S. Miyano**, T. Sakurai, T. Hiramoto, University of Tokyo, *MIRAI-Selete, **STARC, Japan

18.3 - 1) '
Single Dopant Impact on Electrical Characteristics of SOI NMOSFETs with Effective Length Down to 10nm, R. Wacquez, M. Vinet, M. Pierre, B. Roche, X. Jehl, O. Cueto, J. Verduijn*, G.C. Tettamanzi*, S. Rogge*, V. Deshpande, B. Previtali, C. Vizioz, S. Pauliac-Vaujour, C. Comboroure, N. Bove, O. Faynot, M. Sanquer, CEA Grenoble, France, *TU Delft, Netherlands

18.4 - 1))
Dopant and Carrier Profiling in FinFET-Based Devices with Sub-Nanometer Resolution, J. Mody*, A. K. Kambham*, G. Zschaetzsch*, P. Schatzer, T. Chiarella, N. Collaert, L. Witters, M. Jurczak, N. Horiguchi, M. Gilbert*, P. Eyben, S. Koelling*, A. Schulze*, T.Y. Hoffmann, W. Vandervorst, IMEC, *KU Leuven, Belgium

SESSION 19

PCRAM

Thursday, June 17, 1:30 p.m.
TAPA II

Chairpersons: K. Parekh, Micron
H. Miyake, Elpida Memory, Inc.

19.1 - 1) +
Programming Disturbance and Cell Scaling in Phase Change Memory : For up to 16nm Based 4F^2 Cell, S.H. Lee, M.S.Kim, G.S. Do, S.G. Kim, H.J. Lee, J.S. Sim, N.G. Park, S.B. Hong, Y.H. Jeon, K.S. Choi, H.C. Park, T.H. Kim, J.U. Lee, H.W. Kim, M.R. Choi, S.Y. Lee, Y.S. Kim, H.J. Kang, J.H. Kim, H.J. Kim, Y.S. Son**, B.H. Lee, J.H. Choi, S.C. Kim, J.H. Lee, S.J. Hong, S.W. Park, Hynix Semiconductor Inc., Korea

19.2 - 1) -
MLC PRAM with SLC Write-Speed and Robust Read Scheme, Y. Hwang, C. Um, J. Lee, C. Wei, H.-R. Oh, G. Jeong, H. Jeong, C. Kim, C. Chung, Samsung Electronics Co., LTD, Korea

19.3 - %* %
High Performance PRAM Cell Scalable to Sub-20nm Technology with Below 4F^2 Cell Size, Extendable to DRAM Applications, I.S. Kim, S. Cho, D.-H. Im, E.-H. Cho, D. Kim, G. Oh, D.H. Ahn, S.O. Park, S.W. Nam, J.-T. Moon, C. Chung, Samsung Electronics Co., LTD, Korea

19.4 - %* '
Highly-Scalable Novel Access Device Based on Mixed Ionic Electronic Conduction (MIEC) Materials for High Density Phase Change Memory (PCM) Arrays, K. Gopalakrishnan, R. Shenoy, C. Rettner, K. Virwani, D. Bethune, R. Shelby, G. Burr, A. Kellock, R. King, K. Nguyen, A. Bowers, M. Jurich, B. Jackson, A. Friz, T. Topuria, P. Rice, B. Kurdi, IBM Almaden Research Center, USA

SESSION 20

GeMOSFETs

Thursday, June 17, 1:30 p.m.
TAPA III

Chairpersons: R. Jammy, SEMATECH
K. Shibahara, Hiroshima University

20.1 - 1*)
Electron Mobility in High-k Ge-MISFET Goes up to Higher, T. Nishimura, C.H. Lee, S. Wang, T. Tabata, K. Kita, K. Nagashio, A. Toriumi, The University of Tokyo, Japan

20.2 - 1* +
High-k/Ge *p*- & *n*-MISFETs with Strontium Germanide Interlayer for EOT Scalable CMIS Application, Y. Kamata, K. Ikeda, Y. Kamimuta, T. Tezuka, Toshiba, Japan

20.3 - %* -
Impact of Ge Nitride Interfacial Layers on Performance of Metal Gate/High-k Ge-nMISFETs, T. Maeda, Y. Morita, Shinichi Takagi, NIRC-AIST, Japan

20.4 - %+%
Experimental Demonstration of High Source Velocity and its Enhancement by Uniaxial Stress in Ge PFETs, M. Kobayashi*, J. Mitard*, T. Irisawa, T. Hoffmann*, M. Meuris*, K. Saraswat, Y. Nishi, M. Heyns*, Stanford University, USA, *IMEC, Belgium

SESSION 21

Design Enablement II

Thursday, June 17, 3:25 p.m.
TAPA II

Chairpersons: K. Schruefer, Infineon Technologies
C. Wann, TSMC

21.1 - %+'
World's First Monolithic 3D-FPGA with TFT SRAM over 90nm 9 Layer Cu CMOS, T. Naito, T. Ishida, T. Onoduka*, M. Nishigoori, T. Nakayama, Y. Ueno, Y. Ishimoto, A. Suzuki, W. Chung, R. Madurawe**, S. Wu**, S. Ikeda^, H. Oyamatsu, Toshiba Corporation, *Covalent Materials Corp., **Tier Logic Inc., ^tei Technology, Japan

21.2 - %+)
New Cost-Effective Integration Schemes Enabling Analog and High-Voltage Design in Advanced CMOS SOC Technologies, K. Benaissa, G. Baldwin, S. Liu, P. Srinivasan, F. Hou, B. Obradovic, S. Yu, H. Yang, R. McMullan, V. Reddy, C. Chancellor, S. Venkataraman, H. Lu, S. Dey, C. Cirba, Texas Instruments Inc., USA

21.3 – %++
Multi-Design of Architecture, Circuit/Device/Process and Package for Cost-effective Smart Mobile Devices: An Integrated Fabless Manufacturer (IFM)'s Perspective (Invited), G.C-F Yeap, Qualcomm, Inc., USA

21.4 – %+-
Design Challenges and Enablement for 28nm and 20nm Technology Nodes (Invited), C.Y-C Hou, Taiwan Semiconductor Manufacturing Company, Taiwan

21.5 – %,%
High Performance Design with Advanced Features in 22nm and Beyond (Invited), S. Borkar, Intel Corporation, USA

SESSION 22

Exploratory Research

Thursday, June 17, 3:25 p.m.
TAPA III

Chairpersons: A. Seabaugh, Notre Dame University
S. Takagi, The University of Tokyo

22.1 - %'
Study of Channel Length Scaling in Large-Scale Graphene FETs, S.-J. Han, Y. Sun, A. Bol, W. Haensch, Z. Chen, IBM T.J. Watson Research Center, USA

22.2 - %)
III-V MOSFETs with New Self-Aligned Contact, X. Zhang, H. Guo, C.-H. Ko*, C.H. Wann*, C.-C. Cheng*, H.-Y. Lin*, H.-C. Chin, X. Gong, P. Lim, G.-L. Luo**, C.-Y. Chang^, C.-H. Chien**, Z.-Y. Han^, S.-C. Huang**, Y.-C. Yeo, National University of Singapore, *TSMC, **National Nano Device Laboratory, ^National Chiao-Tung University, Taiwan

22.3 - %+
High Mobility III-V-On-Insulator MOSFETs on Si with ALD-Al_2O_3 BOX Layers, M. Yokoyama, Y. Urabe*, T. Yasuda*, H. Takagi*, H. Ishii*, N. Miyata*, H. Yamada**, N. Fukuhara**, M. Hata**, M. Sugiyama, Y. Nakano, M. Takenaka, S. Takagi, The University of Tokyo, *National Institute of Advanced Industrial Science and Technology, **Sumitomo Chemical Co. Ltd., Japan

22.4 - %-
Efficient Metallic Carbon Nanotube Removal Readily Scalable to Wafer-Level VLSI CNFET Circuits, H. Wei, N. Patil, J. Zhang, A. Lin, H.-Y. Chen, H.-S.P. Wong, S. Mitra, Stanford University, USA