

# **2010 International Conference on Embedded Computer Systems**

**(SAMOS 2010)**

**Samos, Greece  
19 – 22 July 2010**



**IEEE Catalog Number: CFP1052A-PRT  
ISBN: 978-1-4244-7936-8**

# Table of Contents

<b>Keynotes</b>	<b>i</b>
Technologies for Reducing Power . . . . .	i
<i>Trevor Mudge</i>	
VLSI Challenges to more Energy Efficient Devices . . . . .	ii
<i>Tawfik Arabi</i>	
<b>Simulation and Modeling</b>	<b>1</b>
Cycle-Accurate Performance Modelling in an Ultra-Fast Just-In-Time Dynamic Binary Translation Instruction Set Simulator . . . . .	1
<i>Igor Böhm, Björn Franke, and Nigel Topham</i>	
A Trace-based Scenario Database for High-level Simulation of Multimedia MP-SoCs . . . . .	11
<i>Peter van Stralen and Andy D. Pimentel</i>	
A Library of Dual-Clock FIFOs for Cost-Effective and Flexible MPSoCs Design . . . . .	20
<i>Alessandro Strano, Daniele Ludovici, and Davide Bertozzi</i>	
Transparent Sampling . . . . .	28
<i>Taj Muhammad Khan, Daniel Gracia-Pérez, and Olivier Temam</i>	
<b>Network Processing</b>	<b>37</b>
Design of a Flexible High-speed FPGA-based Flow Monitor for Next Generation Networks . . . . .	37
<i>John McGlone, Roger Woods, Alan Marshall, and Michaela Blott</i>	
A Fully Programmable FSM-based Processing Engine for Gigabytes/s Header Parsing . . . . .	45
<i>Konstantin Septinus, Peter Pirsch, Holger Blume, and Ulrich Mayer</i>	
Empirical Evaluation of Data Transformations for Network Infrastructure Applications . . . . .	55
<i>Damon Fenacci and Björn Franke</i>	
Design Environment for the Support of Configurable Network Interfaces in NoC-based Platforms . . . . .	63
<i>Amin El Mrabti, Frédéric Rousseau, Frédéric Pétrot, Jérôme Martin, Romain Lemaire, and Emmanuel Vaumorin</i>	

<b>Image and Video Processing</b>	<b>71</b>
<hr/>	
An Efficient Realization of Forward Integer Transform in H.264/AVC Intra-frame Encoder . . . . .	71
<i>Muhammad Nadeem, Stephan Wong, and Georgi Kuzmanov</i>	
SIMD Performance in Software Based Mobile Video Coding . . . . .	79
<i>Tero Rintaluoma and Olli Silvén</i>	
Fast Huffman Decoding by Exploiting Data Level Parallelism . . . . .	86
<i>Tim Drijvers, Carlos Alba Pinto, Henk Corporaal, Bart Mesman, and Gert-Jan van den Braak</i>	
Real-Time Stereo Vision System using Semi-Global Matching Disparity Estimation: Architecture and FPGA-Implementation . . . . .	93
<i>Christian Banz, Sebastian Hesselbarth, Holger Flatt, Holger Blume, and Peter Pirsch</i>	
<b>System-Level Design</b>	<b>102</b>
<hr/>	
Custom Multi-Threaded Dynamic Memory Management for Multiprocessor System-on-Chip Platforms . .	102
<i>Sotirios Xydīs, Alexandros Bartzas, Iraklis Anagnostopoulos, Dimitrios Soudris, and Kiamal Pekmestzi</i>	
Power Aware Heterogeneous MPSoC with Dynamic Task Scheduling and Increased Data Locality for Multiple Applications . . . . .	110
<i>Oliver Arnold and Gerhard Fettweis</i>	
A System-Level Synthesis Approach from Formal Application Models to Generic Bus-Based MPSoCs . . . .	118
<i>Jens Gladigau, Andreas Gerstlauer, Christian Haubelt, Martin Streubühr, and Jürgen Teich</i>	
<b>Profiling and Analysis</b>	<b>126</b>
<hr/>	
ImpBench Revisited: An Extended Characterization of Implant-Processor Benchmarks . . . . .	126
<i>Christos Strydis, Dhara Dave, and Georgi N. Gaydadjiev</i>	
Efficient Static Buffering to Guarantee Throughput-Optimal FPGA Implementation of Synchronous Dataflow Graphs . . . . .	136
<i>Hojin Kee, Shuvra Bhattacharyya, and Jacob Kornerup</i>	
Compositional Timing Analysis . . . . .	144
<i>Amine Marref</i>	
<b>MP-SoC Programming</b>	<b>152</b>
<hr/>	
Programming Multi-core Architectures Using Data-Flow Techniques . . . . .	152
<i>Samer Arandi and Paraskevas Evripidou</i>	
CLI-Based Compilation Flows for the C Language . . . . .	162
<i>Erven Rohou, Andrea C. Ornstein, and Marco Cornero</i>	
Design Space Exploration of Instruction Set Customizable MPSoCs for Multimedia Applications . . . . .	170
<i>Unmesh D. Bordoloi, Huynh Phung Huynh, Tulika Mitra, and Samarjit Chakraborty</i>	

<b>Network-On-Chip Interconnects</b>	<b>178</b>
Enhancements for Variable N-point Streaming FFT/IFFT on REDEFINE, a Runtime Reconfigurable Architecture . . . . .	178
<i>N.Thambi Prashank, M. Prasadarao, Avinaba Dutta, Keshavan Varadarajan, Mythri Alle, and Soumitra Kumar Nandy</i>	
On-chip Network Interfaces supporting automatic burst write creation, posted writes and read prefetch . .	185
<i>Radu Stefan, Jason de Windt, and Kees Goossens</i>	
Monitor-Adapter Coupling for NOC Performance Tuning . . . . .	193
<i>Débora Matos, Caroline Concatto, Anelise Kologeski, Luigi Carro, Fernanda Kastensmidt, Altamiro Susin, and Márcio Kreutz</i>	
<b>Compiler Techniques</b>	<b>200</b>
Compile-time GPU Memory Access Optimizations . . . . .	200
<i>Gert-Jan van den Braak, Bart Mesman, and Henk Corporaal</i>	
Code Generation for a Novel STA Architecture by Using Post-Processing Backend . . . . .	208
<i>Xiaoyan Jia and Gerhard Fettweis</i>	
Accelerating High-Level Engineering Computations by Automatic Compilation of Geometric Algebra to Hardware Accelerators . . . . .	216
<i>Jens Huthmann, Peter Müller, Florian Stock, Dietmar Hildenbrand, and Andreas Koch</i>	
OpenCL-based Design Methodology for Application-Specific Processors . . . . .	223
<i>Pekka Jääskeläinen, Carlos S. de la Lama, Pablo Huerta, and Jarmo Takala</i>	
<b>Micro-Architecture</b>	<b>231</b>
LV*: A Low Complexity Lazy Versioning HTM Infrastructure . . . . .	231
<i>Anurag Negi, MM Waliullah, and Per Stenström</i>	
A Polymorphic Register File for Matrix Operations . . . . .	241
<i>Cătălin Ciobanu, Georgi Kuzmanov, Georgi Gaydadjiev, and Alex Ramirez</i>	
Interleaving Granularity on High Bandwidth Memory Architecture for CMPs . . . . .	250
<i>Felipe Cabarcas, Alejandro Rico, Yoav Etsion, and Alex Ramirez</i>	
Automatic Port and Bus Sizing in NoGAP . . . . .	258
<i>Per Karlström, Wenbiao Zhou, and Dake Liu</i>	
<b>Design Space Exploration</b>	<b>265</b>
Design Space Exploration of Systolic Realization of QR Factorization on a Runtime Reconfigurable Platform . . . . .	265
<i>Prasenjit Biswas, Keshavan Varadarajan, Mythri Alle, and Soumitra Kumar Nandy</i>	
Energy-Aware Design Space Exploration of RegisterFile for Extensible Processors . . . . .	273
<i>Amir Yazdanbakhsh, Mehdi Kamal, Mostafa E. Salehi, Hamid Noori, and Sied Mehdi Fakhraie</i>	
Exploring the Unified Design-Space of Custom-Instruction Selection and Resource Sharing . . . . .	282
<i>Marcela Zuluaga and Nigel Topham</i>	

<b>Special Session on Software Defined Radio (SDR) and Cognitive Radio (CR)</b>	<b>292</b>
Introduction to the Special Session on Software Defined Radio (SDR) and Cognitive Radio (CR) . . . . .	292
<i>John Glossner</i>	
A GPU Implementation for two MIMOOFDM Detectors . . . . .	293
<i>Teemu Nyländén, Janne Janhunen, Olli Silvén, and Markku Juntti</i>	
CORDIC-Based LMMSE Equalizer for Software Defined Radio . . . . .	301
<i>Murugappan Senthilvelan, Javier Hormigo, Joon Hwa Chun, Mihai Sima, Daniel Iancu, Michael Schulte, and John Glossner</i>	
On the Scalability of SIMD Processing for Software Defined Radio Algorithms . . . . .	309
<i>Peter Westermann and Hartmut Schröder</i>	
SDR Platform for 802.11n and 3-GPP LTE . . . . .	318
<i>Jeroen Declerck, Praveen Raghavan, Frederik Naessens, Tom Vander Aa, Lieven Hollevoet, Antoine Dejonghe, and Liesbet Van der Perre</i>	
ARAL-CR: An Adaptive Reasoning and Learning Cognitive Radio Platform . . . . .	324
<i>Sao-Jie Chen, Pao-Ann Hsiung, Chu Yu, Mao-Hsu Yen, Sakir Sezer, Michael Schulte, and Yu-Hen Hu</i>	

<b>Special Session on Multicore Architectures for Embedded Systems</b>	<b>332</b>
--	------------

Introduction to the Special Session on Multicore Architectures for Embedded Systems . . . . .	332
<i>Luigi Carro and Stephan Wong</i>	
Exploration Framework for Run-Time Resource Management of Embedded Multi-Core Platforms . . . . .	333
<i>Ch. Ykman-Couvreur</i>	
Towards Scalable I/O on a Many-core Architecture . . . . .	341
<i>Michael A. Hicks, Hicks Michiel, W. van Tol, and Chris R. Jesshope</i>	
Embedded Multicore Architectures for LDPC Decoding . . . . .	349
<i>Gabriel Falcao, Leonel Sousa, and Vitor Silva</i>	
Message Passing Interface Support for the Runtime Adaptive Multi-Processor System-on-Chip RAMPSoC	357
<i>Diana Göhringer, Michael Hubner, Laure Hugot-Derville, and Jürgen Becker</i>	
Designing and Validating Access Policies to Reconfigurable Resources in Multiprocessor Systems on Chip	365
<i>Fabio Arlati, Francesco Bruschi, and Donatella Sciuto</i>	
Identifying Communication Models in Process Networks derived from Weakly Dynamic Programs . . . . .	372
<i>Dmitry Nadezhkin and Todor Stefanov</i>	



<b>Author Index</b> . . . . .	<b>380</b>
-------------------------------	------------