

2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology

(ICSICT 2010)

**Shanghai, China
1 – 4 November 2010**

Pages 1-689



**IEEE Catalog Number: CFP10829-PRT
ISBN: 978-1-4244-5797-7**

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	¹ Beijing Microelectronic Institute, Beijing, China; ² China Aerospace Corporation, Beijing, China; ⁴ Beijing Microelectronics Center, Beijing, China; ⁵ China Academy of Science, Beijing, China; ⁶ Z.H. Communication, Zhen Cheng, China; ⁷ Beijing C.T. University, Beijing, China; ⁸ Tsing Hua University, Beijing, China; ⁹ Beijing Normal University, Beijing, China; ¹⁰ Florence Science and Technology, San Jose, USA	
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	1 IBM, 5 Technology Park Dr, Westford, USA; 2 IBM, 1000 River St, USA	
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	¹ National United University, Taiwan, China; ² I-Shou University, Taiwan, China	
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	¹ Nanjing University, China; ² SMIC, P. R. China	
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	¹ ST-Ericsson, Sweden; ² ST-Ericsson, France	
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	¹ University of Calabria, Italy; ² University of Pisa, Italy; ³ Indian Institute of Technology, India	
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	¹ Peking University Shenzhen Graduate School, , China; ² TSRC, Peking University, China; ³ PKU HKUST Shenzhen Institute, China; ⁴ Shanghai Institute of Microsystems and Information Technology, Chinese Academy of Sciences	
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	¹ Peking University Shenzhen Graduate School, China; ² Peking University, China,	
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	¹ Asia University, Taiwan, China; ² Vanguard International Semiconductor Corp., Taiwan, China	
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	¹ Institute of Microelectronics of Chinese Academy and Sciences, China ² Columbia University, USA	
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	¹ Ying Zhang, ² Miao Li, ¹ Yuxia Shi, ¹ Li Zhang and ¹ Yan Wang	
	¹ Tsinghua University, China; ² Accelicon Technologies, Inc, China	
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	¹ Nankai University, P. R. China; ² Tianjin Medical University, P. R. China	
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	¹ University of Electronic Science and Technology of China, PR China	
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	¹ Accelicon Technologies, Inc, USA; ² Qualcomm 5775 Morehouse Drive San Diego, USA	
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	¹ Peking University Shenzhen Graduate School, P. R. China; ² Peking University, P. R. China; ³ PKU HKUST Shenzhen Institute, P. R. China	
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	Lining Zhang ^{1,2,3,4} , Haijun Lou ¹ , Zhiwei Liu ² , Frank He ^{1,2,3} , and Mansun Chan ⁴	
	¹ Peking University Shenzhen Graduate School, China; ² Peking University Shenzhen SOC Key Laboratory, China; ³ TSRC, IME, Peking University, China; ⁴ Hong Kong University of Science and Technology	
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	¹ PekingUniversity Shenzhen Graduate School, P. R. China; ² Peking University Shenzhen SOC Key Laboratory, P. R. China; ³ Hong Kong University of Science and Technology, Hong Kong	

P14_15	An Analog CMOS Pulse Coupled Neural Network for Image Segmentation	1883
	Ying Xiong ¹ , Wei-Hua Han, Kai Zhao, Yan-Bo Zhang, Fu-Hua Yang	
	¹ Chinese Academy of Science, China	
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	University of Electronic Science and Technology of China, China	
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	Cai Jueping ¹ , Huang Gang ¹ , Wang Shaoli ² , Yao Lei ² , Li Zan ² and Hao Yue ¹	
	¹ Wide Bandgap Semiconductor Technology Disciplines State Key Laboratory, Xidian University, China; ² State Key Laboratory of Integrated Services Networks, Xidian University, China	
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	Wenfeng Lou, Xiaozhou Yan, Zhiqing Geng, ⁽²⁾ Zhihua Wang, ⁽¹⁾ Nanjian Wu	
	⁽¹⁾ Chinese Academy of Sciences, P. R. China; ⁽²⁾ Tsinghua University, China	
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	Jin-ying Zhang ^{1,2} , Xin-ming Ji ¹ , Wei-jiang Xu ² , Julien Carlier ² , Bertrand Nongaillard ² , Yi-ping Huang ¹	
	¹ Fudan University, P. R. China; ² Université de Valenciennes et du Hainaut Cambrésis, France	
P14_21	Performance Optimization of n-MOSFETs Using Asymmetric Interfacial Oxide layer	1901
	Weize Yu, Zhijiong Luo, Huilong Zhu, Qingqing Liang, and Haizhou Yin	
	Institute of Microelectronics of Chinese Academy of Sciences, P. R. China	
P14_22	Current Modeling and Simulation of Dual-Material Surrounding-Gate MOSFET with Asymmetric Halo	1904
	Zun-Chao L ¹ , Jin-Peng Xu, and Lin-Lin Liu	
	Xi'an Jiaotong University, China	
P14_23	LPCVD Process Simulation Based On Monte Carlo Method	1907
	Jian-Yang Dai, Zai-Fa Zhou, Qing-An Huang, Wei-Hua Li	
	Southeast University, China	
P14_24	A New Extraction Method for Source/Drain Resistance in MOSFETs	1910
	Yang-Hua Chang, Yao-Jen Liu	
	National Yunlin University of Science & Technology, Taiwan, China	
P14_25	Research on Modeling for the Pattern Library of Interconnect parasitic capacitances in VLSI	1913
	Hui Qu ¹ , Xiaoyu Xu ¹ , and Zhuoxiang Ren ²	
	¹ Chinese Academy of Sciences, China; ² UPMC University of Paris 6, France	

P14_26	A High Speed Low Power Interface for Inter-die Communication	1916
	Siliang Hua ¹ , Qi Wang ^{1,2} , Hao Yan ^{1,2} , Donghui Wang ¹ , Chaohuan Hou ¹	
	¹ Institute of Acoustics, Chinese Academy of Sciences, China; ² Graduate University of Chinese Academy of Sciences, China	
P14_27	A Threshold Voltage Model for the Surrounding-Gate MOSFETs	1919
	Guanghui Mei, Guangxi Hu, Peicheng Li, Jinglun Gu, Ran Liu and Tingao Tang	
	Fudan University, China	
P14_28	An Analytic Threshold Voltage Model for the Double-Gate Schottky-Barrier Source/Drain MOSFETs	1922
	Peicheng Li, Guangxi Hu, Guanghui Mei, Ran Liu, Yi Jiang and Tingao Tang	
	Fudan University, China	
P14_29	A Simplified Simulation Model for CMOS Integrated Hall Devices Working at Low Magnetic Field Circumstance	1925
	Yue Xu, Fei-Fei Zhao	
	Nanjing University of Posts and Telecommunications, China	
P14_30	Design and Simulation of the vertical pnp transistor on SOI	1928
	JieXin Luo ¹ , Jing Chen, JianHua Zhou, QingQing Wu, XiaoLu Huang, Xi Wang	
	¹ Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, China	
P14_31	Analytical models of the transition layer in HEMTs on silicon substrate for device simulation	1931
	Petru Andrei	
	Florida State University, USA	
P14_32	Improved mobility model of MOSFETs for device simulation	1934
	Wu Qingqing, Chen Jing, Wang Xi	
	Shanghai Institute of Microsystem and Information Technology, CAS, China	
P14_33	On Dynamic Behavior of Triangular Shaped Cantilevers in MEMS Sensors: Effect of Curvature	1937
	Gui-Ming Zhang ¹ , Li-Bo Zhao ^{2,1} , En-Ze Huang ¹ , Guo-Ying Yuan ¹ , Yong Li ² , Zhi-Gang Liu ³ and Zhuang-De Jiang ¹	
	¹ Xi'an Jiaotong University, China; ² Tsinghua University, China ³ Xi'an Jiaotong University, China	
P14_34	Modeling Low Frequency Noise in PDSOI MOSFETs for Analog and RF Applications	1940
	S. Sirohi ¹ and S. Khandelwal ¹	
	¹ IBM Semiconductor Research & Development Centre, India	
P14_35	Simple Approach for Statistical Modeling of Process Impacts on CMOS Device Variations in VLSI Applications	1943
	Meng Li, Qingqing Liang, Huicai Zhong, and Huilong Zhu	
	Institute of MicroElectronics of Chinese Academy of Sciences, China,	
P14_36	Modeling the Parasitic Bipolar Device in the 40nm PD SOI NMOS Device Considering the Floating Body Effect	1946
	C. H. Chen, J. B. Kuo, D. Chen, and C. S. Yeh	
	National Taiwan University, Taiwan, China; UMC, Taiwan, China	

P14_37	Evaluation the Layout Dependences on Strained 22nm NMOSFETs	1949
	Jieyu Qin ^{1,2} , Gang Du ² , Ruqi Han ² , Xiaoyan Liu ²	
	¹ Shenzhen Graduate School, Peking University, China; ² Institute of Microelectronics, Peking University, China	
P14_38	Study of 20nm bulk FINFET by Using 3D full band Monte Carlo Method with Effective Potential Quantum Correction	1952
	Gang Du ¹ , Wei Zhang ² , Juncheng Wang ¹ , Tiao Lu ² , Pingwen Zhang ² , Xiaoyan Liu ¹	
	¹ Institute of Microelectronics, Peking University, China; ² School of Mathematical Sciences, LMAM and CAPT, Peking University, China	
P14_39	Collision Based Capacitive Vibration Energy Harvesting	1955
	Ling Bu, Xiaoming Wu, Litian Liu	
	Tsinghua University, China	
P14_40	Predictive Modeling of Capacitance and Resistance in Gate-all-around Cylindrical Nanowire MOSFETs for Parasitic Design Optimization	1958
	Qiumin Xu, Jibin Zou, Jieyin Luo, Runsheng Wang, Ru Huang	
	Peking University, China	
Packaging and testing technology		
P15_01	A Vacuum/airtight Package with Multifunctional LTCC Substrate and Integrated Pirani Vacuum Gauge for 3D SIP Integration Applications	1961
	Min Miao ^{1,2} , Hua Gan ^{2,3} , Yufeng Jin ² , Zhensong Li ¹	
	¹ Beijing Information Science and Technology University, China; ² Peking University, China; ³ Shenzhen Graduate School of Peking University, China	
P15_02	Study on The Accelerated Soakage Testing during The Reliability Evaluation of Plastic Package	1964
	Qian Min ¹ , Yang Cuijun ¹ , Yuan Hua ^{1,2} , Cao Yunpeng ¹	
	Suzhou University, China	
P15_04	Design and Implementation of a Differential Power Analysis System for Cryptographic Devices	1967
	Cong Chen, Xiangyu Li, Liji Wu, Xiangmin Zhang	
	Institute of Microelectronics of Tsinghua University, China	
P15_05	The implementation of the global scheduling strategy	1970
	Jinyi Zhang ^{1,3} , Wanlin Cai ² , Chunhua Wang ³	
	¹⁻³ Shanghai University, China	
P15_06	Improved Delay Fault Coverage in SoC Using Controllable Multi-Scan-Enable	1973
	Jin-yi ZHANG ^{1,3} , Xu-hui HUANG ² , Wan-lin CAI ² , Han-yi WENG ^{1,3}	
	¹⁻³ Shanghai University, China	
P15_07	Automated Test Bitstream Generation for an SOI-Based FPGA	1976
	Yan Li, Stanley L. Chen, Liang Chen, Qianli Zhang, Ming Li	
	Chinese Academy of Sciences, China	
P15_08	State-Space-based Uncertainty Analysis for Identification of Faulty Behaviour	1979
	H J Kadim	

	LJMU, UK	
Solar cell & other devices for new energy sources		
I17_01	Surface Texturing of Si thin film solar cells via Low Cost Periodic Nanopillars Array to Enhance Efficiency	1982
(Invited)	HongYu Yu	
	Nanyang Technological University, Singapore	
I17_02	High-efficiency silicon heterojunction solar cells: From physics to production lines	1986
(Invited)	S. De Wolf ¹ , Y. Andraut ² , L. Barraud ¹ , R. Bartlome ¹ , D. Bätzner ² , P. Bôle ¹ , G. Choong ¹ , B. Demareux ¹ , A. Descoeur ¹ , C. Guérin ² , N. Holm ² , M. Kobas ² , D. Lachenal ² , B. Mendes ² , B. Strahm ² , M. Tefai ² , G. Wahli ² , F. Wuensch ² , F. Zicarelli ¹ , A. Buechel ² and C. Ballif ¹	
	¹ Ecole Polytechnique Fédérale de Lausanne (EPFL), Institute of micro engineering (IMT), Photovoltaics and thin film electronics laboratory, Switzerland; ² Roth & Rau Switzerland (RRS), Switzerland	
I17_03	Potential Application of Thin-film Nanotechnologies in Third-Generation Si Solar Cells	1990
(Invited)	Jia-Min Shieh, Chang-Hong Shen, Ting-Jen Hsueh, Wen-Hsien Huang, Bau-Tong Dai, and Fu-Liang Yang	
	¹ National Nano Device Laboratories, Taiwan, China	
I17_04	Germanium-doped Crystal Silicon for solar cells	1994
(Invited)	Deren Yang ¹ , Xuegong Yu, Xiaoqiang Li, Peng Wang, Lei Wang	
	¹ Zhejiang University, China	
P17_01	Influence of Measurement Parameter on Dye-sensitized Solar Cell Efficiency	1995
	Hanmin Tian ^{1,2} , Xiangyan Wang ^{1,3} , Tao Yu ^{1,3} and Zhigang Zou ^{1,3}	
	¹ Nanjing University, Nanjing 210093, P.R. China; ² Hebei University of Technology, P.R. China; ³ National Laboratory of Solid State Microstructures, P.R. China	
P17_02	Effect of the band gap of the window layer on the properties of silicon heterojunction solar cells	1998
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	¹ Shan Dong University, China; ² Xi'an JiaoTong University, China	
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	¹ Florida A&M University and Florida State University, USA; ² Center for Advanced Power Systems, Florida State University, USA; ³ U.S. Army CERDEC, USA	
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