2010 NORCHIP

Tampere, Finland
15 – 16 November 2010

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Monday 15 November 2010

09:00 **Opening and welcome**
Jari Nurmi, Tampere University of Technology (FI)

09:15 **Invited talk: Testing and Design-for-Testability Techniques for 3D Integrated Circuits**
Krishnendu Chakrabarty,Duke University (US)

10:00 **Ultra Low Energy vs Throughput Design Exploration of 65 nm Sub-VT CMOS Digital Filters (page 1)**
Syed Muhammad Yasser Sherazi et al, Lund University (SE)

10:20 **Research and Practices on 3D Networks-on-Chip Architectures (page 5)**
Amir-Mohammad Rahmani et al, University of Turku (FI)

1.1 Analog Circuits

11:10 **A Low Power Analog Channel Decoder for Ultra Portable Devices in 65 nm Technology (page 11)**
Reza Meraji et al, Lund University (SE)

11:30 **Analog Baseband Chain of Synthetic Array Radar (SAR) Receiver (page 16)**
Faizah Abu Bakar et al, Aalto University (FI)

11:50 **A 900 MHz 10 mW Monolithically Integrated Inverse Class E Power Amplifier (page 20)**
Jukka Typpö, NTNU (NO)

1.2 Memory Architecture

11:10 **An Analysis of Designing 2D/3D Chip Multiprocessor with Different Cache Architecture (page 24)**
Thomas Canhao Xu et al, University of Turku (FI)

11:30 **A NoC Based Distributed Memory Architecture with Programmable and Partitionable Capabilities. (page 30)**
Muhammad Adeel Tajammul et al, Royal Institute of Technology (SE)

11:50 **On Power and Performance Tradeoff of L2 Cache Compression (page 36)**
Tom Chen et al, Colorado State University (US)

12:10 **Lunch**

13:30 **Invited talk: Towards Self-Powered Biomedical Devices**
Yong Lian, National University of Singapore

2.1 D/A Converters

14:15 **Effects of Filtering on the Linearity of Current-steering IF DAC (page 40)**
Timo Rahkonen et al, Oulu University (FI)

14:35 **A Higher Nyquist-Range DAC Employing Sinusoidal Interpolation (page 44)**
Reza Sadeghifar et al, Linköping University (SE)

2.2 High-Level Modeling

14:15 **Execution Models for Processors and Instructions (page 48)**
Florian Brandner et al, ENS de Lyon (FR)

14:35 **Analysis of Modeling Styles on Network-on-Chip Simulation (page 52)**
Lasse Lehtonen et al, Tampere Univ. of Technology (FI)

3. Poster Session I

14:55 **Coffee / Poster Session**

High Level Synthesis Framework For a Coarse Grain Reconfigurable Architecture (page 56)
Omer Malik et al, Royal Institute of Technology (SE)

Designing a dataflow processor using ClaSH (page 62)
Anja Niedermeier et al, University of Twente (NL)

An Improved Hardware Acceleration Scheme for Java Method Calls (page 66)
Tero Säntti et al, University of Turku (FI)

Exploration of Target Architecture for a Wireless Camera Based Sensor Node (page 72)
Muhammad Imran et al, Mid Sweden University (SE)

FPGA-based Real-Time Disparity Computation and Object Location (page 76)
Pedro Miguel Santos et al, Universidade do Porto (PT)

Application Of Medium-Grain Multiprocessor Mapping Methodology To Epileptic Seizure Predictor (page 80)
Elena Hammari et al, NTNU (NO)

DLL based temperature compensated MEMS clock (page 86)
Arto Rantala et al, VTT Finland (FI)

Modeling of Peak-to-peak Switching Noise along a Vertical Chain of Power Distribution TSV pairs in a 3D Stack of ICs interconnected through TSVs (page 90)
Waqar Ahmad et al, Royal Institute of Technology (SE)

A Fast and Accurate Phase Noise Measurement of Free Running Oscillators Using a Single Spectrum Analyzer (page 96)
JIan Chen et al, Royal Institute of Technology (SE)

A Novel Simple And High Performance Structure For Improving CMRR: Application to Current Buffers and Folded Cascode Ampilifier (page 100)
Amir Hossein Miremadi et al, Islamic Azad University (IR)

A Low-Power, Medium-Resolution, High-Speed CMOS Pipelined ADC (page 104)
*Deivasigamani Meganathan et al,*Madras Institute of Technology (IN)

Dimensioning Space of a Parallel Tuned Amplifier (page 108)
Simo Hietakangas, University of Oulu (FI)

A Self-Oscillating LNA-Mixer (page 112)
Tero Koivisto et al, University of Turku (FI)

A New DFT based Approach for Gain Mismatch Detection and Correction in Time-Interleaved ADCs (page 116)
Yashar Hesamiafshar et al, Urmia University (IR)

Low Power and Optimal Delay Multi Threshold Voltage Level Converters (page 120)
Rajendra Naik

Developments of the SoC for High-Multi-Level QAM 1 Gbps Class Wireless System and its Evaluation with RF Hardware of 38 GHz Band FWA (page 124)
Toru Taniguchi et al, Japan Radio Co (JP)

Study of Modified Noise-Shaper Architectures for Oversampled Sigma-Delta DACs (page 128)
Nadeem Afzal et al, Linköping University (SE)

4.1 RF: Low-Noise Amplifiers

16:00 **A DC-Invariant Gain Control Technique for CMOS Differential Variable-Gain Low-Noise Amplifiers (page 132)**
Muh-Dey Wei et al, Aachen University (DE)

16:20 **A Small-Area Self-Biased Wideband CMOS Balun LNA with Noise Cancelling and Gain Enhancement (page 136)**
J. R. Custódio et al, Universidade Nova de Lisboa (PT)

16:40 **Wideband Inductorless LNA Employing Simultaneous 2nd and 3rd Order Distortion Cancellation (page 140)**
Omid E Najari et al, Linköping University (SE)

4.2 Manycore Systems

16:00 **Multi-Application Multi-Step Mapping Method for Many-Core Network-on-Chips (page 144)**
Bo Yang et al, University of Turku (FI)

16:20 **Multi-FPGA Implementation of a Network-on-Chip Based Many-core Architecture with Fast Barrier Synchronization Mechanism (page 150)**
Xiaowen Chen et al, Royal Institute of Technology (SE)

16:40 **Latency Reduction of Selected Data Streams in Network-on-Chips for Adaptive Manycore Systems (page 154)**
Thilo Pionteck et al, Universität zu Lübeck (DE)

Tuesday 16 November 2010

09:00 **Invited talk: Sensor Processing and Power Management in Smartphone Platforms**
*Lasse Harju,*ST-Ericsson (FI)

5.1 Time-to-Digital Converters

09:45 **A High-resolution Vernier Gated-Ring-Oscillator TDC in 90-nm CMOS (page 160)**
Ping Lu et al, Lund University (SE)

10:05 **A 12-Bit Digital- to-Time Converter (DTC) for Time-to-Digital Converter (TDC) and Other Time Domain Signal Processing Applications (page 164)**
Salim Alahdab et al, University of Oulu (FI)

5.2 FPGA Applications

09:45 **Exploring FPGAs Capability to Host a HPC Design (page 168)**
Clement Foucher et al, Université de Nice-Sophia Antipolis (FR)

10:05 **Flexible Hardware Implementation of Collaborative GNSS Tracking Channel (page 172)**
Heikki Hurskainen et al, Tampere Univ. of Technology (FI)

6. Poster Session II

10:25 **Coffee / Poster Session**

Simulation of Thermal Behavior for Networks-on-Chip (page 176)
Tim Wegner et al, University of Rostock (DE)

Traffic Characterization for Multicasting in NoC (page 180)
V. Laxmi et al, National Institute of Technology (IN)

SoC Chip Scheduler Embodying I-SLIP Algorithm (page 186)
Trupti B. Salankar et al, SRKNEC, NAGPUR

Layered Spiral Algorithm for Memory-Aware Mapping and Scheduling on Network-on-Chip (page 194)
Shuo Li et al, Royal Institute of Technology (SE)

Implementation Exploration for a Self Reconfigurable Interconnection Network in DRRA (page 200)
Muhammad Ali Shami et al, Royal Institute of Technology (SE)

Hierarchical Power Monitoring on NoC - A Case Study for Hierarchical Agent Monitoring Design Approach (page 206)
Liang Guang et al, University of Turku (FI)

High-Performance NoC Interface with Interrupt Batching for Micronmesh MPSoC Prototype Platform on FPGA (page 212)
Heikki Kariniemi et al, Tampere University of Technology (FI)

NoC-based CSP Support for a Java Chip Multiprocessor (page 218)
Flavius Gruian et al, Lund University (SE)

Calibration of Sigma Delta Analog-to-Digital Converters Based on Histogram Test Methods (page 224)
Armin Jalili et al, Isfahan University of Technology (IR)

A Second-Order Low-Power ΔΣ Modulator For Pressure Sensor Applications (page 228)
Tero Nieminen et al, Aalto University (FI)

A 500-MHz Low-Voltage Programmable Gain Amplifier for HD Video in 65-nm CMOS (page 232)
Syed Ahmed Aamir et, Syed Ahmed Aamir et

A Novel Transimpedance Amplifier with Variable Gain (page 236)
Pietro Monsurrò et al, Università di Roma (IT)

Diode Based Charge Pump Design using 0.35µm Technology (page 240)
Muahammad Adeel Ansari et al, Royal Institute of Technology (SE)

An 8-bit 166nw 11.25 kS/s 0.18um two-Step-SAR for RFID applications Using Novel DAC Architecture (page 244)
Iman Kianpour et al, Sabzevar Tarbiat Moallem University (IR)

Digital PVT Calibration of a Frequency-to-Voltage Converter (page 248)
Jørgen Andreas Michaelsen et al, University of Oslo (NO)

7.1 Receivers and Transmitters

11:10 **A 175µW 100MHz-2GHz inductorless receiver front-end in 65nm CMOS (page 252)**
Carl Bryant et al, Lund University (SE)

11:30 **Higher order FFSFR coupled micromechanical mixer-filters integrated in CMOS (page 256)**
Jan Erik Ramstad et al, University of Oslo (NO)

11:50 **A 9.2pJ/pulse UWB-IR Transmitter with Tunable Amplitude for Wireless Sensor Tags in 0.18um CMOS (page 260)**
David Sarmiento Mendoza et al, Royal Institute of Technology (SE)

7.2 Dependability and Testing

11:10 **High-Level Design Error Diagnosis Using Backtrace on Decision Diagrams (page 264)**
Jaan Raik et al, Tallinn University of Technology (EE)

11:30 **Generic Partial Dynamic Reconfiguration Controller for Fault Tolerant Designs Based on FPGA (page 268)**
Martin Straka et al, Brno University of Technology (CZ)

11:50 **SfW Method: Delay Test Generation for Simple Chain Wrapper Architecture (pae 272)**
Marcel Balaz, Slovak Academy of Sciences (SK)

12:10 **Lunch**

13:10 **Invited talk: Purely-Digital *versus* Mixed-Signal Self-Calibration Techniques in High-Resolution Pipeline ADCs (page 276)**
*Joao Goes,*Universidade Nova de Lisboa (PT)

8.1 A/D Converters

13:55 **On CMOS Scaling and A/D-Converter Performance (page 284)**
Bengt E. Jonsson, ADMS Design AB (SE)

14:15 **An 1.2V 440-MS/s 0.13-µm CMOS Pipelined Analog-to-Digital Converter With 5-8bit Mode Selection (page 288)**
Tero Nieminen, Aalto University (FI)

14:35 **A 290uA, 3.2 MHz 4-bit Phase ADC for Constant Envelope, Ultra-low Power Radio (page 292)**
Budhaditya Banerjee et al, CSEM (CH)

14:55 **Design of CMOS Sampling Switch for Ultra-Low Power ADCs in Biomedical Applications (page 296)**
Dai Zhang et al, Linköping University (SE)

8.2 Network-on-Chip

13:55 **Energy Aware Design Methodologies for Application Specific NoC (page 300)**
Naveen Choudhary et al, Malaviya National Institute of Technology (IN)

14:15 **A Scalable, Non-Interfering, Synthesizable Network-on-Chip Monitor (page 304)**
Antti Alhonen et al, Tampere University of Technology (FI)

14:35 **An Efficient VFI-Based NoC Architecture Using Johnson-Encoded Reconfigurable FIFOs (page 310)**
Amir-Mohammad Rahmani et al, University of Turku (FI)

14:55 **A Hybrid NoC Combining SDM-Based Circuit Switching with Packet Switching for Real-Time Applications (page 315)**

Angelo Kuti Lusala et al, UC Louvain (BE)

15:15 **Closing remarks and NORCHIP 2011**